19-1537; Rev 0; 7/99

MAXIM

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

General Description

The MAX3676 is a complete clock-recovery and data-retiming IC incorporating a limiting amplifier. It is intended for 622Mbps SDH/SONET applications and operates from a single +3.3V supply.

The MAX3676 is designed for both section-regenerator and terminal-receiver applications in OC12/STM-4 transmission systems. Its jitter performance exceeds all SONET/SDH specifications.

The MAX3676 has two differential input amplifiers: one accepts positive-referenced emitter-coupled logic (PECL) levels, while the other accepts small-signal analog levels. The analog inputs access the limiting amplifier stage, which provides both a received-signal-strength indicator (RSSI) and a programmable-threshold loss-of-power (LOP) monitor. Selecting the PECL amplifier disables the limiting amplifier, conserving power. A loss-of-lock (LOL) monitor is also incorporated as part of the fully integrated phase-locked loop (PLL).

Applications

SDH/SONET Receivers and Regenerators
SDH/SONET Access Nodes
Add/Drop Multiplexers
ATM Switches
Digital Cross-Connects

Features

- **Single +3.3V or +5.0V Power Supply**
- **Exceeds ITU/Bellcore SDH/SONET Regenerator Specifications**
- **Low Power: 237mW at +3.3V**
- **Selectable Data Inputs, Differential PECL or Analog**
- **Received-Signal-Strength Indicator**
- **Loss-of-Power and Loss-of-Lock Monitors**
- **Differential PECL Clock and Data Outputs**
- **No External Reference Clock Required**

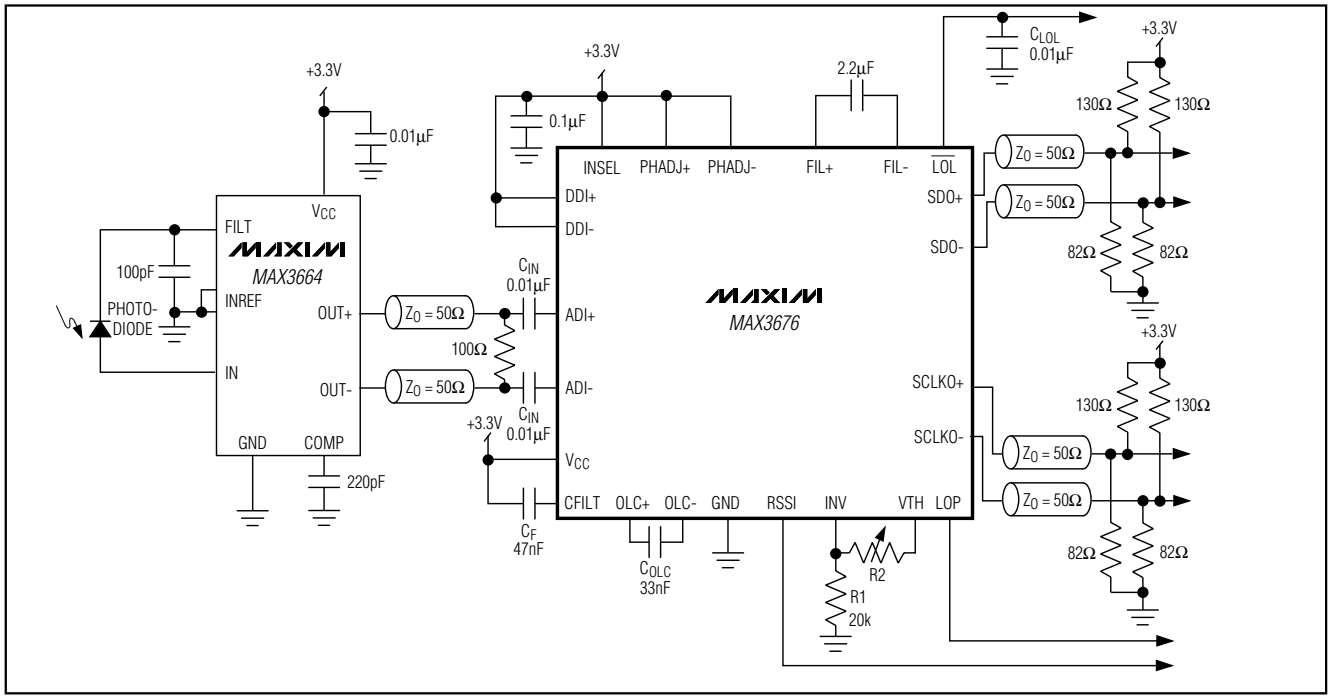
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3676EHJ	-40°C to +85°C	5mm 32 TQFP
MAX3676E/D	-40°C to +85°C	Dice*

**Contact factory for availability. Dice are designed to operate over a -40°C to +140°C junction temperature (T_J) range, but are tested and guaranteed at T_J = +45°C.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .....-0.5V to +6.5V
Input Voltage Levels,
DDI+, DDI-, ADI+, ADI- .....-0.5V to (V_{CC} + 0.5V)
Input Differential Voltage (ADI+) - (ADI-) .....±3V
PECL Output Currents, SDO+, SDO-, SCLKO+, SCLKO- ...100mA
$\overline{LOL}$, LOP, INSEL, PHADJ+, PHADJ- .....-0.5V to (V_{CC} + 0.5V)
FIL+, FIL-, OLC+, OLC-, RSSI, VTH .....-0.5V to (V_{CC} + 0.5V)
(OLC+) - (OLC-) .....±3V
(FIL+) - (FIL-) .....±700mV
CFILT .....(V_{CC} - 2.5V) to (V_{CC} + 0.5V)
INV .....-0.5V to +2.0V
Continuous Power Dissipation (T_A = +85°C)
TQFP (derate 11.1mW/°C above +85°C) 721mW
Operating Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Processing Temperature (die) .....+400°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	MAX3676EHJ, PECL outputs unterminated	INSEL = V_{CC}		72	111	mA
			INSEL = GND		51	81	
PECL Input Voltage High	V_{IH}			V_{CC} - 1.16		V_{CC} - 0.88	V
PECL Input Voltage Low	V_{IL}			V_{CC} - 1.81		V_{CC} - 1.48	V
PECL Input Current High	I_{IH}			-10		10	µA
PECL Input Current Low	I_{IL}			-10		10	µA
PECL Output Voltage High	V_{OH}	T_A = 0°C to +85°C		V_{CC} - 1.025		V_{CC} - 0.88	V
		T_A = -40°C		V_{CC} - 1.085		V_{CC} - 0.88	
PECL Output Voltage Low	V_{OL}	T_A = 0°C to +85°C		V_{CC} - 1.81		V_{CC} - 1.620	V
		T_A = -40°C		V_{CC} - 1.83		V_{CC} - 1.555	
LOP, LOL Voltage High	V_{OH}			2.4			V
LOP, LOL Voltage Low	V_{OL}			0.1		0.4	V
INV Input Bias Voltage		4kΩ between INV and VTH		1.10	1.23	1.30	V

Note 1: Dice are tested at T_j = +45°C, V_{CC} = +4.25V.
Note 2: At T_A = -40°C, DC characteristics are guaranteed by design and characterization.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Input Voltage Range	V_{ID}	BER < 10^{-10}, ADI inputs (Note 5)		0.003		1.2000	Vp-p
Input-Referred Noise	V_N	ADI inputs			80		μV_{RMS}
Power-Detect Hysteresis		(Notes 6, 7)		3		6	dB
Limiting Amplifier Small-Signal Bandwidth	BW	(Note 8)			650		MHz
RSSI Output Voltage		(ADI+) - (ADI-) = 2mVp-p			1.40		V
		(ADI+) - (ADI-) = 20mVp-p			1.93		
Threshold Voltage	V_{TH}	(Note 7)			1.41		V
LOP Threshold Accuracy		(Note 7)		-2		+2	dB
RSSI Linearity		(ADI+) - (ADI-) = 2mVp-p to 50mVp-p			±0.7		%
RSSI Slope		(ADI+) - (ADI-) = 2mVp-p to 50mVp-p (Note 9)			26		mV/dB
Loop Bandwidth		C_F = 2.2µF			250	500	kHz
Jitter Generation (Note 10)		C_F = 2.2µF			2.0	2.6	mUI
Jitter-Transfer Peaking		C_F = 2.2µF			0.03	0.08	dB
Jitter Tolerance (Note 11)		C_F = 2.2µF	f = 10kHz		8.9		UI
			f = 25kHz	(Note 12)	3.64		
			f = 250kHz	0.55	0.77		
			f = 1MHz	0.45	0.69		
Maximum Consecutive Input Run Length (1 or 0)					1200		Bits
Clock Transition Time	tr, tf	20% to 80%			205	245	ps
Data Transition Time	tr, tf	20% to 80%			180	230	ps
Serial Clock-to-Q Delay	t_{CLK-Q}			140	275	400	ps
Serial Clock Frequency	f_{SCLK}				622.08		MHz

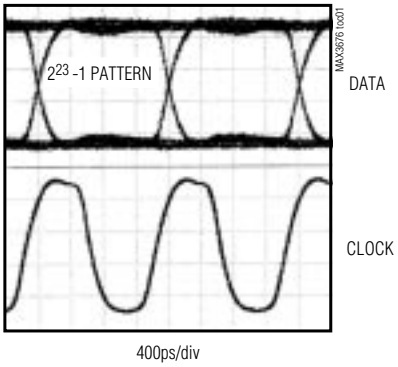
Note 3: AC parameters are guaranteed by design and characterization.
Note 4: The MAX3676 is characterized with a PRBS of 2^{23} - 1 maintaining a BER of ≤ 10^{-10} having a confidence level of 99.9%.
Note 5: A lower minimum input voltage of 2mVp-p is achievable; however, the LOP hysteresis is not guaranteed below 3.6mVp-p.
Note 6: Hysteresis = 20log($V_{RELEASE}$ / V_{ASSERT}).
Note 7: R_1 = 20kΩ, R_2 = 3.0kΩ, resulting in $V_{RELEASE}$ ≈ 3.6mVp-p.
Note 8: Small-signal bandwidth cannot be measured directly.
Note 9: RSSI slope = [V_{RSSI2} - V_{RSSI1}] / [20log (V_{ID2} / V_{ID1})].
Note 10: 1UI = 1 unit interval = $(622.08MHz)^{-1}$ = 1.608ns.
Note 11: At jitter frequencies <10kHz, the jitter tolerance characteristics exceed the ITU/Bellcore specifications. The low-frequency jitter tolerance outperforms the instrument's measurement capability.
Note 12: See *Typical Operating Characteristics* for worst-case distribution.

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

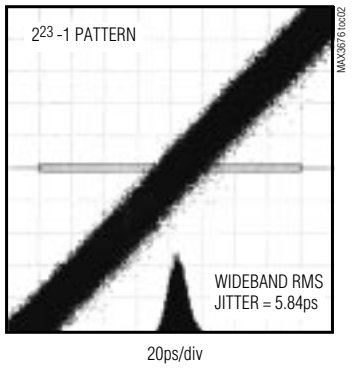
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

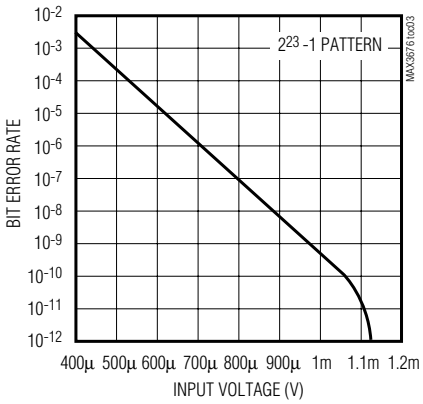
RECOVERED DATA AND CLOCK (SINGLE ENDED)



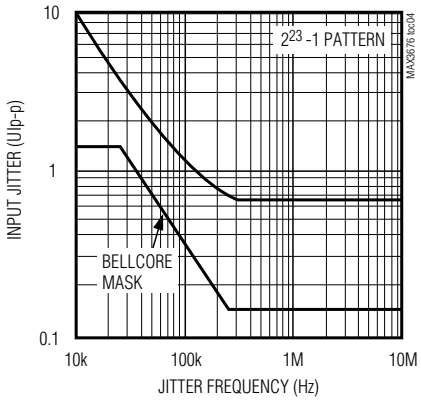
RECOVERED CLOCK JITTER



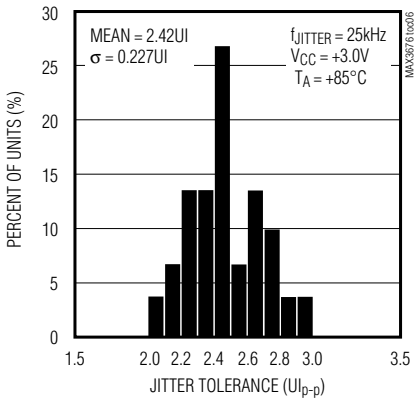
BIT ERROR RATE vs. ADI INPUT VOLTAGE



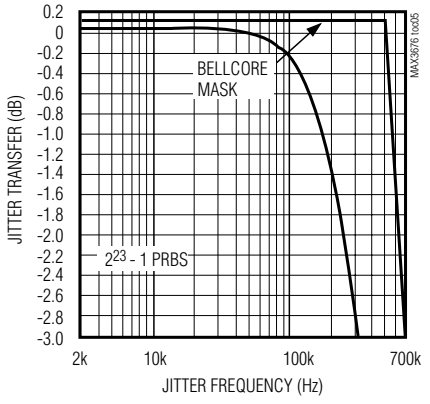
JITTER TOLERANCE



DISTRIBUTION OF JITTER TOLERANCE (WORST-CASE CONDITIONS)



JITTER TRANSFER

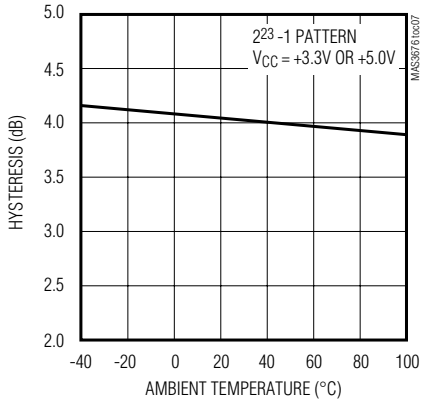


622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

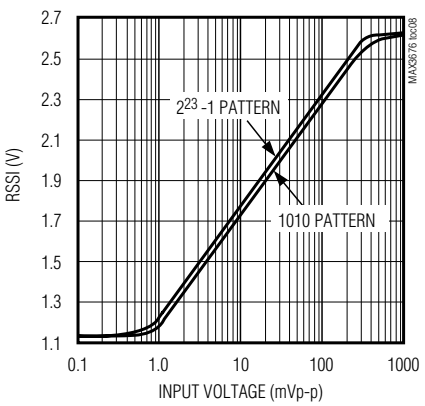
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

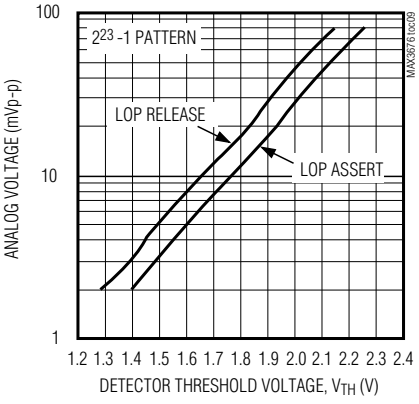
LOSS-OF-POWER HYSTERESIS vs. TEMPERATURE



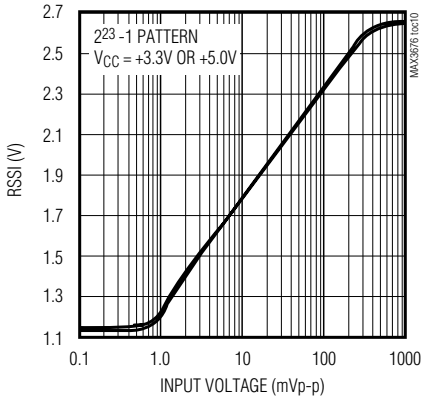
RECEIVED-SIGNAL-STRENGTH INDICATOR vs. INPUT VOLTAGE



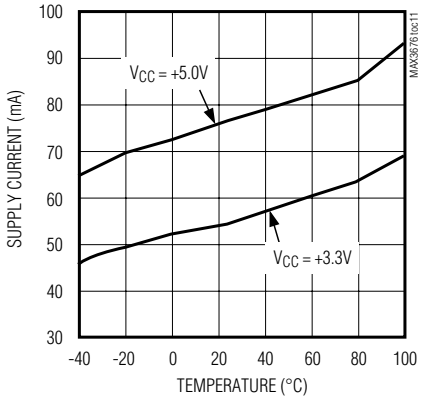
LOSS-OF-POWER ASSERT AND RELEASE LEVEL vs. DETECTOR THRESHOLD VOLTAGE



RECEIVED-SIGNAL-STRENGTH INDICATOR vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Pin Description

PIN	NAME	FUNCTION
1	OLC+	Positive Offset-Correction Loop Capacitor Input
2	OLC-	Negative Offset-Correction Loop Capacitor Input
3	RSSI	Received-Signal-Strength Indicator Output
4, 8, 16, 24, 25	GND	Supply Ground
5	INV	Op Amp Inverting Input. Attach to ground if op amp is not used.
6	VTH	Voltage Threshold Input. Threshold voltage for loss-of-power monitor. Attach to V_{CC} if LOP function is not used.
7	LOP	Loss-of-Power Output, TTL. Limiting amplifier loss-of-power monitor. Asserts high when input signal is below threshold set by VTH.
9, 12, 15, 18, 21, 31	V_{CC}	Positive Supply Voltage
10	SCLKO-	Negative Serial-Clock Output, PECL, 622.08MHz. SDO- is clocked out on the falling edge of SCLKO-.
11	SCLKO+	Positive Serial-Clock Output, PECL, 622.08MHz. SDO+ is clocked out on the rising edge of SCLKO+.
13	SDO-	Negative Serial-Data Output, PECL, 622.08Mbps
14	SDO+	Positive Serial-Data Output, PECL, 622.08Mbps
17	$\overline{LOL}$	Loss-of-Lock Output, TTL. PLL loss-of-lock monitor, active low (see *Design Procedure*).
19	PHADJ-	Negative Phase-Adjust Input. Used to optimally align internal PLL phase. Attach to V_{CC} if not used.
20	PHADJ+	Positive Phase-Adjust Input. Used to optimally align internal PLL phase. Attach to V_{CC} if not used.
22	FIL-	Negative Filter Input. PLL loop filter connection.
23	FIL+	Positive Filter Input. PLL loop filter connection.
26	DDI+	Positive Digital Data Input, PECL, 622.08Mbps serial-data stream
27	DDI-	Negative Digital Data Input, PECL, 622.08Mbps serial-data stream
28	INSEL	Input Select. Connect to GND to select digital data inputs or V_{CC} for analog data inputs.
29	ADI-	Negative Analog Data Input, 622.08Mbps serial-data stream
30	ADI+	Positive Analog Data Input, 622.08Mbps serial-data stream
32	CFILT	RSSI Filter Capacitor Input

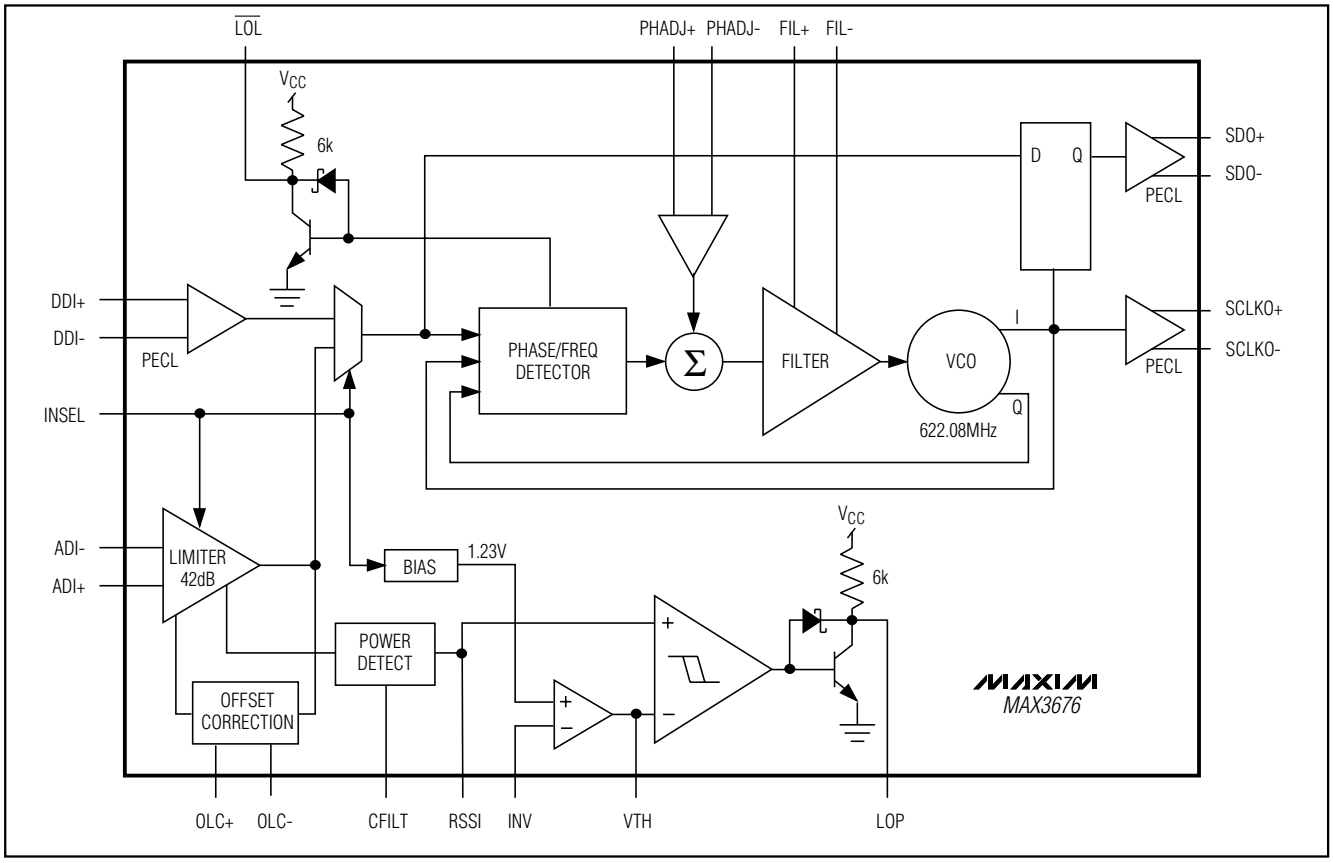


Figure 1. Functional Diagram

Detailed Description

The block diagram in Figure 1 shows the MAX3676's architecture. It consists of a limiting-amplifier input stage followed by a fully integrated clock/data-recovery (CDR) block implemented with a PLL. The input stage is selectable between a limiting amplifier or a simple PECL input buffer. The limiting amplifier provides an LOP monitor and an RSSI output. The PLL consists of a phase/frequency detector (PFD), a loop filter amplifier, and a voltage-controlled oscillator (VCO).

Limiting Amplifier

The MAX3676's on-chip limiting amplifier accepts an input signal level from 3.0mVp-p to 1.2Vp-p. The amplifier consists of a cascade of gain stages that include full-wave logarithmic detectors. The combined small-signal gain is approximately 42dB, and the -3dB bandwidth is 650MHz. Input-referred noise is typically $80\mu V_{RMS}$, providing excellent sensitivity for small-amplitude data streams.

In addition to driving the CDR, the limiting amplifier provides both an RSSI output and an LOP monitor that allow the user to program the threshold voltage. The RSSI circuitry provides an output voltage that is linearly proportional to the input power (in decibels) detected between the ADI+ and ADI- input pins and is sensitive enough to reliably detect signals as small as 2mVp-p (see *Typical Operating Characteristics*).

Input DC offset reduces the accuracy of the power detector; therefore, an integrated feedback loop is included that automatically nulls the input offset of the gain stage. The addition of this offset-correction loop requires that the input signal be AC-coupled when using the ADI+ and ADI- inputs.

Finally, for applications that do not require the limiting amplifier, selecting the digital inputs conserves power by turning off the postamplifier block.

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Phase Detector

The phase detector produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the incoming data. The external phase adjustment pins (PHADJ+, PHADJ-) allow the user to vary the internal phase alignment.

Frequency Detector

The frequency detector incorporated into the PLL uses the input data stream edges to sample the quadrature components of the VCO clock. This generates a difference frequency that aids acquisition during start-up. Depending on the polarity of the difference frequency, the PFD drives the VCO so that the difference frequency is reduced to zero. Once frequency acquisition is obtained, the frequency detector returns to a neutral state.

Loop Filter and VCO

The VCO is fully integrated, while the loop filter requires an external R-C network. This filter network determines the bandwidth and peaking of the second-order PLL.

Design Procedure

Received-Signal-Strength Indicator

The RSSI output voltage is insensitive to temperature and supply fluctuations. The power detector functions as a broadband power meter that detects the total RMS power of all signals within the detector bandwidth (including input signal noise). The RSSI voltage varies linearly (in decibels) for inputs of 2mVp-p to 50mVp-p. The slope over this input range is approximately 26mV/dB.

The high-speed RSSI signal is filtered to an RMS level with one external capacitor tied from CFILT to V_{CC}. The impedance looking into CFILT is about 500Ω to V_{CC}. As a result, the lower -3dB cutoff frequency is set by the following simple relationship:

$$f_{FILT} = 1 / \left[2\pi(500)C_F\right]$$

For 622Mbps applications, Maxim recommends a cutoff frequency of 6.8kHz, which requires C_F = 47nF. The RSSI output is designed to drive a minimum load resistance of 100kΩ to ground and a maximum of 20pF. Loads greater than 20pF must be buffered by a series resistance of 100kΩ (i.e., voltmeter).

Input Offset Correction

The on-chip limiting amplifier provides more than 42dB of gain. A low-frequency feedback loop is integrated into the MAX3676 to remove the input offset. DC-coupling to the ADI+ and ADI- inputs is not allowed, as this would prevent the proper functioning of the DC offset-correction circuitry.

The differential input impedance (Z_{IN}) is approximately 2.5kΩ. The impedance between OLC+ and OLC- (Z_{OLC}) is approximately 120kΩ. Take care when setting the combined low-frequency cutoff (f_{CUTOFF}), due to the input DC-blocking capacitor (C_{IN}) and the offset correction loop capacitor (C_{OLC}). See Table 1 for selecting the values of C_{IN} and C_{OLC}.

These values ensure that the poles associated with C_{IN} and C_{OLC} work together to provide a flat response at the lower -3dB corner frequency (no gain peaking).

C_{IN} must be a low-TC, high-quality capacitor of type X7R or better in order to minimize f_{CUTOFF} deviations. C_{OLC} must be a capacitor of type Z5U or better.

Loss-of-Power Monitor

An LOP monitor with a user-programmable threshold and a hysteresis comparator is also included with the limiting amplifier circuitry. Internally, one comparator input is tied to the RSSI output signal, and the other is tied to the threshold voltage (V_{TH}), which is set externally and provides a trip point for the LOP indication. A low-voltage, low-drift op amp, referenced to an internal bandgap voltage (1.23V), is supplied for programming a supply independent threshold voltage. This op amp requires two external resistors to program the LOP trip point. V_{TH} is programmable from 1.23V to 2.6V using the equation:

$$V_{TH} = 1.23(1 + R2 / R1)$$

The op amp can source only 100µA of current. Therefore, an R1 value of 20kΩ is recommended for proper operation. The input bias current of the op amp at the INV pin is less than ±100nA.

Table 1. Setting the Low-Frequency Cutoff

C_{IN}	C_{OLC}	COMBINED LOW f_{CUTOFF} (kHz)
0.022µF	0.15µF	3.0
0.010µF	0.1µF	6.8
6800pF	0.082µF	10
4700pF	0.033µF	13.5
2200pF	0.015µF	29
1000pF	0.01µF	68
470pF	3300pF	135
330pF	2200pF	190
220pF	1500pF	290

The comparator is configured with an active-high LOP output. An on-chip, 6kΩ pull-up resistor is provided to reduce the external part count.

Setting the Loop Filter

The MAX3676 is designed for both regenerator and receiver applications. Its fully integrated PLL is a classic second-order feedback system, with a loop bandwidth (f_L) fixed at 250kHz. The external capacitor, C_F, can be adjusted to set the loop damping. Figures 2 and 3 show the open-loop and closed-loop transfer functions. The PLL zero frequency, f_Z, is a function of external capacitor C_F, and can be approximated according to:

$$f_Z = \frac{1}{2\pi(90)\ C_F}$$

For an overdamped system (f_Z/f_L) <0.25, the jitter peaking (M_P) of a second-order system can be approximated by:

$$M_P = 20\log\left(1+\frac{f_Z}{f_L}\right)$$

For example, using C_F = 0.22µF results in a jitter peaking of 0.27dB. Reducing C_F below 0.22µF may result in PLL instability. The recommended value for C_F is 2.2µF to guarantee a maximum jitter peaking of less than 0.1dB.

The MAX3676 is optimally designed to acquire lock and to provide a bit-error rate (BER) of less than 10^{-10} for long strings of consecutive zeros and ones. Measured results show that the MAX3676 can tolerate 1200 consecutive ones or zeros. Decreasing C_F reduces the number of tolerated consecutive identical zeros and ones. C_F must be a low-TC, high-quality capacitor of type X7R or better.

Lock Detect

The MAX3676's LOL monitor indicates when the PLL is locked. Under normal operation, the loop is locked and the $\overline{LOL}$ output signal is high. When the MAX3676 loses lock, a fast negative-edge transition occurs on $\overline{LOL}$. The output level remains at a low level (held by C_{LOL}) until the loop reacquires lock (Figure 4).

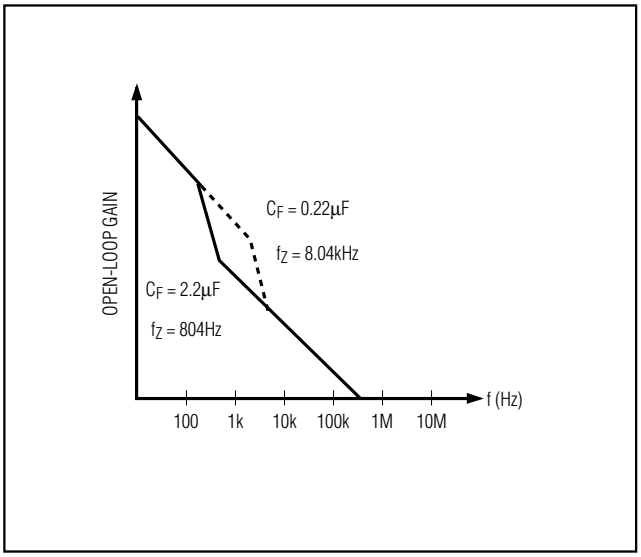


Figure 2. Open-Loop Transfer Function

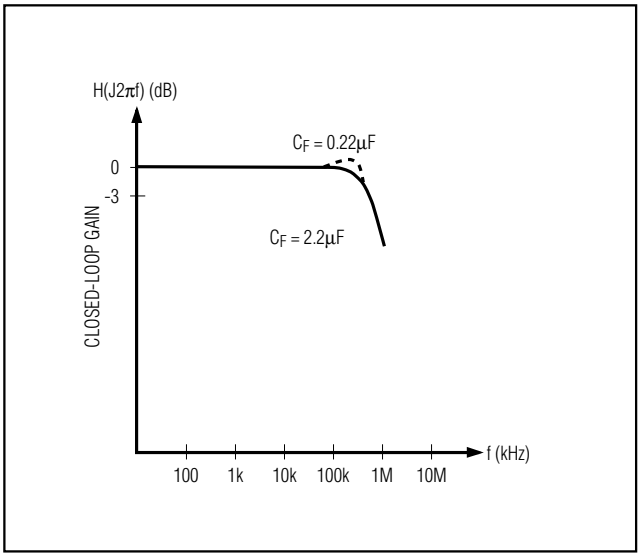


Figure 3. Closed-Loop Transfer Function

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Note that the LOL monitor is only valid when a data stream is present on the inputs to the MAX3676. As a result, LOL does not detect a loss-of-power condition resulting from a loss of the incoming signal. See the *Loss-of-Power Monitor* section for this type of indicator.

Input and Output Terminations

The MAX3676 digital data and clock I/Os (DDI+, DDI-, SDO+, SDO-, SCLK+, and SCLK-) are designed to interface with PECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thevenin equivalent of 50Ω to V_{CC} - 2V should be used with fixed-impedance transmission lines for proper termination. Make sure that the differential outputs have balanced loads.

The digital data input signals (DDI+ and DDI-) are differential inputs to an emitter-coupled pair. As a result, the MAX3676 can accept differential input signals as low as 250mV. These inputs can also be driven single-ended by externally biasing DDI- to the center of the voltage swing.

The MAX3676's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. Power-supply decoupling should be placed as close to V_{CC} as possible. Take care to isolate the input from the output signals to reduce feedthrough.

Applications Information

Driving the Limiting Amplifier Single-Ended

There are three important requirements for driving the limiting amplifier from a single-ended source (Figure 5):

1) There must be no DC-coupling to the ADI+ and ADI- inputs. DC levels at these inputs disrupt the offset-correction loop.
2) The terminating resistor R_T (50Ω) must be referenced to the ADI- input to minimize common-mode coupling problems.
3) The low-frequency cutoff for the limiting amplifier is determined by either C_{IN} and the 2.5kΩ input impedance or $C_b/2$ together with R_T. With C_b = 0.22µF and R_T = 50Ω, the low-frequency cutoff is 29kHz.

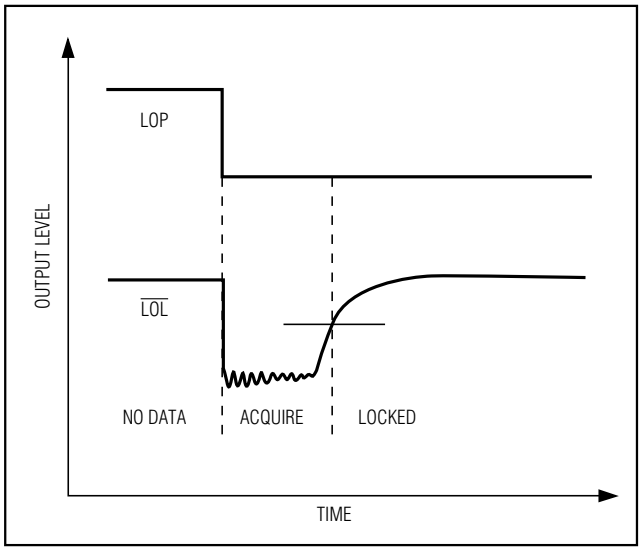


Figure 4. Loss-of-Lock Output

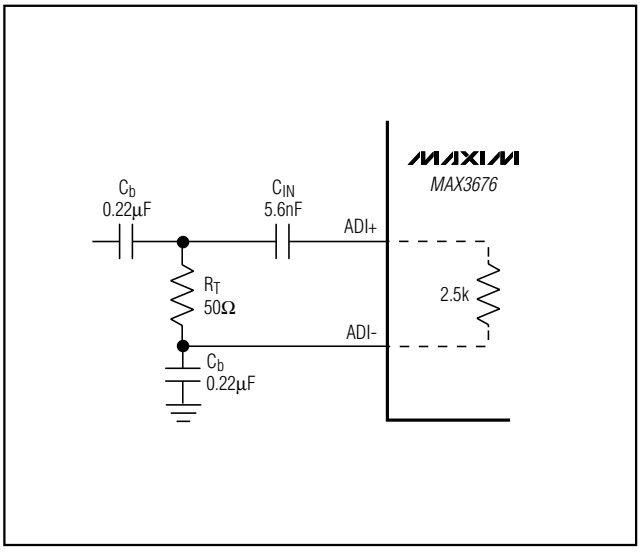


Figure 5. Single-Ended Input Termination

Reduced Power Consumption Without the Limiting Amplifier

The limiting amplifier is biased independently from the clock recovery circuitry. Grounding INSEL turns off the limiting amplifier and selects the PECL DDI inputs.

Converting Average Optical Power to Signal Amplitude

Many of the MAX3676's specifications relate to input-signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations given in Table 2 and Figure 6 are helpful for converting optical power to input signal when designing with the MAX3676.

In an optical receiver, the input voltage to the limiting amplifier can be found by multiplying the relationship in Table 2 by the photodiode responsivity and transimpedance amplifier gain.

Optical Hysteresis

Power and hysteresis are often expressed in decibels. By definition, decibels are always 10log (power). At the inputs to the MAX3676 limiting amplifier, the power is V_{IN}^2/R. If a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage at the input to the MAX3676 also increases by a factor of two.

The optical power increase is:

$$10\log(2x/x) = 10\log(2) = +3\text{dB}$$

At the MAX3676, the voltage increase is:

$$10\log\frac{(2V_{IN})^2/R}{V_{IN}^2/R} = 10\log(2^2) = 20\log(2) = +6\text{dB}$$

Table 2. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVG}	$P_{AVG} = (P0 + P1)/2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVG}\frac{r_e}{r_e+1}$
Optical Power of a "0"	P0	$P0 = 2P_{AVG}/(r_e+1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVG}\frac{(r_e-1)}{r_e+1}$

Assuming a 50% average input-data duty cycle

In an optical receiver, the decibel change at the MAX3676 always equals 2x the optical decibel change.

The MAX3676's typical voltage hysteresis is 3.0dB. This provides an optical hysteresis of 1.5dB.

Jitter in Optical Receivers

Timing jitter, edge speeds, aberrations, optical dispersion, and attenuation all impact the performance of high-speed clock recovery for SDH/SONET receivers (Figure 7). These effects decrease the time available for error-free data recovery by reducing the received "eye opening" of nonreturn-to-zero (NRZ) transmitted signals.

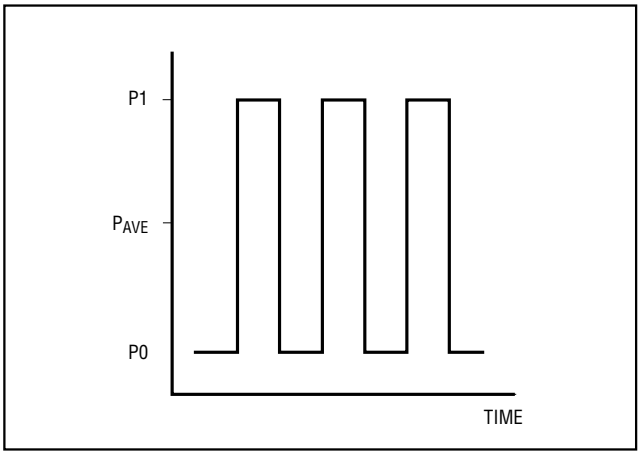


Figure 6. Optical Power Relations

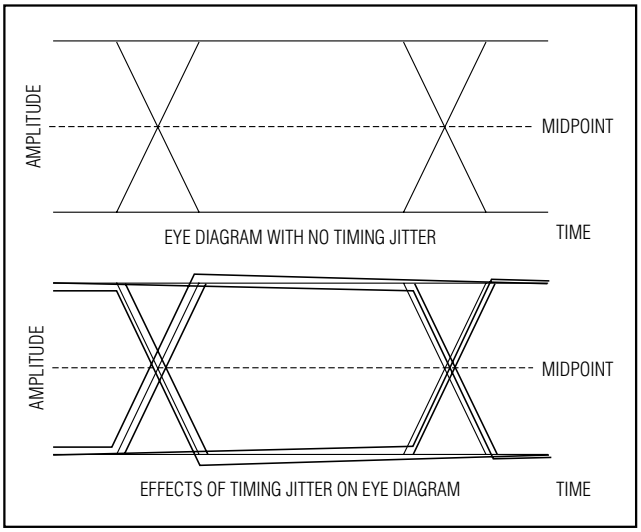


Figure 7. Eye Diagram With and Without Timing Jitter

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Optical receivers, incorporating transimpedance preamplifiers and limiting postamplifiers, can significantly clean up the effects of dispersion and attenuation. In addition, these amplifiers can provide fast transitions with minimal aberrations to the subsequent CDR blocks. However, these stages also add distortions to the midpoint crossing, contributing to timing jitter. Timing jitter is one of the most critical technical issues to consider when developing optical receivers and CDR circuits.

A better understanding of the different sources of jitter helps in the design and application of optical receiver modules and integrated CDR solutions. SDH/SONET specifications are well defined regarding the amount of jitter tolerance allowed at the inputs of optical receivers, as well as jitter peaking requirements, but they do little to define the different sources of jitter. The jitter that must be tolerated at an optical receiver input involves three significant sources, all of which are present in varying degrees in typical receiver systems:

1) Random jitter (RJ)
2) Pattern-dependent jitter (PDJ)
3) Pulse-width distortion (PWD)

Random Jitter

RJ is caused by random noise present during edge transitions (Figure 8). This random noise results in random midpoint crossings. All electrical systems generate some random noise; however, the faster the speed of the transitions, the lower the effect of noise on random jitter. The following equation is a simple worst-case estimation of random jitter:

$$RJ\ (rms) = (rms\ noise) / (slew\ rate)$$

Pattern-Dependent Jitter

PDJ results from wide variations in the number of consecutive bits contained in NRZ data streams working against the bandwidth requirements of the receiver (Figure 9). The location of the lower -3dB cutoff frequency is important, and must be set to pass the low frequencies associated with long consecutive bit streams. AC-coupling is common in optical receiver design.

When using a preamplifier with a highpass frequency response, select the input AC-coupling capacitor, C_{IN}, to provide a low-frequency cutoff (f_C) one decade lower than the preamplifier low-frequency cutoff. As a result, the PDJ is dominated by the low-frequency cutoff of the preamplifier.

When using a preamplifier without a highpass response with the MAX3676, the following equation provides a good starting point for choosing C_{IN}:

$$C_{IN} \geq \frac{-t_L}{(1.25k\Omega)\ln\left[1-\frac{(PDJ)(BW)}{0.5}\right]}$$

where t_L = duration of the longest run of consecutive bits of the same value (seconds); PDJ = maximum

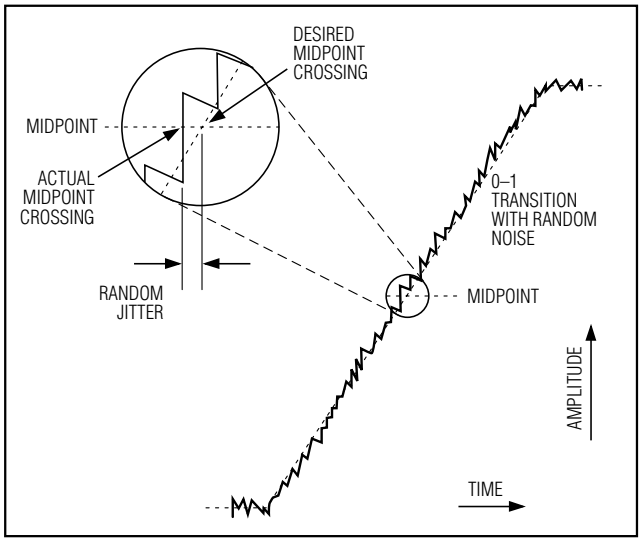


Figure 8. Random Jitter on Edge Transition

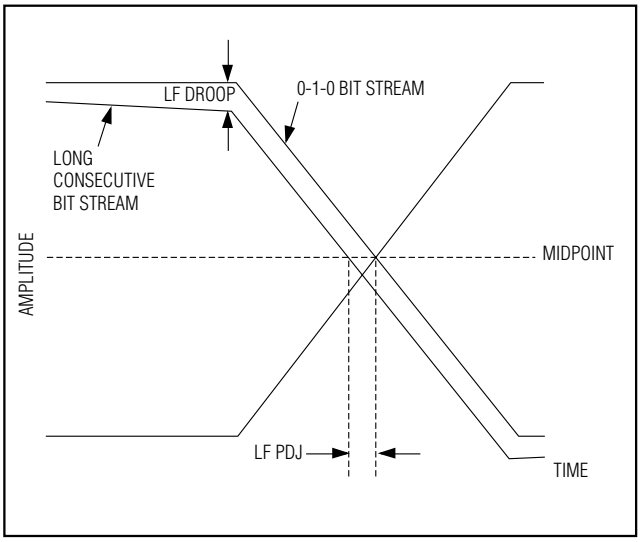


Figure 9. Pattern-Dependent Jitter Due to Low-Frequency Cutoff

allowable pattern-dependent jitter, peak-to-peak (seconds); and BW = typical system bandwidth, normally 0.6 to 1.0 times the data rate (Hertz). If the PDJ is still larger than desired, continue increasing the value of C_{IN}. Note that to maintain stability when using the MAX3676 analog inputs (ADI+, ADI-), it is important to keep the low-frequency cutoff associated with C_{OLC} below the corner frequency associated with C_{IN} (f_C) (Table 1).

PDJ can also be present due to insufficient high-frequency bandwidth (Figure 10). If the amplifiers are not fast enough to allow for complete transitions during single-bit patterns, or if the amplifier does not allow adequate settling time, high-frequency PDJ can result.

Pulse-Width Distortion

Finally, PWD occurs when the midpoint crossing of a 0–1 transition and a 1–0 transition does not occur at the same level (Figure 11). DC offsets and nonsymmetrical rising and falling edge speeds both contribute to PWD. For a 1–0 bit stream, calculate PWD as follows:

PWD = [(width of wider pulse) -
(width of narrower pulse)] / 2

Phase Adjust

The internal clock and data alignment in the MAX3676 is well maintained close to the center of the data eye. Although not required, this sampling point can be shifted using the PHADJ inputs to optimize BER performance. The PHADJ inputs operate with differential input signals to approximately ±1V. A simple resistor divider with a bypass capacitor is sufficient to set up these levels. When the PHADJ inputs are not used, they should be tied directly to V_{CC}.

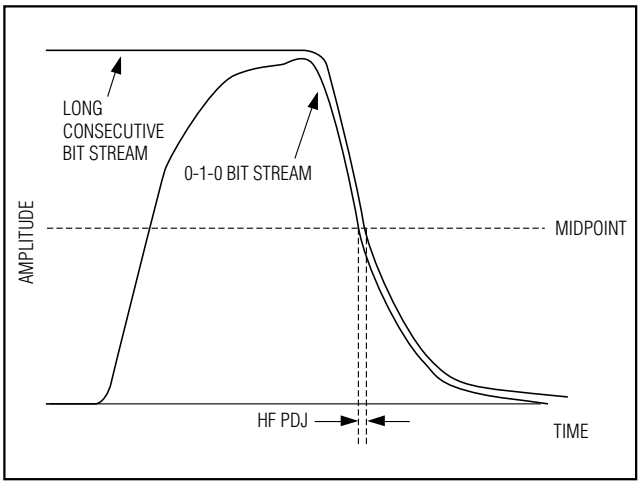


Figure 10. Pattern-Dependent Jitter Due to High-Frequency Rolloff

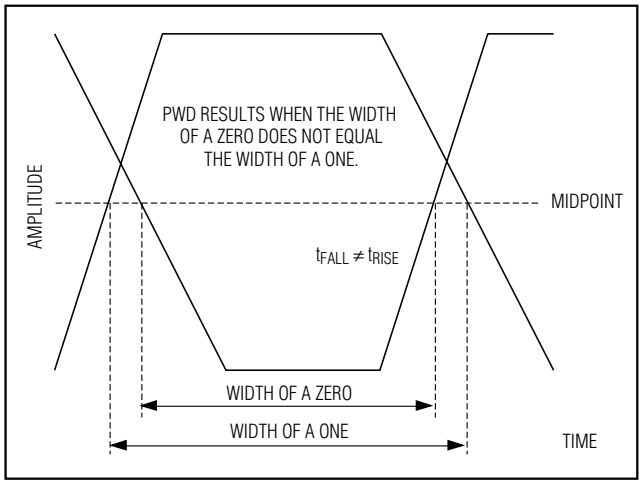
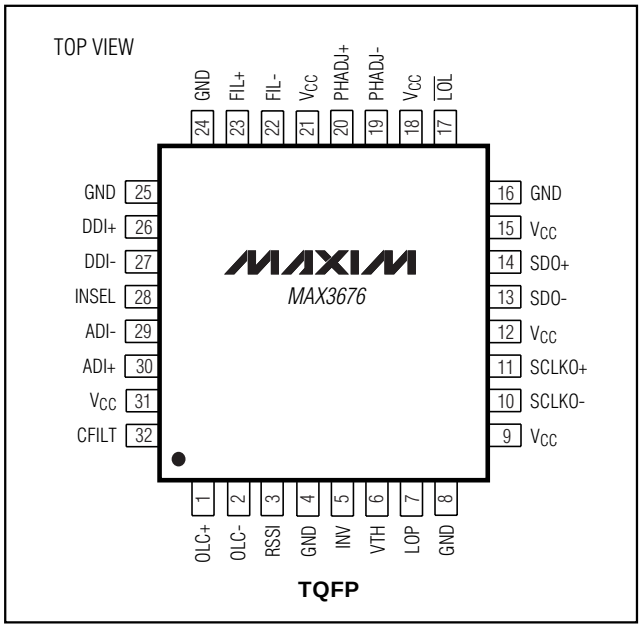


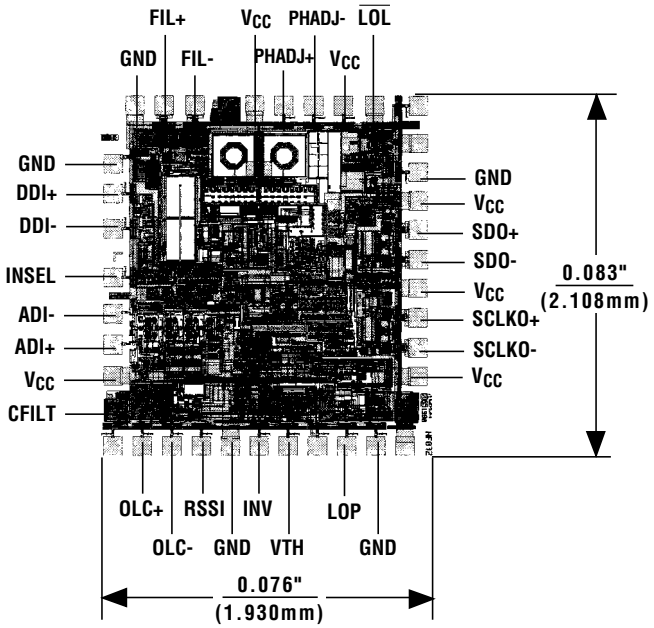
Figure 11. Pulse-Width Distortion

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Pin Configuration



Chip Topography

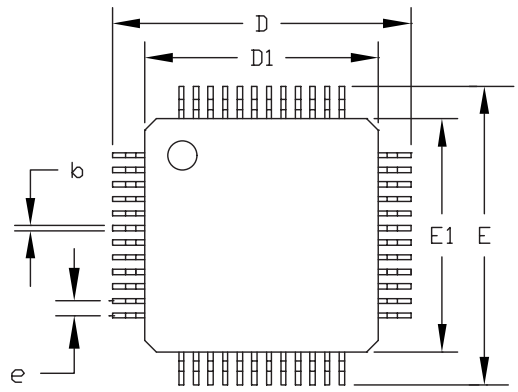


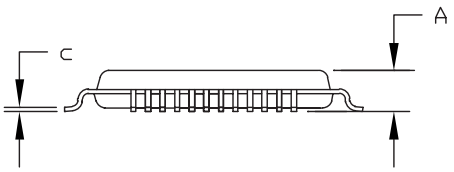
Chip Information

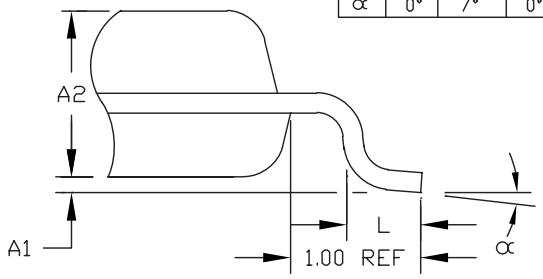
TRANSISTOR COUNT: 2528

Package Information

32L/48L,TQFP.EPS







JEDEC VARIATION				
	BC		BE	
	32 LEAD		48 LEAD	
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A_1	0.05	0.15	0.05	0.15
A_2	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D_1	7.00 BSC.		7.00 BSC.	
E	8.90	9.10	8.90	9.10
E_1	7.00 BSC.		7.00 BSC.	
e	0.8 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP			
APPROVAL	DOCUMENT CONTROL NO. 21-0054	REV D	1/1

622Mbps, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

NOTES