19-3181; Rev 0; 2/04

MAXIM

3.2Gbps SFP Transimpedance Amplifiers with RSSI

General Description

The MAX3724/MAX3725 transimpedance amplifiers provide a compact, low-power solution for communication up to 3.2Gbps. They feature 325nA input-referred noise at 2.1GHz bandwidth (BW) with 0.6pF input capacitance. The parts also have >2mA$_{P-P}$ AC input overload.

Both parts operate from a single +3.3V supply and consume 93mW. The MAX3724/MAX3725 are in a compact 30-mil x 50-mil die and require no external compensation capacitor. A space-saving filter connection is provided for positive bias to the photodiode through an on-chip 580Ω resistor to V_{CC}. These features allow easy assembly into a low-cost TO-46 or TO-56 header with a photodiode.

The MAX3724 and MAX3748A receiver chip set provides an RSSI output using a Maxim-proprietary* interface technique. The MAX3724 preamplifier, MAX3748A postamplifier, and the DS1858/DS1859 SFP controller meet all the SFF-8472 digital diagnostic requirements.

Applications

Up to 3.2Gbps SFF/SFP Optical Receivers

Optimized for Small-Form-Factor Pluggable (SFP) Optical Receivers

**Patent pending.*

Features

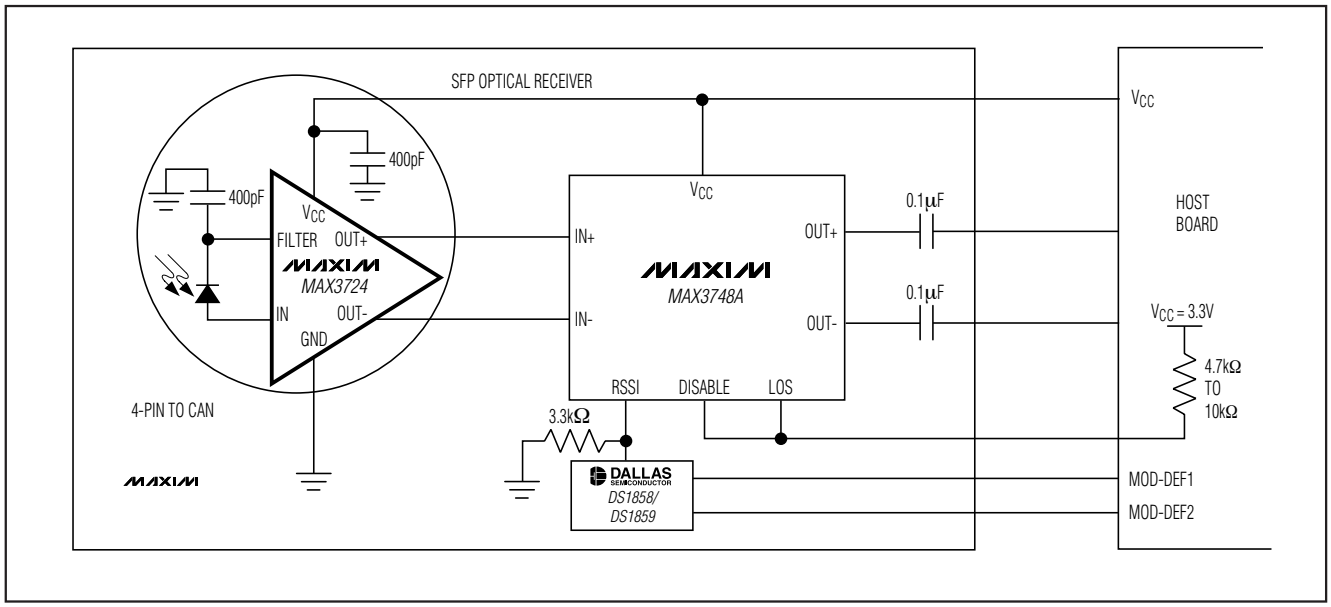
- **Wider Bandwidth than MAX3744/MAX3745**
- **RSSI Implementation in 4-Pin TO-46 Header (MAX3724 and MAX3748A)**
- **8ps$_{P-P}$ Deterministic Jitter for <100µA$_{P-P}$ Input Current**
- **325nA$_{RMS}$ Input-Referred Noise at 2.1GHz Bandwidth**
- **28mA Supply Current at +3.3V**
- **2.5GHz Small-Signal Bandwidth**
- **2.0mA$_{P-P}$ AC Overload**
- **Die Size: 30 mils x 50 mils (Identical to the MAX3744/MAX3745)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3724E/D	-40°C to +85°C	Dice**
MAX3725E/D	-40°C to +85°C	Dice**

***Dice are designed to operate with junction temperatures of -40°C to +110°C but are tested and guaranteed only at T_A = +25°C.*

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3.2Gbps SFP Transimpedance Amplifiers with RSSI

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}).....-0.5V to +6.0V
Continuous CML Output Current
(OUT+, OUT-) ..... -25mA to +25mA
Continuous Input Current (IN).....-4mA to +4mA
Continuous Input Current (FILTER).....-8mA to +8mA
Operating Junction Temperature Range (T_J)....-55°C to +150°C
Storage Ambient Temperature Range (T_{STG}) ...-55°C to +150°C
Die Attach Temperature.....+400°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V and T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, source capacitance (C_{IN}) = 0.85pF, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	Including CML output current (I_{IN} = 0)			28	41	mA
Input Bias Voltage						1.0	V
Input Overload		(Note 3)		2			mA_{P-P}
Input-Referred Noise (Note 4)	I_N	C_{IN} = 0.85pF, BW = 933MHz			200		nA_{RMS}
		C_{IN} = 0.85pF, BW = 2.1GHz (Note 3)			360	485	
		C_{IN} = 0.85pF, BW = 18GHz (Note 3)				700	
		C_{IN} = 0.6pF, BW = 933MHz			200		
		C_{IN} = 0.6pF, BW = 2.1GHz (Note 3)			325	440	
		C_{IN} = 0.6pF, BW = 18GHz (Note 3)				635	
Differential Transimpedance		Differential output, I_{IN} = $40\mu A_{AVE}$		2.8	3.5	4.5	kΩ
Small-Signal Bandwidth (Note 3)	BW	-3dB, C_{IN} = 0.6pF		2	2.5		GHz
		-3dB, C_{IN} = 0.85pF		1.8	2.3		
Low-Frequency Cutoff		-3dB, input current = $20\mu A_{AVE}$ (Note 3)				30	kHz
Deterministic Jitter (Notes 3, 5)	DJ	$100\mu A_{P-P}$ < input ≤ $2mA_{P-P}$	2.1Gbps, K28.5 pattern		11	33	ps_{P-P}
			2.7Gbps, 2^{31} - 1 pattern		15		
		$10\mu A_{P-P}$ < input ≤ $100\mu A_{P-P}$	2.1Gbps, K28.5 pattern		8	17	
			2.7Gbps, 2^{31} - 1 pattern		12		
Filter Resistance				510	580	690	Ω
Differential Output Resistance (OUT+, OUT-)				85	100	115	Ω
Maximum Differential Output Voltage	V_{OD}	Input > $50\mu A_{AVE}$, output termination 50Ω to V_{CC} (output in limited state)		220	280	400	mV_{P-P}

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V and T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, source capacitance (C_{IN}) = 0.85pF, and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Single-Ended Output Common-Mode Minimum Level (MAX3724)		Relative to V_{CC}, I_{IN} = 1mA$_{AVE}$		540	490		mV
Output Data Transition Time		Input > 200µA$_{P-P}$ 20% to 80% rise/fall time (Note 3)			70	100	ps
Differential Output Return Loss		Frequency ≤ 1GHz			17		dB
		1GHz < frequency ≤ 2GHz			10		
Power-Supply Noise Rejection	PSNR	I_{IN} = 0 (Note 6)	f < 1MHz		46		dB
			1MHz ≤ f < 10MHz		34		
RSSI Gain (MAX3724)	A_{RSSI}	(Note 7)			21		A/A
RSSI Gain Stability (MAX3724)		10log($A_{RSSI}/A_{RSSI-NOM}$) where $A_{RSSI-NOM}$ = A_{RSSI} at 3.3V, +25°C (Note 3)				0.24	dB

Note 1: Dice are designed to operate with junction temperatures of -40°C to +110°C but are tested and guaranteed only at T_A = 25°C.

Note 2: Source capacitance represents the total capacitance at the IN pad during characterization of the noise and bandwidth parameters.

Note 3: Guaranteed by design and characterization.

Note 4: Input-referred noise is:

$$\left(\frac{\text{RMS output noise}}{\text{Gain at f = 100MHz}}\right)$$

Note 5: Deterministic jitter is the sum of pulse-width distortion (PWD) and pattern-dependent jitter (PDJ).

Note 6: Power-supply noise rejection PSNR = -20log(ΔV_{OUT} / ΔV_{CC}), where ΔV_{OUT} is the differential output voltage and ΔV_{CC} is the noise on V_{CC}.

Note 7:

$$A_{RSSI} = \frac{I_{OUT\_CM}(I_{IN} = 400\mu A) - I_{OUT\_CM}(I_{IN} = 0\mu A)}{400\mu A}$$

where $I_{OUT\_CM} = \frac{I_{OUT+} + I_{OUT-}}{2}$

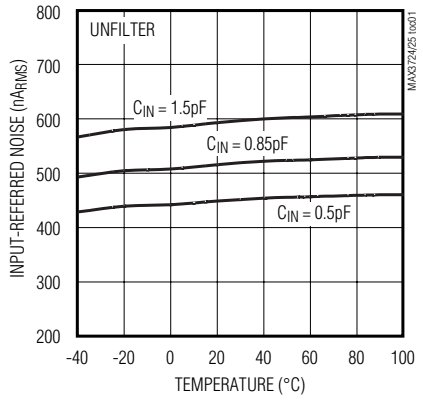
RSSI range is from I_{IN} = 6µA to 500µA

3.2Gbps SFP Transimpedance Amplifiers with RSSI

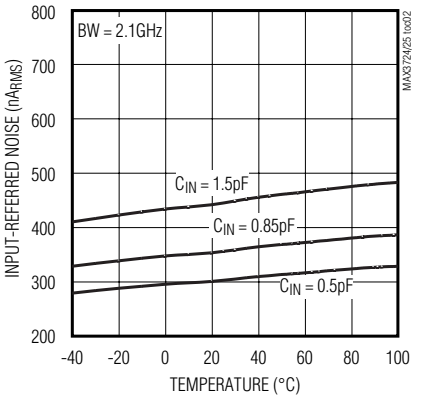
Typical Operating Characteristics

(V_{CC} = +3.3V, C_{IN} = 0.85pF, T_A = +25°C, unless otherwise noted.)

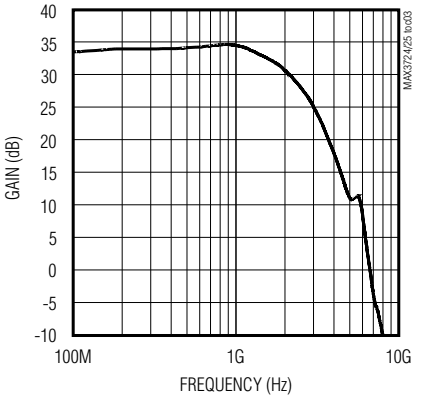
INPUT-REFERRED NOISE vs. TEMPERATURE



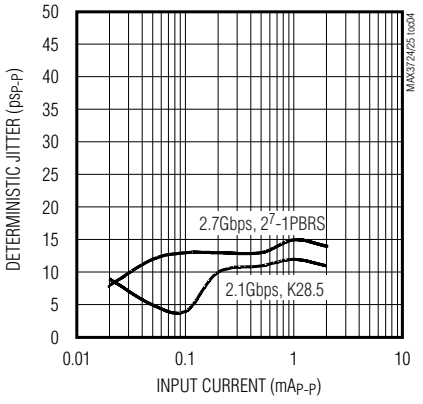
INPUT-REFERRED NOISE vs. TEMPERATURE



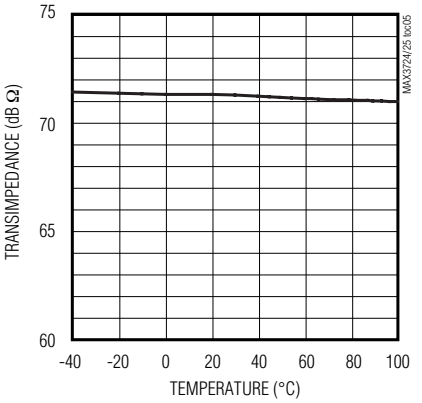
OPTICAL FREQUENCY RESPONSE (70µm InGaAS PHOTODIODE, INPUT -22dBm)



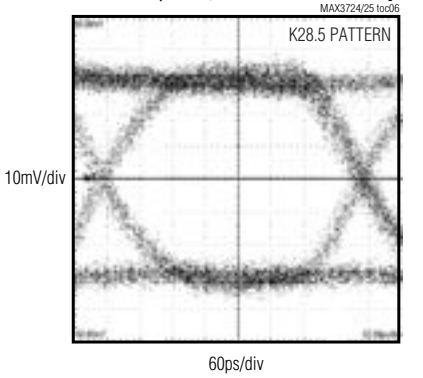
DETERMINISTIC JITTER vs. INPUT VOLTAGE



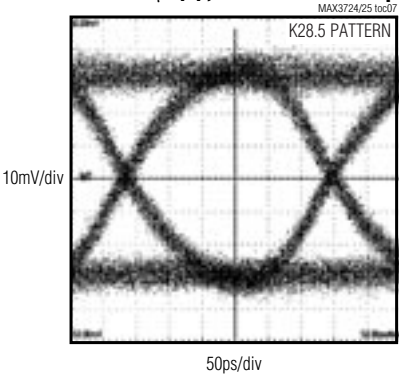
SMALL-SIGNAL TRANSIMPEDANCE vs. TEMPERATURE



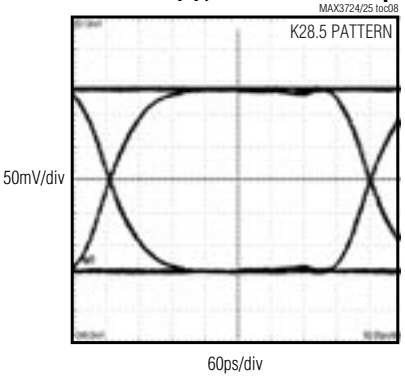
EYE DIAGRAM INPUT = 20µAP-P, DATA RATE = 2.1Gbps



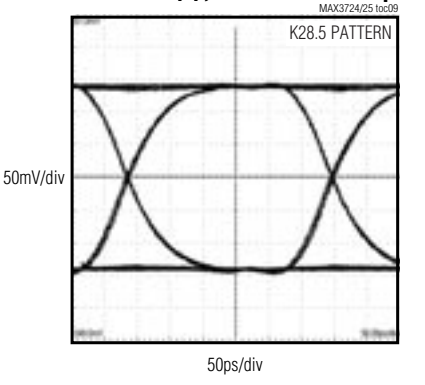
EYE DIAGRAM INPUT = 20µAP-P, DATA RATE = 3.2Gbps



EYE DIAGRAM INPUT = 2mAP-P, DATA RATE = 2.1Gbps



EYE DIAGRAM INPUT = 2mAP-P, DATA RATE = 3.2Gbps

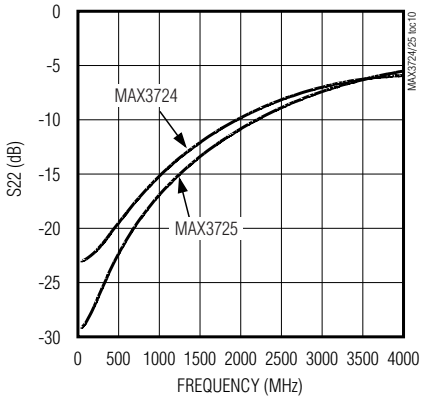


3.2Gbps SFP Transimpedance Amplifiers with RSSI

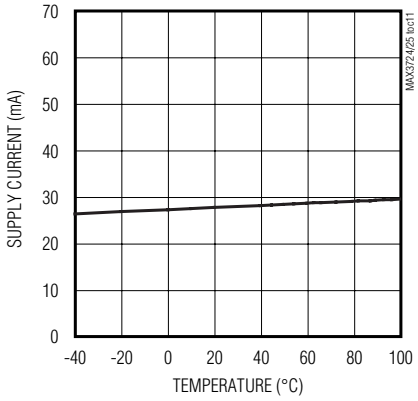
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, C_{IN} = 0.85pF, T_A = +25°C, unless otherwise noted.)

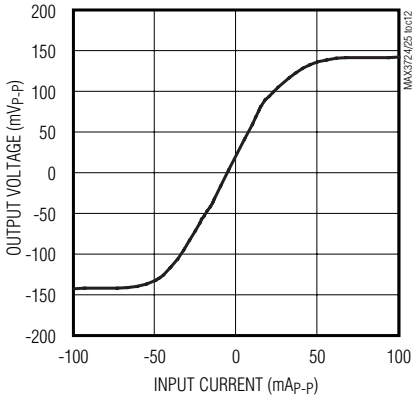
DIFFERENTIAL S22 vs. FREQUENCY



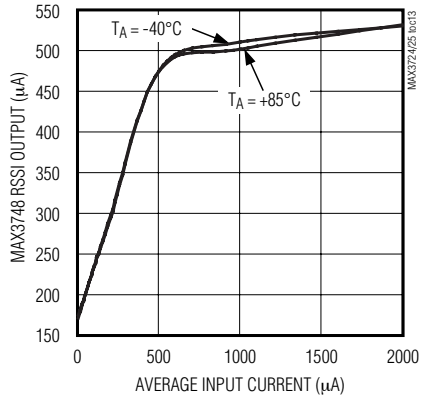
SUPPLY CURRENT vs. TEMPERATURE



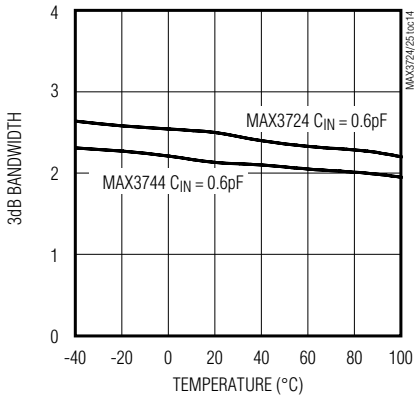
DC TRANSFER FUNCTION (V_{FILT} = 0V)



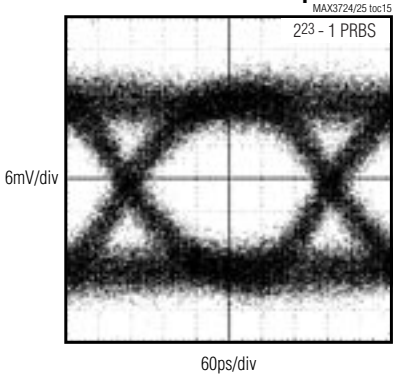
RSSI MAX3724, MAX3748A



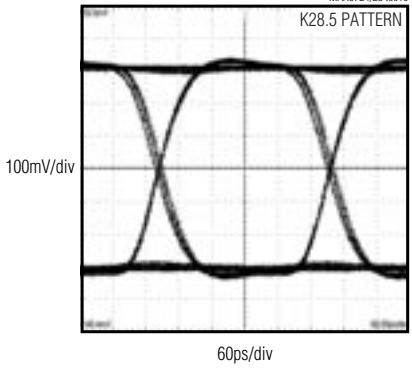
BANDWIDTH vs. TEMPERATURE



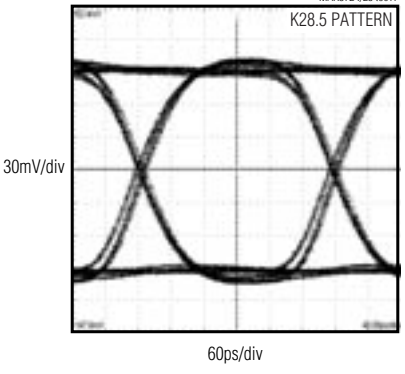
EYE DIAGRAM TEMPERATURE = +100°C INPUT = 20µAP-P DATA RATE = 2.7Gbps



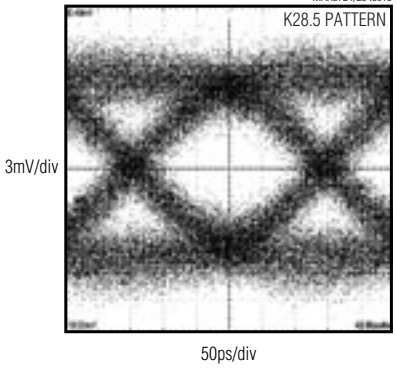
OPTICAL EYE DIAGRAM INPUT = 0dBm, DATA RATE = 3.2Gbps



OPTICAL EYE DIAGRAM INPUT = 0dBm, DATA RATE = 4.25Gbps



OPTICAL EYE DIAGRAM INPUT = -18dBm, DATA RATE = 4.25Gbps



3.2Gbps SFP Transimpedance Amplifiers with RSSI

Pin Description

MAX3724/ MAX3725 BOND PAD	NAME	FUNCTION
1, 3	V_{CC}	Supply Voltage
2, 7	N.C.	No Connection
4	IN	TIA Input. Signal current from photodiode flows into this pin.
5	FILTER	Provides bias voltage for the photodiode through a 580Ω resistor to V_{CC}. When grounded, this pin disables the DC cancellation amplifier to allow a DC path from IN to OUT+ and OUT- for testing.
6, 10	GND	Supply Ground
8	OUT-	Inverting Data Output. Current flowing into IN causes the voltage at OUT- to decrease. For the MAX3724, the common mode between OUT+ and OUT- is proportional to the average input current.
9	OUT+	Noninverting Data Output. Current flowing into IN causes the voltage at OUT+ to increase. For the MAX3724, the common mode between OUT+ and OUT- is proportional to the average input current.

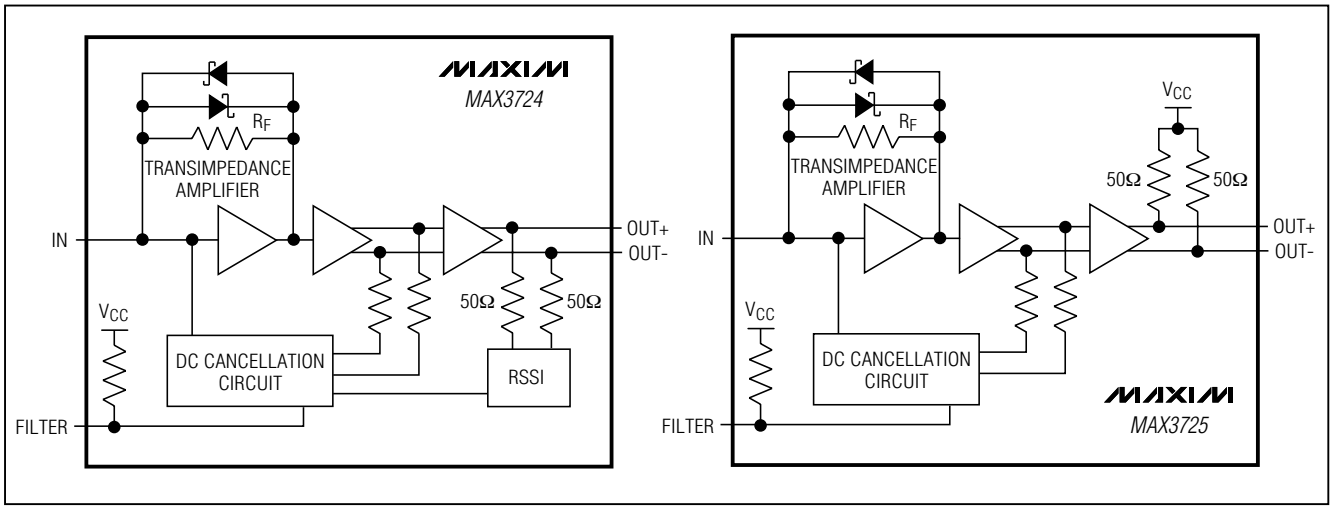


Figure 1. Functional Diagram

Detailed Description

The MAX3724/MAX3725 are transimpedance amplifiers designed for up to 3.2Gbps SFF/SFP transceiver modules. A functional diagram of the MAX3724/MAX3725 is shown in Figure 1. The MAX3724/MAX3725 comprise a transimpedance amplifier stage, a voltage amplifier stage, an output buffer, and a direct-current (DC) feedback cancellation circuit. The MAX3724 also includes a signal strength indicator (RSSI). To provide this signal in a standard 4-pin TO header, the RSSI level is added to the common mode of the differential data output pins.

Transimpedance Amplifier Stage

The signal current at the input flows into the summing node of a high-gain amplifier. Shunt feedback through the resistor R_F converts this current to a voltage. In parallel with the feedback resistor are two back-to-back Schottky diodes that clamp the output signal for large input currents, as shown in Figure 2.

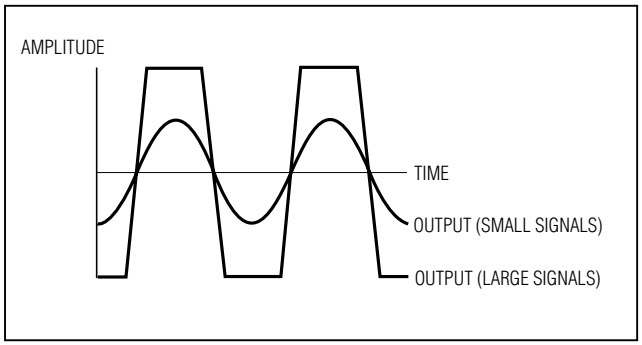


Figure 2. MAX3724/MAX3725 Limited Output

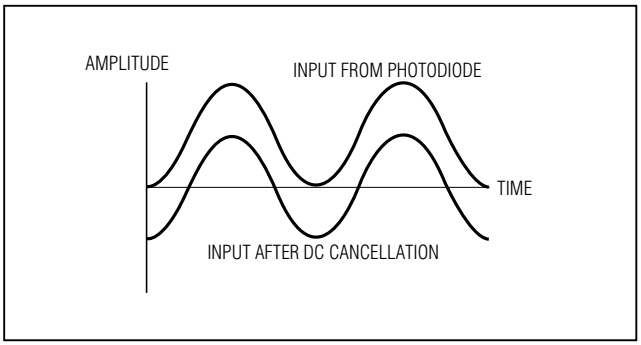


Figure 3. DC Cancellation Effect on Input

Voltage Amplifier Stage

The voltage amplifier stage provides gain and converts the single-ended input to differential outputs.

DC Cancellation Circuit

The DC cancellation circuit uses low-frequency feedback to remove the DC component of the input signal (Figure 3). This feature centers the input signal within the transimpedance amplifier's linear range, thereby reducing pulse-width distortion caused by large input signals. The DC cancellation circuit is internally compensated and therefore does not require external capacitors.

Output Buffer

The output buffer provides a reverse-terminated voltage output. The buffer is designed to drive a 100Ω differential load between OUT+ and OUT-. The MAX3724 must be DC-coupled to the MAX3748A. See Figures 4 and 5.

For optimum supply-noise rejection, the MAX3725 should be terminated with a matched load. If a single-ended output is required, the unused output should be terminated to a 50Ω resistor to V_{CC}. The MAX3725 does not drive a DC-coupled, 50Ω grounded load; however, it does drive a compatible 50Ω CML input.

Signal-Strength Indicator

The MAX3724 produces a signal proportional to the average photodiode current. This is added to the common mode of the data outputs OUT+ and OUT-. This signal is intended for use with the MAX3748A to provide a ground-referenced RSSI voltage.

Applications Information

Signal-Strength Indicator

The SFF-8472 digital diagnostic specification requires monitoring of input receive power. The MAX3748A and MAX3724 receiver chipset allows for the monitoring of the average receive power by measuring the average DC current of the photodiode.

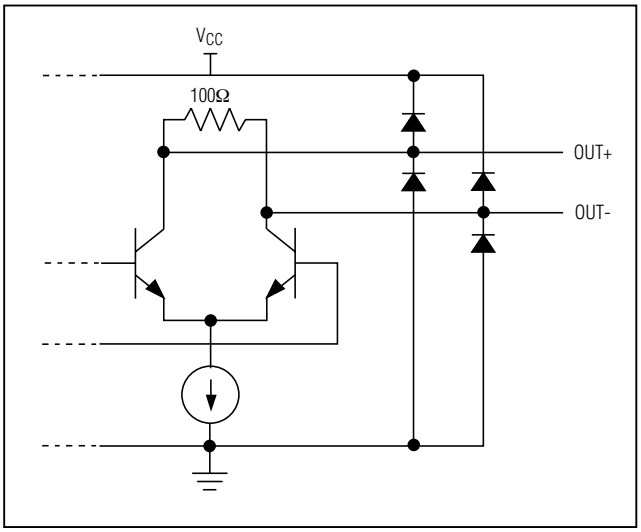


Figure 4. Equivalent Output MAX3724

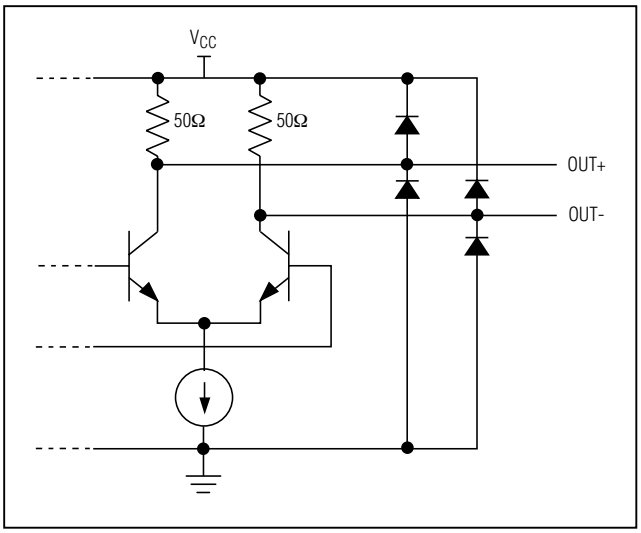


Figure 5. Equivalent Output MAX3725

3.2Gbps SFP Transimpedance Amplifiers with RSSI

The MAX3724 preamp measures the average photodiode current and provides the information to the output common mode. The MAX3748A RSSI detect block senses the common-mode DC level of input signals IN+ and IN- and provides a ground-level-referenced output signal of the photodiode current. The advantage of this implementation is that it allows the TIA to be packaged in a low-cost conventional 4-pin TO-46 header.

The MAX3748A RSSI output is connected to an analog input channel of the DS1858/DS1859 SFP controller to convert the analog information into a 16-bit word. The DS1858/DS1859 provide the received power information to the host board of the optical receiver through a 2-wire interface. The DS1859 allows for internal calibration of the receive power monitor.

The MAX3724 and the MAX3748A have been optimized to achieve RSSI stability of better than 2.5dB within the 6µA to 500µA range of average input photodiode current. To achieve the best accuracy, Maxim recommends receive power calibration to be 6µA at the low end, and 500µA at the high end of the required range.

Optical Power Relations

Many of the MAX3724/MAX3725 specifications relate to the input signal amplitude. When working with optical receivers, the input is sometimes expressed in terms of average optical power and extinction ratio. Figure 6 and Table 1 show relations that are helpful for converting optical power to input signal when designing with the MAX3724/MAX3725. (Refer to Application Note HFAN–3.0.0: *Accurately Estimating Optical Receiver Sensitivity*.)

Optical Sensitivity Calculation

The input-referred RMS noise current (I_N) of the MAX3724/MAX3725 generally determines the receiver sensitivity. To obtain a system bit-error rate (BER) of 1E-12, the signal-to-noise ratio must always exceed 14.1. The input sensitivity, expressed in average power, can be estimated as:

$$\text{Sensitivity} = 10\log\left(\frac{14.1 \times I_N(r_e + 1)}{2\rho(r_e - 1)}1000\right)\text{dBm}$$

where ρ is the photodiode responsivity in A/W and I_N is RMS current in amps.

Input Optical Overload

The overload is the largest input that the MAX3724/MAX3725 can accept while meeting deterministic jitter specifications. The optical overload can be estimated in terms of average power with the following equation:

$$\text{Overload} = 10\log\left(\frac{2mA_{RMS}(r_e + 1)}{2\rho(r_e - 1)}1000\right)\text{dBm}$$

Optical Linear Range

The MAX3724/MAX3725 have high gain, which limits the output when the input signal exceeds $50\mu A_{P-P}$. The MAX3724/MAX3725 operate in a linear range (10% linearity) for inputs not exceeding:

$$\text{Linear Range} = 10\log\left(\frac{50\mu A_{RMS}(r_e + 1)}{2\rho(r_e - 1)}1000\right)\text{dBm}$$

Table 1. Optical Power Relations

PARAMETER	SYMBOL	RELATION
Average power	P_{AVG}	$P_{AVG} = (P_0 + P_1) / 2$
Extinction ratio	r_e	$r_e = P_1 / P_0$
Optical power of a 1	P_1	$P_1 = 2P_{AVG}(r_e) / (r_e + 1)$
Optical power of a zero	P_0	$P_0 = 2P_{AVG} / (r_e + 1)$
Signal amplitude	P_{IN}	$P_{IN} = P_1 - P_0$; $P_{IN} = 2P_{AVG}(r_e - 1) / (r_e + 1)$

Note: *Assuming 50% average duty cycle and mark density.*

Layout Considerations

Noise performance and bandwidth are adversely affected by capacitance at the IN pad. Minimize capacitance on this pad and select a low-capacitance photodiode. Assembling the MAX3724/MAX3725 in die form using chip and wire technology provides the best possible performance. Figure 7 shows a suggested layout for a TO header for the MAX3724/MAX3725. The placement of the filter cap to minimize the ground loop of the photodiode is required to achieve the specified bandwidth. The OUT+ and OUT- bond wire lengths should also be minimized to meet the bandwidth specification. Special care should be taken to ensure that ESD at IN does not exceed 500V.

Photodiode Filter

Supply voltage noise at the cathode of the photodiode produces a current $I = C_{PD}\ \Delta V/\Delta t$, which reduces the receiver sensitivity (C_{PD} is the photodiode capacitance.) The filter resistor of the MAX3724/MAX3725, combined with an external capacitor, can be used to reduce this noise (see the *Typical Application Circuit*). Current generated by supply noise voltage is divided between C_{FILTER} and C_{PD}. The input noise current due to supply noise is (assuming the filter capacitor is much larger than the photodiode capacitance):

$$I_{NOISE} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(C_{FILTER})$$

If the amount of tolerable noise is known, the filter capacitor can be easily selected:

$$C_{FILTER} = (V_{NOISE})(C_{PD}) / (R_{FILTER})(I_{NOISE})$$

For example, with maximum noise voltage = $100mV_{P-P}$, C_{PD} = 0.85pF, R_{FILTER} = 600Ω, and I_{NOISE} selected to be 350nA:

$$C_{FILTER} = (100mV)(0.85pF) / (600\Omega)(350nA) = 405pF$$

Wire Bonding

For high-current density and reliable operation, the MAX3724/MAX3725 use gold metalization. Connections to the die should be made with gold wire only, using ball-bonding techniques. Die thickness is typically 14 mils (0.4mm).

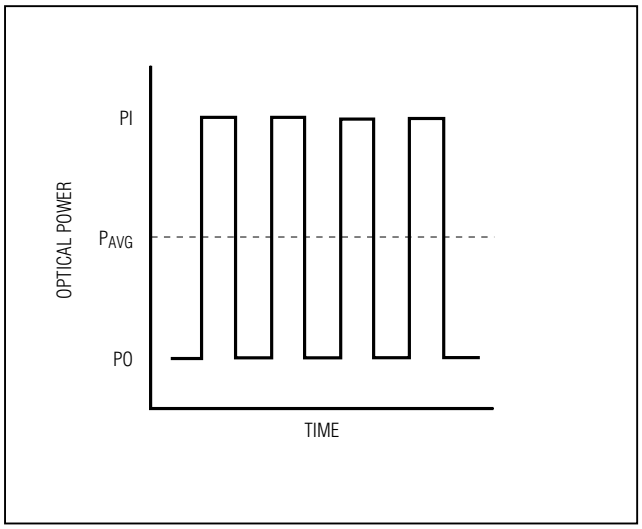


Figure 6. Optical Power Relations

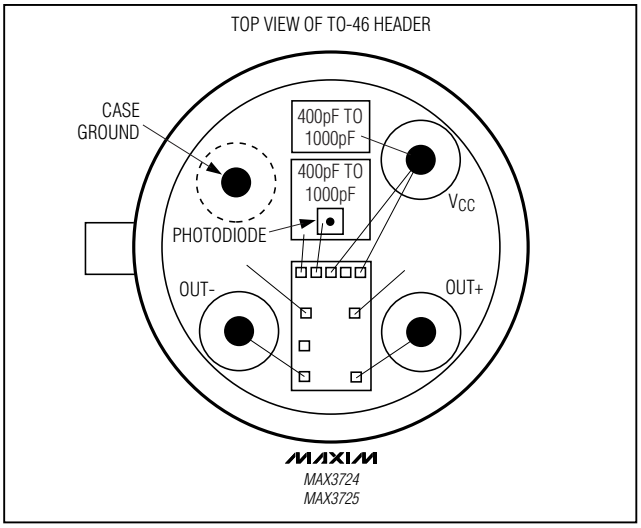
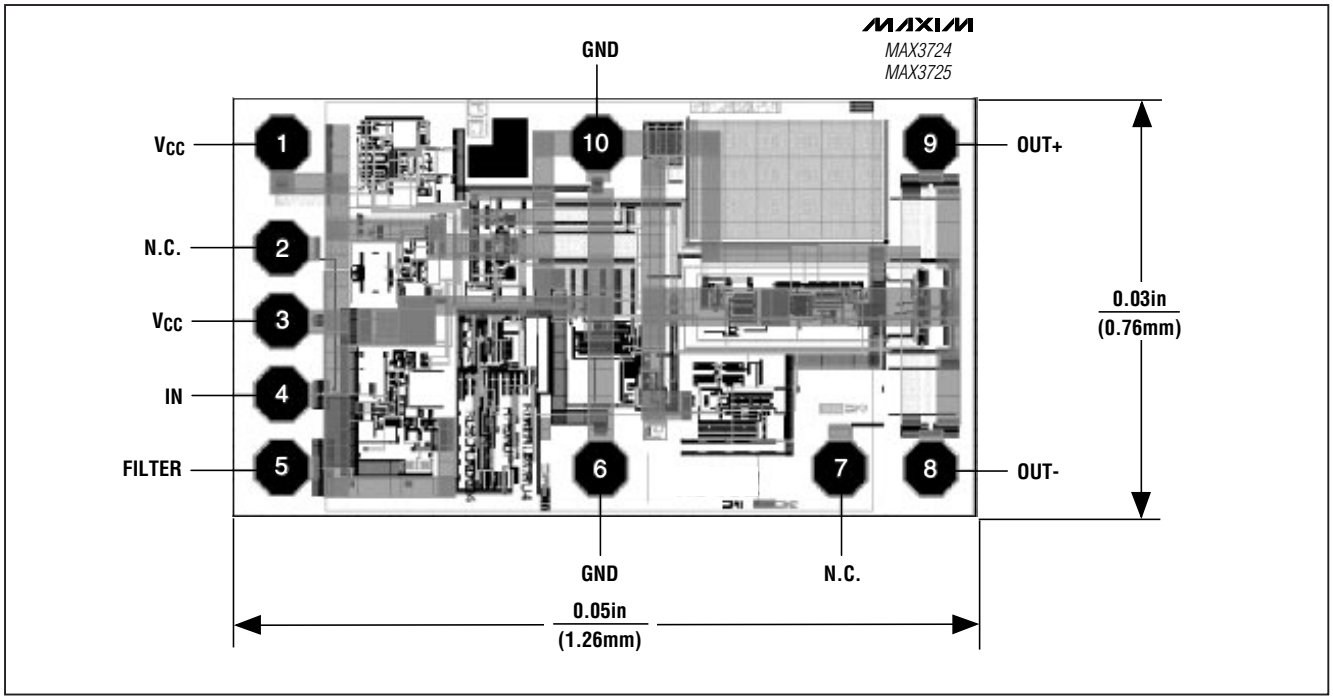


Figure 7. Suggested Layout for TO-46 Header

3.2Gbps SFP Transimpedance Amplifiers with RSSI

Chip Topography



Pad Coordinates

PAD	COORDINATES (µm) X	COORDINATES (µm) Y
1	1.4	495.6
2	0	336
3	0	224
4	0	112
5	0	0
6	494.2	-1.4
7	865.2	-1.4
8	1005.2	-1.4
9	1005.2	495.6
10	490	495.6

Chip Information

TRANSISTOR COUNT: 301

PROCESS: SiGe Bipolar

SUBSTRATE: ISOLATED

DIE THICKNESS: 0.014in ±0.001in

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