

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## General Description

The MAX5878 is an advanced 16-bit, 250Mps, dual digital-to-analog converter (DAC). This DAC meets the demanding performance requirements of signal synthesis applications found in wireless base stations and other communications applications. Operating from +3.3V and +1.8V supplies, this dual DAC offers exceptional dynamic performance such as 76dBc spurious-free dynamic range (SFDR) at  $f_{OUT} = 16\text{MHz}$  and supports update rates of 250Mps, with a power dissipation of only 296mW.

The MAX5878 utilizes a current-steering architecture that supports a 2mA to 20mA full-scale output current range, and allows a 0.1V<sub>P-P</sub> to 1V<sub>P-P</sub> differential output voltage swing. The device features an integrated +1.2V bandgap reference and control amplifier to ensure high-accuracy and low-noise performance. A separate reference input (REFIO) allows for the use of an external reference source for optimum flexibility and improved gain accuracy.

The clock inputs of the MAX5878 accept both LVDS and LVPECL-compatible voltage levels. The device features an interleaved data input that allows a single LVDS bus to support both DACs. The MAX5878 is available in a 68-pin QFN package with an exposed paddle (EP) and is specified for the extended temperature range (-40°C to +85°C).

Refer to the MAX5876\* and MAX5877\* data sheets for pin-compatible 12-bit and 14-bit versions of the MAX5878, respectively. Refer to the MAX5875 data sheet for a CMOS-compatible version of the MAX5878.

## Applications

Base Stations: Single/Multicarrier UMTS, CDMA, GSM  
Communications: Fixed Broadband Wireless Access,  
Point-to-Point Microwave  
Direct Digital Synthesis (DDS)  
Cable Modem Termination Systems (CMTS)  
Automated Test Equipment (ATE)  
Instrumentation

\*Future product—contact factory for availability.

## Selector Guide

PART	RESOLUTION (BITS)	UPDATE RATE	LOGIC INPUTS
MAX5873	12	200Mps	CMOS
MAX5874	14	200Mps	CMOS
MAX5875	16	200Mps	CMOS
MAX5876*	12	250Mps	LVDS
MAX5877*	14	250Mps	LVDS
MAX5878	16	250Mps	LVDS

## Features

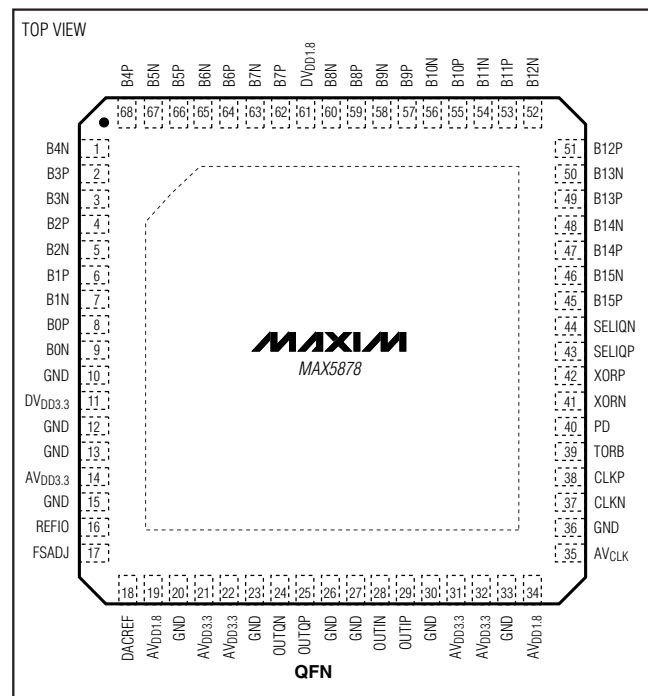
- ◆ 250Mps Output Update Rate
- ◆ Noise Spectral Density = -164dBFS/Hz at  $f_{OUT} = 16\text{MHz}$
- ◆ Excellent SFDR and IMD
  - SFDR = 76dBc at  $f_{OUT} = 16\text{MHz}$  (to Nyquist)
  - SFDR = 71dBc at  $f_{OUT} = 80\text{MHz}$  (to Nyquist)
  - IMD = -90dBc at  $f_{OUT} = 10\text{MHz}$
  - IMD = -72dBc at  $f_{OUT} = 80\text{MHz}$
- ◆ ACLR = 75dB at  $f_{OUT} = 61\text{MHz}$
- ◆ 2mA to 20mA Full-Scale Output Current
- ◆ LVDS-Compatible Digital and Clock Inputs
- ◆ On-Chip +1.20V Bandgap Reference
- ◆ Low 296mW Power Dissipation
- ◆ Compact 68 QFN-EP Package (10mm x 10mm)
- ◆ Evaluation Kit Available (MAX5878EVKIT)

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX5878EGK	-40°C to +85°C	68 QFN-EP**	G6800-4

\*\*EP = Exposed pad.

## Pin Configuration



# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## ABSOLUTE MAXIMUM RATINGS

AVDD1.8, DVDD1.8 to GND, DACREF.....-0.3V to +2.16V  
 AVDD3.3, DVDD3.3, AVCLK to GND, DACREF.....-0.3V to +3.9V  
 REFIO, FSADJ to  
 GND, DACREF.....-0.3V to (AVDD3.3 + 0.3V)  
 OUTIP, OUTIN, OUTQP,  
 OUTQN to GND, DACREF.....-1V to (AVDD3.3 + 0.3V)  
 CLKP, CLKN to GND, DACREF.....-0.3V to (AVCLK + 0.3V)  
 B15P/B15N-B0P/B0N, XORN, XORP, SELIQN,  
 SELIQP to GND, DACREF.....-0.3V to (DVDD1.8 + 0.3V)  
 TORB, PD to GND, DACREF.....-0.3V to (DVDD3.3 + 0.3V)

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

68-Pin QFN-EP

(derate 41.7mW/°C above +70°C) (Note 1).....3333.3mW

Thermal Resistance  $\theta_{JA}$  (Note 1).....+24°C/W

Operating Temperature Range ..... -40°C to +85°C

Junction Temperature ..... +150°C

Storage Temperature Range ..... -60°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

**Note 1:** Thermal resistors based on a multilayer board with 4 x 4 via array in exposed paddle area.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(AVDD3.3 = DVDD3.3 = AVCLK = +3.3V, AVDD1.8 = DVDD1.8 = +1.8V, GND = 0, f<sub>CLK</sub> = 2 x f<sub>DAC</sub>, external reference V<sub>REFIO</sub> = +1.25V, output load 50Ω double-terminated, transformer-coupled output, I<sub>OUTFS</sub> = 20mA, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>STATIC PERFORMANCE</b>						
Resolution				16		Bits
Integral Nonlinearity	INL	Measured differentially		±3		LSB
Differential Nonlinearity	DNL	Measured differentially		±2		LSB
Offset Error	OS		-0.015	±0.001	+0.015	%FS
Offset-Drift Tempco				±10		ppm/°C
Full-Scale Gain Error	GE <sub>FS</sub>	External reference	-4.1	-0.6	+4.1	%FS
		Internal reference		±100		ppm/°C
		External reference		±50		
Full-Scale Output Current	I <sub>OUTFS</sub>	(Note 3)	2		20	mA
Output Compliance		Single-ended	-0.5		+1.1	V
Output Resistance	R <sub>OUT</sub>			1		MΩ
Output Capacitance	C <sub>OUT</sub>			5		pF
<b>DYNAMIC PERFORMANCE</b>						
Clock Frequency	f <sub>CLK</sub>		2		500	MHz
Output Update Rate	f <sub>DAC</sub>		1		250	Msps
Noise Spectral Density		f <sub>DAC</sub> = 150MHz	f <sub>OUT</sub> = 16MHz, -12dBFS	-164		dBFS/ Hz
		f <sub>DAC</sub> = 250MHz	f <sub>OUT</sub> = 80MHz, -12dBFS	-161		

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## ELECTRICAL CHARACTERISTICS (continued)

(AVDD3.3 = DVDD3.3 = AVCLK = +3.3V, AVDD1.8 = DVDD1.8 = +1.8V, GND = 0, fCLK = 2 x fDAC, external reference VREFIO = +1.25V, output load 50Ω double-terminated, transformer-coupled output, IOUTFS = 20mA, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Spurious-Free Dynamic Range to Nyquist	SFDR	fDAC = 100MHz	fOUT = 1MHz, 0dBFS	94		dBc	
			fOUT = 1MHz, -6dBFS	87			
			fOUT = 1MHz, -12dBFS	81			
			fOUT = 10MHz, -12dBFS	81			
			fOUT = 30MHz, -12dBFS	79			
		fDAC = 200MHz	fOUT = 10MHz, -12dBFS	75			
			fOUT = 16MHz, -12dBFS, TA ≥ +25°C	69	76		
			fOUT = 16MHz, -12dBFS	67	76		
			fOUT = 50MHz, -12dBFS	73			
		fDAC = 250MHz	fOUT = 80MHz, -12dBFS	71			
			fOUT = 10MHz, -12dBFS	74			
			fOUT = 50MHz, -12dBFS	75			
			fOUT = 80MHz, -12dBFS	71			
fOUT = 100MHz, -12dBFS	69						
Spurious-Free Dynamic Range, 25MHz Bandwidth	SFDR	fDAC = 150MHz	fOUT = 16MHz, -12dBFS	78		dBc	
Two-Tone IMD	TTIMD	fDAC = 100MHz	fOUT1 = 9MHz, -7dBFS; fOUT2 = 10MHz, -7dBFS	-90		dBc	
		fDAC = 200MHz	fOUT1 = 79MHz, -7dBFS; fOUT2 = 80MHz, -7dBFS	-72			
Four-Tone IMD, 1MHz Frequency Spacing, GSM Model	FTIMD	fDAC = 150MHz	fOUT = 16MHz, -12dBFS	-80		dBc	
Adjacent Channel Leakage Power Ratio 3.84MHz Bandwidth, W-CDMA Model	ACLR	fDAC = 184.32MHz	fOUT = 61.44MHz	75		dB	
Output Bandwidth	BW-1dB	(Note 4)	240		MHz		
<b>INTER-DAC CHARACTERISTICS</b>							
Gain Matching	ΔGain	fOUT = DC - 80MHz		±0.2		dB	
		fOUT = DC		-0.22	+0.01		+0.22
Gain-Matching Tempco	ΔGain/°C			±20		ppm/°C	
Phase Matching	ΔPhase	fOUT = 60MHz		±0.25		Degrees	
Phase-Matching Tempco	ΔPhase/°C	fOUT = 60MHz		±0.002		Degrees/°C	
Channel-to-Channel Crosstalk		fCLK = 400MHz, fOUT = 50MHz, 0dBFS		86		dB	
<b>REFERENCE</b>							
Internal Reference Voltage Range	VREFIO			1.14	1.2	1.26	V

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## ELECTRICAL CHARACTERISTICS (continued)

(AVDD3.3 = DVDD3.3 = AVCLK = +3.3V, AVDD1.8 = DVDD1.8 = +1.8V, GND = 0, f<sub>CLK</sub> = 2 × f<sub>DAC</sub>, external reference V<sub>REFIO</sub> = +1.25V, output load 50Ω double-terminated, transformer-coupled output, I<sub>OUTFS</sub> = 20mA, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Input Compliance Range	V <sub>REFIOCR</sub>		0.125		1.260	V
Reference Input Resistance	R <sub>REFIO</sub>			10		kΩ
Reference Voltage Drift	TC <sub>REF</sub>			±25		ppm/°C
<b>ANALOG OUTPUT TIMING (See Figure 4)</b>						
Output Fall Time	t <sub>FALL</sub>	90% to 10% (Note 5)		0.7		ns
Output Rise Time	t <sub>RISE</sub>	10% to 90% (Note 5)		0.7		ns
Output Propagation Delay	t <sub>PD</sub>	Excluding data latency (Note 5)		1.1		ns
Glitch Impulse		Measured differentially		1		pV•s
Output Noise	n <sub>OUT</sub>	I <sub>OUTFS</sub> = 2mA		30		pA/√Hz
		I <sub>OUTFS</sub> = 20mA		30		
<b>TIMING CHARACTERISTICS</b>						
Data to Clock Setup Time	t <sub>SETUP</sub>	Referenced to rising edge of clock (Note 6)	-1.2			ns
Data to Clock Hold Time	t <sub>HOLD</sub>	Referenced to rising edge of clock (Note 6)	2.0			ns
Data Latency		Latency to I output		9		Clock Cycles
		Latency to Q output		8		
Minimum Clock Pulse-Width High	t <sub>CH</sub>	CLKP, CLKN		0.9		ns
Minimum Clock Pulse-Width Low	t <sub>CL</sub>	CLKP, CLKN		0.9		ns
<b>LVDS LOGIC INPUTS (B15P/B15N–B0P/B0N, XORN, XORP, SELIQN, SELIQP)</b>						
Differential Input-Logic High	V <sub>IH</sub>				100	mV
Differential Input-Logic Low	V <sub>IL</sub>		-100			mV
Common-Mode Voltage Range	V <sub>CMR</sub>		1.125		1.375	V
Differential Input Resistance	R <sub>IN</sub>	(Note 7)		110		Ω
Input Capacitance	C <sub>IN</sub>			2.5		pF
<b>CMOS LOGIC INPUTS (PD, TORB)</b>						
Input-Logic High	V <sub>IH</sub>		0.7 ×			V
Input-Logic Low	V <sub>IL</sub>			0.3 ×		
Input Leakage Current	I <sub>IN</sub>		-20	1	+20	μA
PD, TORB Internal Pull-down Resistance		V <sub>PD</sub> = V <sub>TORB</sub> = 3.3V		1.5		MΩ
Input Capacitance	C <sub>IN</sub>			2.5		pF
<b>CLOCK INPUTS (CLKP, CLKN)</b>						
Differential Input Voltage Swing		Sine wave		>1.5		V <sub>P-P</sub>
		Square wave		>0.5		

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## ELECTRICAL CHARACTERISTICS (continued)

(AVDD3.3 = DVDD3.3 = AVCLK = +3.3V, AVDD1.8 = DVDD1.8 = +1.8V, GND = 0, fCLK = 2 x fDAC, external reference VREFIO = +1.25V, output load 50Ω double-terminated, transformer-coupled output, IOUTFS = 20mA, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Slew Rate	SRCLK	(Note 8)		>100		V/μs
External Common-Mode Voltage Range	VCOM			AVCLK / 2 ±0.3		V
Input Resistance	RCLK			5		kΩ
Input Capacitance	CCLK			2.5		pF
<b>POWER SUPPLIES</b>						
Analog Supply Voltage Range	AVDD3.3		3.135	3.3	3.465	V
	AVDD1.8		1.710	1.8	1.890	
Digital Supply Voltage Range	DVDD3.3		3.135	3.3	3.465	V
	DVDD1.8		1.710	1.8	1.890	
Analog Supply Current	IAVDD3.3	fDAC = 250Msps, fOUT = 16MHz		52	56	mA
		Power-down		1		μA
	IAVDD1.8	fDAC = 250Msps, fOUT = 16MHz		32	36	mA
		Power-down		1		μA
Digital Supply Current	IDVDD3.3	fDAC = 250Msps, fOUT = 16MHz		0.2	1	mA
		Power-down		1		μA
	IDVDD1.8	fDAC = 250Msps, fOUT = 16MHz		36	40	mA
		Power-down		4		μA
Power Dissipation	PDISS	fDAC = 250Msps, fOUT = 16MHz		296	324	mW
		Power-down		16		μW
Power-Supply Rejection Ratio	PSRR	AVDD3.3 = AVCLK = DVDD3.3 = +3.3V ±5% (Notes 8, 9)	-0.1		+0.1	%FS/V

**Note 2:** Specifications at TA ≥ +25°C are guaranteed by production testing. Specifications at TA < +25°C are guaranteed by design.

**Note 3:** Nominal full-scale current IOUTFS = 32 x IREF.

**Note 4:** This parameter does not include update-rate depending effects of sin(x)/x filtering inherent in the MAX5878.

**Note 5:** Parameter measured single-ended into a 50Ω termination resistor.

**Note 6:** Not production tested. Guaranteed by design.

**Note 7:** No termination resistance between XORP and XORN.

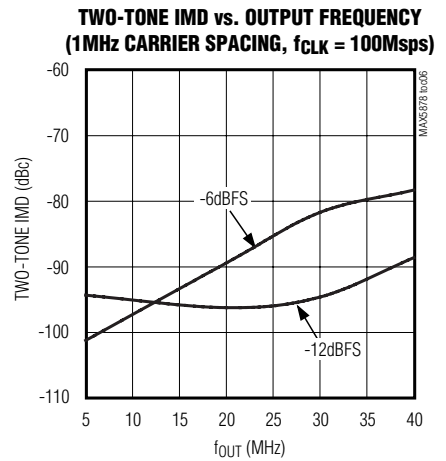
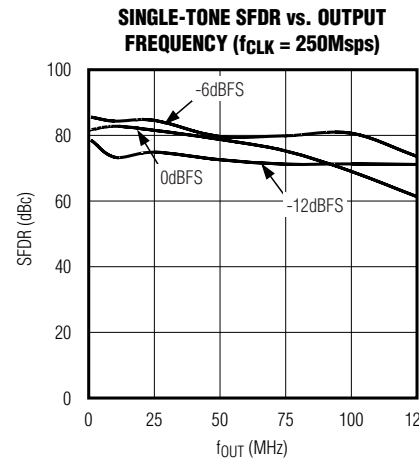
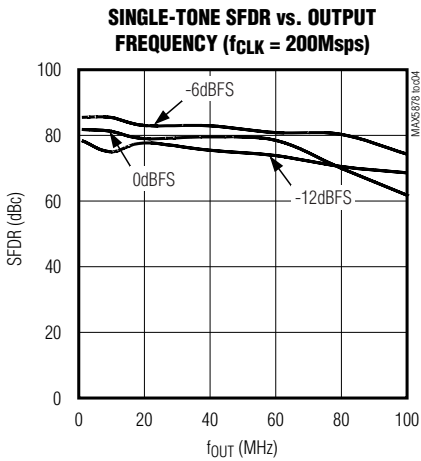
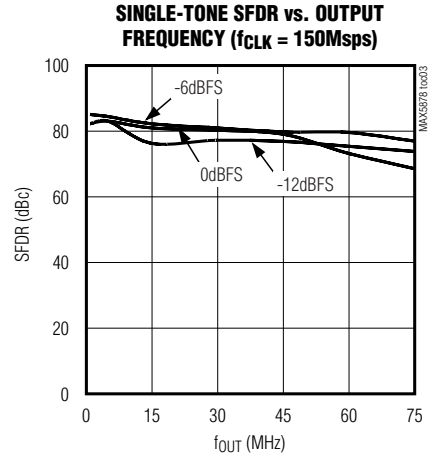
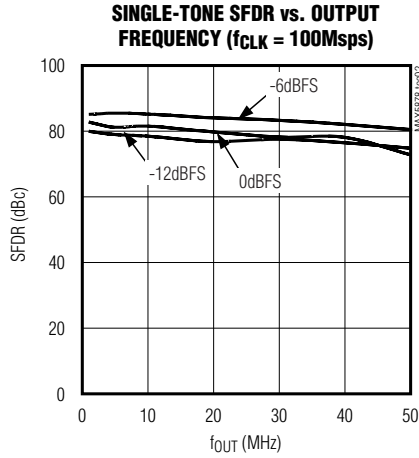
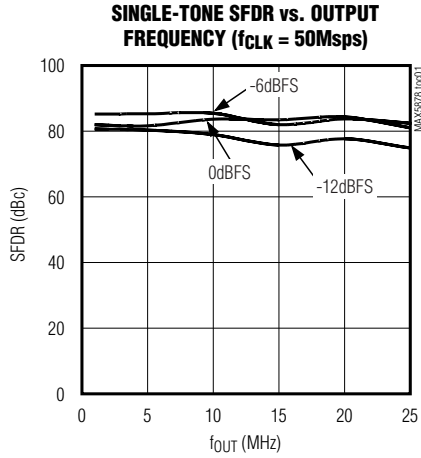
**Note 8:** A differential clock input slew rate of >100V/μs is required to achieve the specified dynamic performance.

**Note 9:** Parameter defined as the change in midscale output caused by a ±5% variation in the nominal supply voltage.

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## Typical Operating Characteristics

( $AV_{DD3.3} = DV_{DD3.3} = AV_{CLK} = +3.3V$ ,  $AV_{DD1.8} = DV_{DD1.8} = +1.8V$ , external reference,  $V_{REFIO} = +1.25V$ ,  $R_L = 50\Omega$  double-terminated,  $I_{OUTFS} = 20mA$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

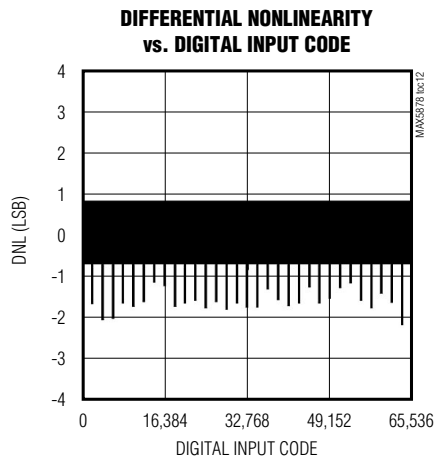
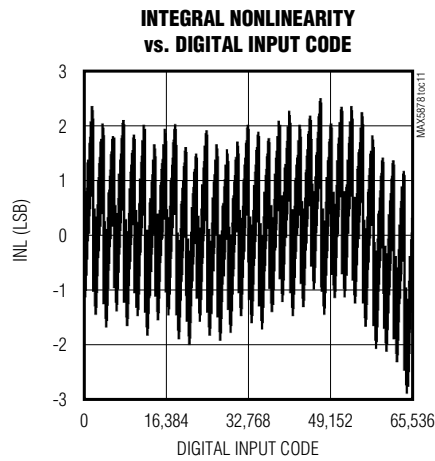
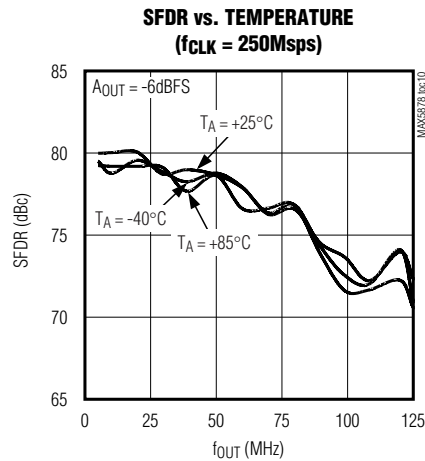
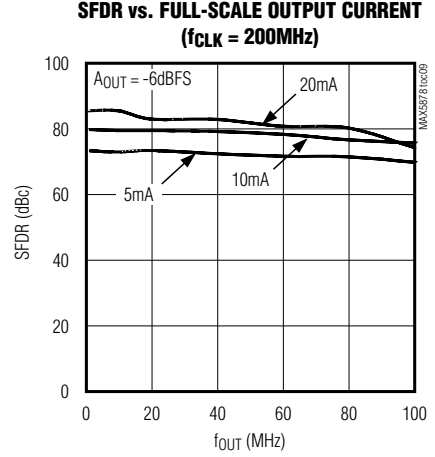
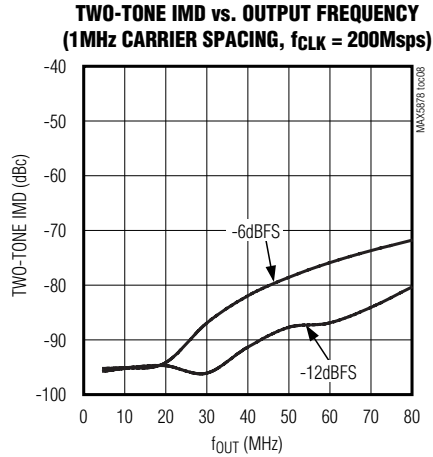
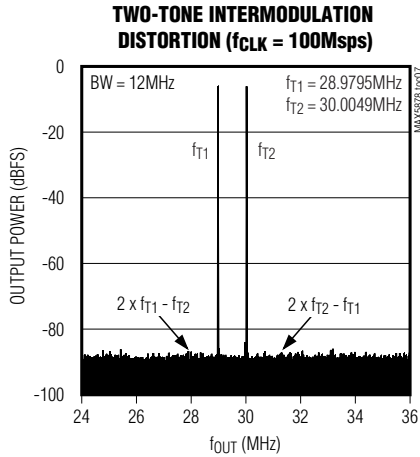


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## Typical Operating Characteristics (continued)

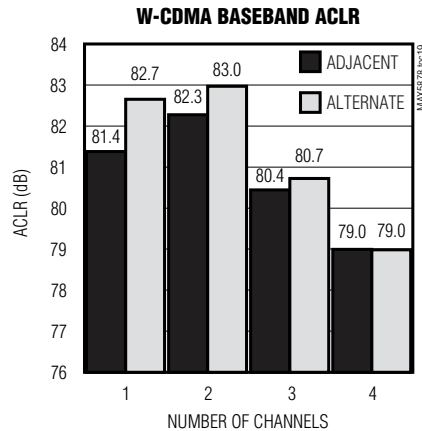
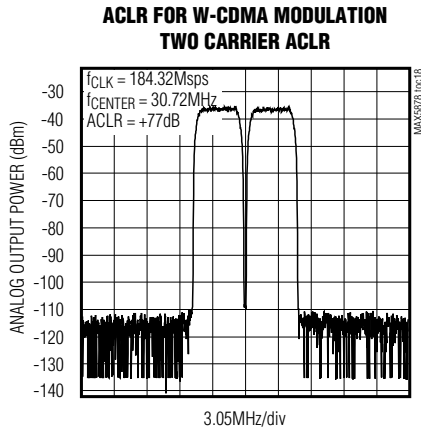
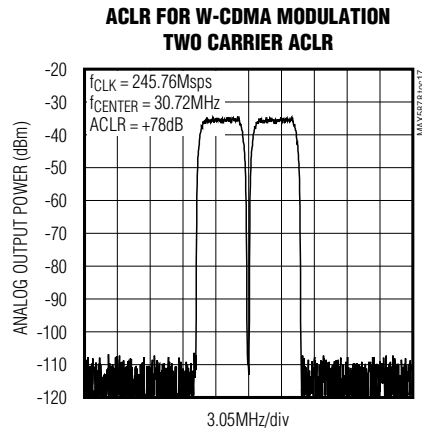
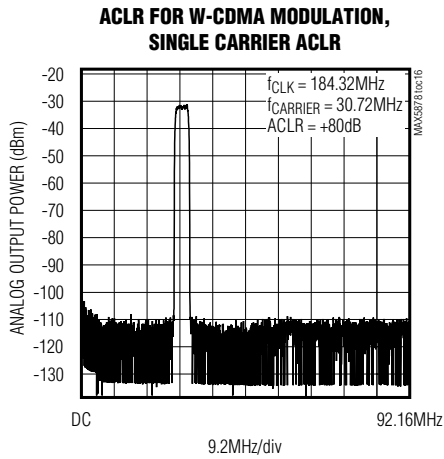
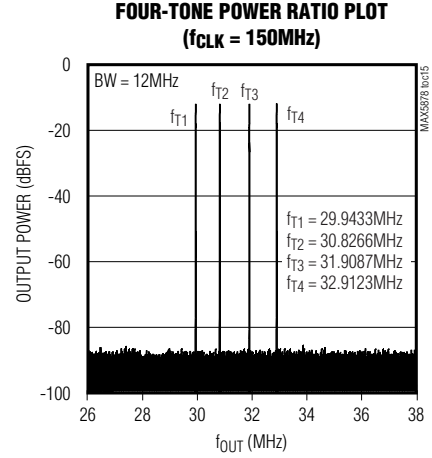
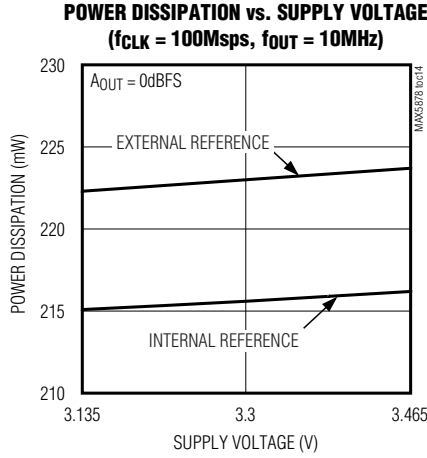
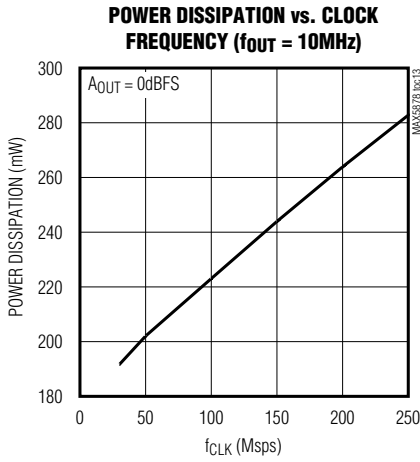
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# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## Typical Operating Characteristics (continued)

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# 16-Bit, 250Mbps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## Pin Description

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PIN	NAME	FUNCTION
1	B4N	Complementary Data Bit 4
2	B3P	Data Bit 3
3	B3N	Complementary Data Bit 3
4	B2P	Data Bit 2
5	B2N	Complementary Data Bit 2
6	B1P	Data Bit 1
7	B1N	Complementary Data Bit 1
8	B0P	Data Bit 0 (LSB)
9	B0N	Complementary Data Bit 0 (LSB)
10, 12, 13, 15, 20, 23, 26, 27, 30, 33, 36	GND	Ground
11	DVDD3.3	Digital Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1 $\mu$ F capacitor to GND.
14, 21, 22, 31, 32	AVDD3.3	Analog Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass each pin with a 0.1 $\mu$ F capacitor to GND.
16	REFIO	Reference I/O. Output of the internal 1.2V precision bandgap reference. Bypass with a 1 $\mu$ F capacitor to GND. REFIO can be driven with an external reference source. See Table 1.
17	FSADJ	Full-Scale Adjust Input. This input sets the full-scale output current of the DAC. For a 20mA full-scale output current, connect a 2k $\Omega$ resistor between FSADJ and DACREF. See Table 1.
18	DACREF	Current-Set Resistor Return Path. Internally connected to GND. <b>Do not use as an external ground connection.</b>
19, 34	AVDD1.8	Analog Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass each pin with a 0.1 $\mu$ F capacitor to GND.
24	OUTQN	Complementary Q-DAC Output. Negative terminal for current output.
25	OUTQP	Q-DAC Output. Positive terminal for current output.
28	OUTIN	Complementary I-DAC Output. Negative terminal for current output.
29	OUTIP	I-DAC Output. Positive terminal for current output.
35	AVCLK	Clock Supply Voltage. Accepts a 3.135V to 3.465V supply voltage range. Bypass with a 0.1 $\mu$ F capacitor to GND.
37	CLKN	Complementary Converter Clock Input. Negative input terminal for differential converter clock. Internally biased to AVCLK / 2.
38	CLKP	Converter Clock Input. Positive input terminal for differential converter clock. Internally biased to AVCLK / 2.
39	TORB	Two's-Complement/Binary Select Input. Set TORB to a CMOS-logic-high level to indicate a two's-complement input format. Set TORB to a CMOS-logic-low level to indicate a binary input format. TORB has an internal pulldown resistor.

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## Pin Description (continued)

PIN	NAME	FUNCTION
40	PD	Power-Down Input. Set PD to a CMOS-logic-high level to force the DAC into power-down mode. Set PD to a CMOS-logic-low level for normal operation. PD has an internal pulldown resistor.
41	XORN	Complementary LVDS DAC Exclusive-OR Select Input. Set XORN high and XORP low to allow the data stream to pass unchanged to the DAC input. Set XORN low and XORP high to invert the DAC input data. If unused, connect XORN to DV <sub>DD1.8</sub> .
42	XORP	LVDS DAC Exclusive-OR Select Input. Set XORN high and XORP low to allow the data stream to pass unchanged to the DAC input. Set XORN low and XORP high to invert the DAC input data. If unused, connect XORP to GND.
43	SELIQP	LVDS DAC Select Input. Set SELIQN low and SELIQP high to direct data to the I-DAC outputs. Set SELIQP low and SELIQN high to direct data to the Q-DAC outputs.
44	SELIQN	Complementary LVDS DAC Select Input. Set SELIQN low and SELIQP high to direct data to the I-DAC outputs. Set SELIQP low and SELIQN high to direct data to the Q-DAC outputs.
45	B15P	Data Bit 15 (MSB)
46	B15N	Complementary Data Bit 15 (MSB)
47	B14P	Data Bit 14
48	B14N	Complementary Data Bit 14
49	B13P	Data Bit 13
50	B13N	Complementary Data Bit 13
51	B12P	Data Bit 12
52	B12N	Complementary Data Bit 12
53	B11P	Data Bit 11
54	B11N	Complementary Data Bit 11
55	B10P	Data Bit 10
56	B10N	Complementary Data Bit 10
57	B9P	Data Bit 9
58	B9N	Complementary Data Bit 9
59	B8P	Data Bit 8
60	B8N	Complementary Data Bit 8
61	DV <sub>DD1.8</sub>	Digital Supply Voltage. Accepts a 1.71V to 1.89V supply voltage range. Bypass with a 0.1 $\mu$ F capacitor to GND.
62	B7P	Data Bit 7
63	B7N	Complementary Data Bit 7
64	B6P	Data Bit 6
65	B6N	Complementary Data Bit 6
66	B5P	Data Bit 5
67	B5N	Complementary Data Bit 5
68	B4P	Data Bit 4
—	EP	Exposed Pad. Must be connected to GND through a low-impedance path.

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

MAX5878

## Detailed Description

### Architecture

The MAX5878 high-performance, 16-bit, dual current-steering DAC (Figure 1) operates with DAC update rates up to 250Mps. The converter consists of input registers and a demultiplexer for single-port operation, followed by a current-steering array. During operation, the input data registers demultiplex the single-port data bus. The current-steering array generates differential full-scale currents in the 2mA to 20mA range. An internal current-switching network, in combination with external 50Ω termination resistors, converts the differential output currents into dual differential output voltages with a 0.1V to 1V peak-to-peak output voltage range. An integrated

+1.2V bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale output range.

### Reference Architecture and Operation

The MAX5878 supports operation with the internal +1.2V bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source. REFIO also serves as a reference output when the DAC operates in internal reference mode. For stable operation with the internal reference, decouple REFIO to GND with a 1μF capacitor. Due to its limited output drive capability, buffer REFIO with an external amplifier when driving large external loads.

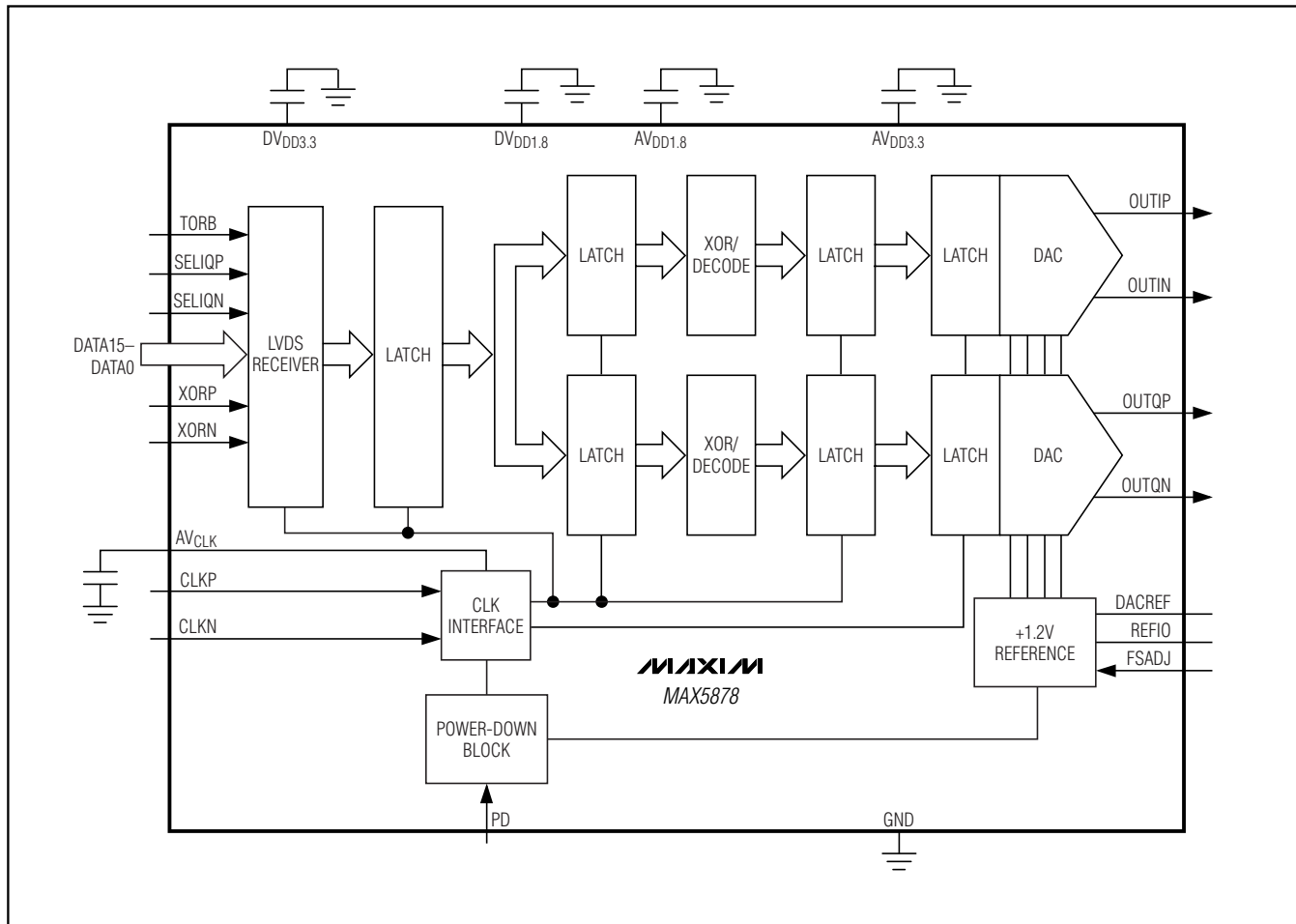


Figure 1. MAX5878 High-Performance, 16-Bit, Dual Current-Steering DAC



# 16-Bit, 250Mbps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

**MAX5878**

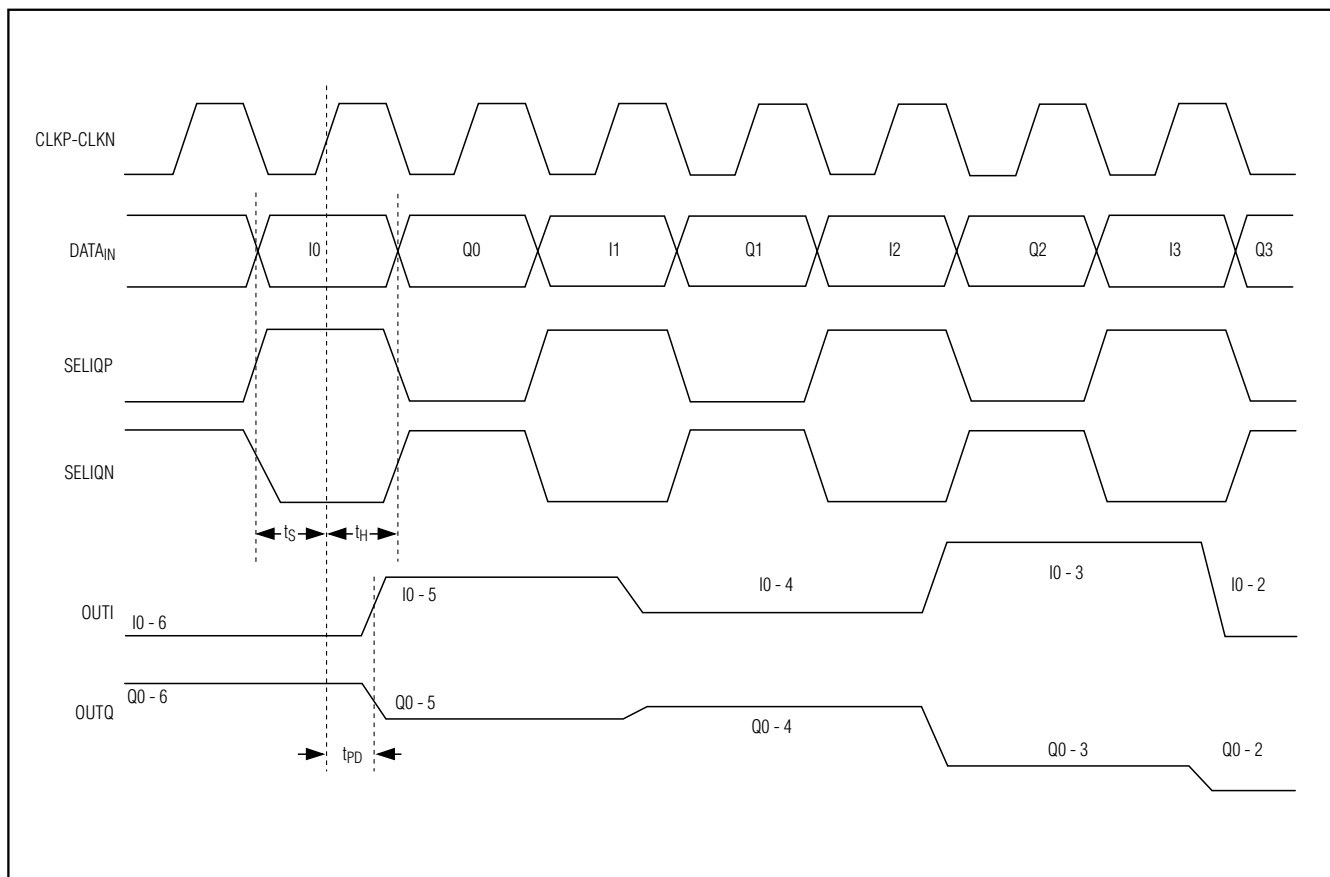


Figure 4. Timing Diagram

### Data Timing Relationship

Figure 4 displays the timing relationship between digital LVDS data, clock, and output signals. The MAX5878 features a 2.0ns hold, a -1.2ns setup, and a 1.1ns propagation delay time. A nine (eight)-clock-cycle latency exists between CLKP/CLKN and OUTIP/OUTIN (OUTQP/OUTQN).

### LVDS-Compatible Digital Inputs (B15P/B15N-B0P/B0N, XORP, XORN, SELIQP, SELIQN)

The MAX5878 latches B15P/N-B0P/N, XORP/N, and SELIQP/N data on the rising edge of the clock. A logic-high signal on SELIQP and a logic-low signal on SELIQN directs data onto the I-DAC inputs. A logic-low signal on SELIQP and a logic-high signal on SELIQN directs data onto the Q-DAC inputs.

The MAX5878 features LVDS receivers on the bus input interface with internal 110Ω termination resistors. See

Figure 5. XORP and XORN are not internally terminated. These LVDS inputs (B15P/N-B0P/N) allow for a low differential voltage swing with low constant power consumption. A 1.25V common-mode level and 250mV differential input swing can be applied to the B15P/N-B0P/N, XORP/N, and SELIQP/N inputs.

The MAX5878 includes LVDS-compatible exclusive-OR inputs (XORP, XORN). Input data (all bits) is compared with the bits applied to XORP and XORN through exclusive-OR gates. Setting XORP high and XORN low inverts the input data. Setting XORP low and XORN high leaves the input data noninverted. By applying a previously encoded pseudo-random bit stream to the data input and applying decoding to XORP/XORN, the digital input data can be decorrelated from the DAC output, allowing for the troubleshooting of possible spurious or harmonic distortion degradation due to digital feedthrough on the PC board. If XOR functionality is not required, connect XORP to GND and XORN to DV<sub>DD</sub>1.8.

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

**Table 2. DAC Output Code Table**

DIGITAL INPUT CODE		OUT_P	OUT_N
OFFSET BINARY	TWO'S COMPLEMENT		
0000 0000 0000 0000	1000 0000 0000 0000	0	I <sub>OUTFS</sub>
0111 1111 1111 1111	0000 0000 0000 0000	I <sub>OUTFS</sub> / 2	I <sub>OUTFS</sub> / 2
1111 1111 1111 1111	0111 1111 1111 1111	I <sub>OUTFS</sub>	0

## CMOS-Compatible Digital Inputs Input Data Format Select (TORB)

The TORB input selects between two's-complement or offset binary digital input data. Set TORB to a CMOS-logic-high level to indicate a two's-complement input format. Set TORB to a CMOS-logic-low level to indicate a binary input format.

## Power-Down Operation (PD)

The MAX5878 also features an active-high power-down mode that reduces the DAC's digital current consumption from 36.2mA to less than 5µA and the analog current consumption from 84mA to less than 2µA. Set PD high to power down the MAX5878. Set PD low for normal operation.

When powered down, the MAX5878 reduces the overall power consumption to less than 16µW. The MAX5878 requires 10ms to wake up from power-down and enter a fully operational state. The PD integrated pulldown resistor activates the MAX5878 if PD is left floating.

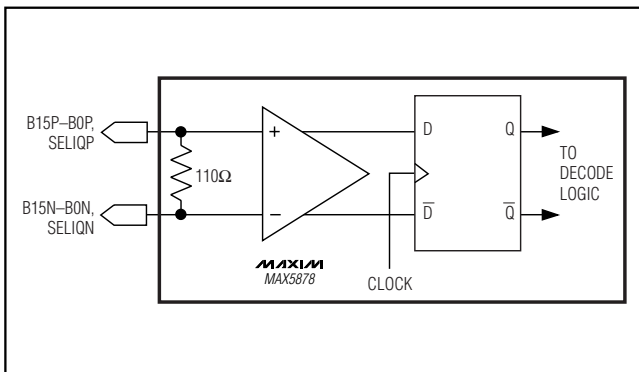


Figure 5. Simplified LVDS-Compatible Digital Input Structure

## Applications Information

### CLK Interface

The MAX5878 features a flexible differential clock input (CLKP, CLKN) with a separate supply (AV<sub>CLK</sub>) to achieve optimum jitter performance. Use an ultra-low jitter clock to achieve the required noise density. Clock jitter must be less than 0.5ps<sub>RMS</sub> for meeting the specified noise density. For that reason, the CLKP/CLKN input source must be designed carefully. The differential clock (CLKN and CLKP) input can be driven from a single-ended or a differential clock source. Differential clock drive is required to achieve the best dynamic performance from the DAC. For single-ended operation, drive CLKP with a low noise source and bypass CLKN to GND with a 0.1µF capacitor.

Figure 6 shows a convenient and quick way to apply a differential signal created from a single-ended source (e.g., HP 8662A signal generator) and a wideband transformer. Alternatively, these inputs can be driven from a CMOS-compatible clock source; however, it is recommended to use sinewave or AC-coupled differential ECL/PECL or LVDS drive for best dynamic performance.

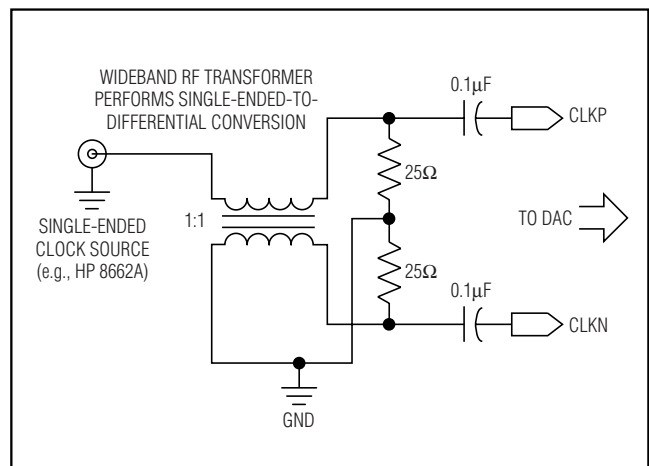


Figure 6. Differential Clock-Signal Generation

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## Differential-to-Single-Ended Conversion Using a Wideband RF Transformer

Use a pair of transformers (Figure 7) or a differential amplifier configuration to convert the differential voltage existing between OUTIP/OUTQP and OUTIN/OUTQN to a single-ended voltage. Optimize the dynamic performance by using a differential transformer-coupled output and limit the output power to <math><0\text{dBm}</math> full scale. Pay close attention to the transformer core saturation characteristics when selecting a transformer for the MAX5878. Transformer core saturation can introduce strong 2nd-order harmonic distortion especially at low output frequencies and high signal amplitudes. For best results, center tap the transformer to ground. When not using a transformer, terminate each DAC output to ground with a  $25\Omega$  resistor. Additionally, place a  $50\Omega$  resistor between the outputs (Figure 8).

For a single-ended unipolar output, select OUTIP (OUTQP) as the output and ground OUTIN (OUTQN) to GND. Driving the MAX5878 single-ended is not recommended since additional noise and distortion will be added.

The distortion performance of the DAC depends on the load impedance. The MAX5878 is optimized for  $50\Omega$  differential double termination. It can be used with a transformer output as shown in Figure 7 or just one  $25\Omega$  resistor from each output to ground and one  $50\Omega$  resistor between the outputs (Figure 8). This produces a full-scale output power of up to  $-2\text{dBm}$ , depending on the output current setting. Higher termination impedance can be used at the cost of degraded distortion performance and increased output noise voltage.

## Grounding, Bypassing, and Power-Supply Considerations

Grounding and power-supply decoupling can strongly influence the MAX5878 performance. Unwanted digital crosstalk couples through the input, reference, power supply, and ground connections, and affects dynamic performance. High-speed, high-frequency applications require closely followed proper grounding and power-supply decoupling. These techniques reduce EMI and internal crosstalk that can significantly affect the MAX5878 dynamic performance.

Use a multilayer printed circuit (PC) board with separate ground and power-supply planes. Run high-speed signals on lines directly above the ground plane. Keep digital signals as far away from sensitive analog inputs and outputs, reference input sense lines, common-mode input, and clock inputs as practical. Use a symmetric design of clock input and the analog output lines to minimize 2nd-order harmonic distortion components, thus optimizing the DAC's dynamic performance. Keep digital signal paths short and run lengths matched to avoid propagation delay and data skew mismatches.

The MAX5878 requires five separate power-supply inputs for analog (AVDD1.8 and AVDD3.3), digital (DVDD1.8 and DVDD3.3), and clock (AVCLK) circuitry. All power-supply pins must be connected to their proper supply. Decouple each AVDD, DVDD, and AVCLK input pin with a separate  $0.1\mu\text{F}$  capacitor as close to the device as possible with the shortest possible connection to the ground plane (Figure 9). Minimize the analog and digital load capacitances for optimized operation. Decouple all three power-supply voltages at the point they enter the PC board with tantalum or electrolytic

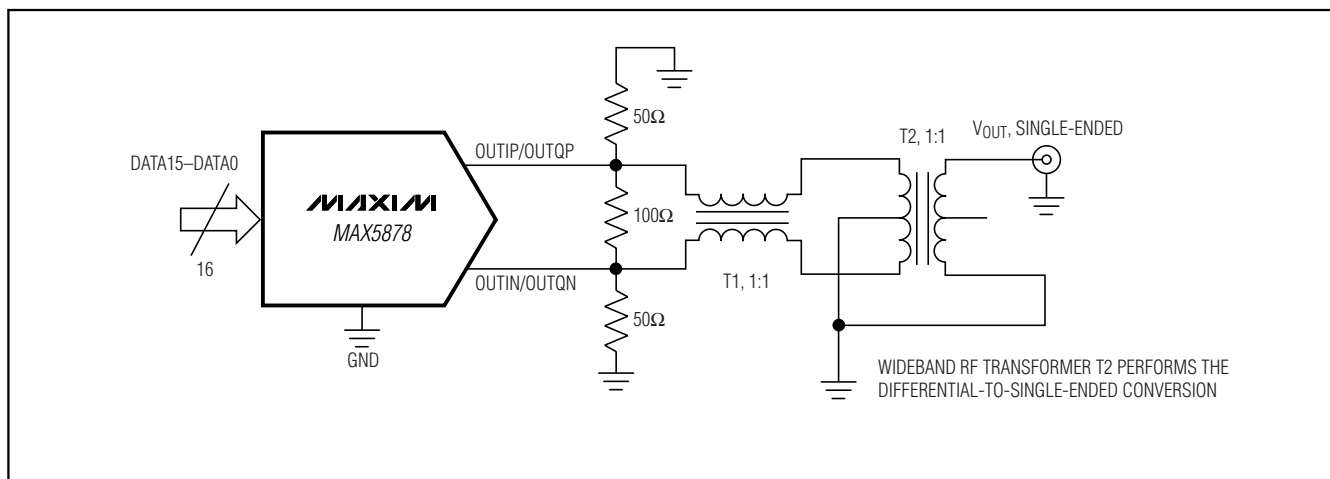


Figure 7. Differential-to-Single-Ended Conversion Using a Wideband RF Transformer

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

The analog and digital power-supply inputs AV<sub>DD3.3</sub>, AV<sub>CLK</sub>, and DV<sub>DD3.3</sub> allow a +3.135V to +3.465V supply voltage range. The analog and digital power-supply inputs AV<sub>DD1.8</sub> and DV<sub>DD1.8</sub> allow a +1.71V to +1.89V supply voltage range.

The MAX5878 is packaged in a 68-pin QFN-EP package, providing greater design flexibility, increased thermal efficiency, and optimized DAC AC performance. The EP enables the use of necessary grounding techniques to ensure highest performance operation. Thermal efficiency is not the key factor, since the MAX5878 features low-power operation. The exposed pad ensures a solid ground connection between the DAC and the PC board's ground layer.

The data converter die attaches to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PC board side of the package. This allows for a solid attachment of the package to the PC board with standard infrared reflow (IR) soldering techniques. A specially created land pattern on the PC board, matching the size of the EP (6mm x 6mm), ensures the proper attachment and grounding of the DAC. Designing vias into the land area and implementing large ground planes in the PC board design allow for the highest performance operation of the DAC. Use an array of at least 4 x 4 vias (≤0.3mm diameter per via hole and 1.2mm pitch between via holes) for this 68-pin QFN-EP package. **Connect the MAX5878 exposed paddle to GND.** Vias connect the land pattern to internal or external copper planes. Use as many vias as possible to the ground plane to minimize inductance.

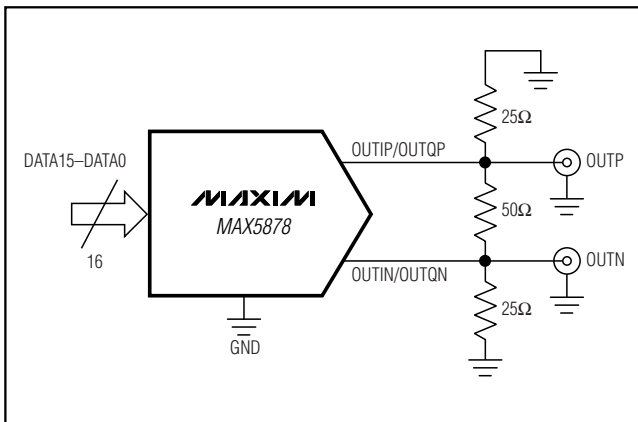


Figure 8. Differential Output Configuration

## Static Performance Parameter Definitions

### Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. For a DAC, the deviations are measured at every individual step.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees a monotonic transfer function.

### Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

### Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

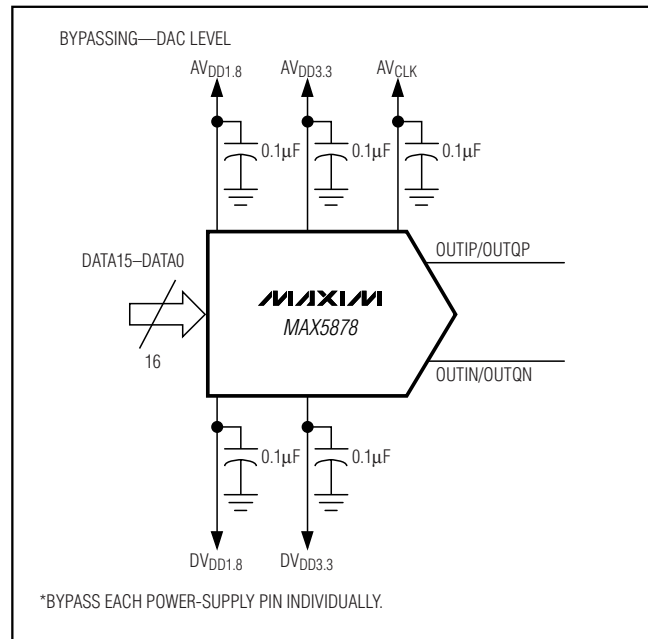


Figure 9. Recommended Power-Supply Decoupling and Bypassing Circuitry



# 16-Bit, 250MSPS, High-Dynamic-Performance, Dual DAC with LVDS Inputs

MAX5878

## Dynamic Performance Parameter Definitions

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog output (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum can be derived from the DAC's resolution (N bits):

$$\text{SNR}_{\text{dB}} = 6.02\text{dB} \times N + 1.76\text{dB}$$

However, noise sources such as thermal noise, reference noise, clock jitter, etc., affect the ideal reading; therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

### Noise Spectral Density

The DAC output noise floor is the sum of the quantization noise and the output amplifier noise (thermal and shot noise). Noise spectral density is the noise power in 1Hz bandwidth, specified in dBFS/Hz.

### Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of their next-largest distortion component. SFDR is usually measured in dBc and with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

### Two-/Four-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD product(s) to either output tone; 2nd-order IMD products usually fall at fre-

quencies that digital filtering easily removes. Therefore, they are not as critical as 3rd-order IMDs. The two-tone IMD performance of the MAX5878 is tested with the two individual output tone levels set to at least -6dBFS and the four-tone performance was tested according to the GSM model at an output frequency of 16MHz and amplitude of -12dBFS.

### Adjacent Channel Leakage Power Ratio (ACLR)

Commonly used in combination with wideband code-division multiple-access (W-CDMA), ACLR reflects the leakage power ratio in dB between the measured power within a channel relative to its adjacent channel. ACLR provides a quantifiable method of determining out-of-band spectral energy and its influence on an adjacent channel when a bandwidth-limited RF signal passes through a nonlinear device.

### Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the converter's specified accuracy.

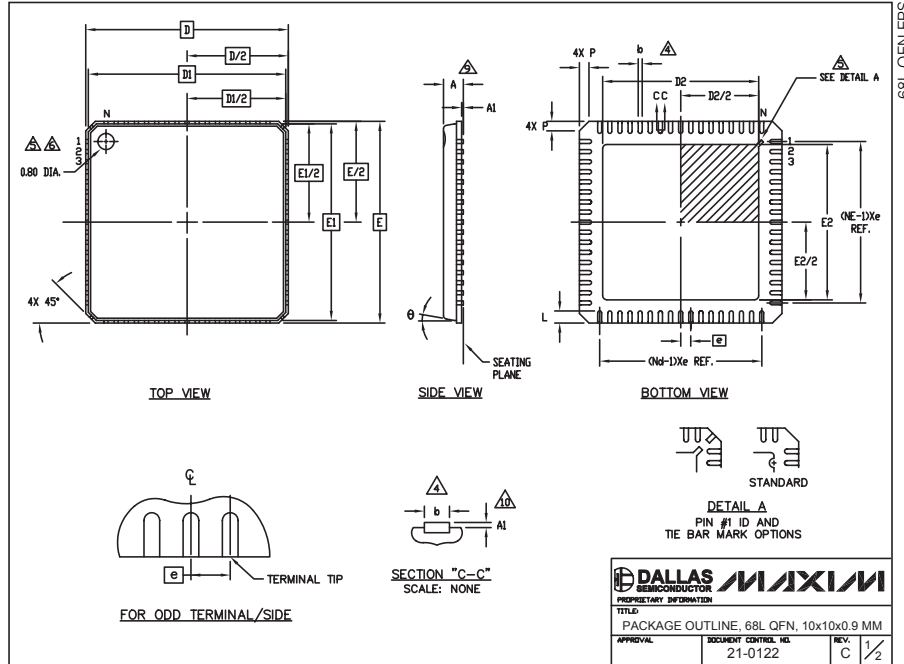
### Glitch Impulse

A glitch is generated when a DAC switches between two codes. The largest glitch is usually generated around the midscale transition, when the input pattern transitions from 011...111 to 100...000. The glitch impulse is found by integrating the voltage of the glitch at the midscale transition over time. The glitch impulse is usually specified in pV•s.

# 16-Bit, 250Mps, High-Dynamic-Performance, Dual DAC with LVDS Inputs

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)



SYMBOL	COMMON DIMENSIONS			N <sub>T</sub>	T <sub>E</sub>
	MIN.	NOM.	MAX.		
A	-	0.90	1.00		
A1	0.00	0.01	0.05	11	
b	0.18	0.23	0.30	4	
D	10.00 BSC				
D1	9.75 BSC				
D2	0.50 BSC				
E	10.00 BSC				
E1	9.75 BSC				
L	0.50	0.60	0.65		
N	68			3	
Nd	17			3	
Ne	17			3	
θ	0	12°			
P	0	0.42	0.60		

EXPOSED PAD VARIATIONS						
PKG CODE	D2			E2		
	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

<b>DALLAS MAXIM</b>		
SEMICONDUCTOR		
PROPRIETARY INFORMATION		
TITLE: PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM		
APPROVAL	DOCUMENT CONTROL, NS	REV. C 1/2
	21-0122	

- DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
- DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M - 1994.
- N IS THE NUMBER OF TERMINALS.
- Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
- DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
- THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
- EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- PACKAGE WARPAGE MAX 0.10mm.
- APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
- APPLIES ONLY TO TERMINALS.
- MEETS JEDEC MO-220.

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