19-0099; Rev 2; 9/95

MAXIM

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

General Description

The MAX706P/R/S/T and MAX708R/S/T microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor +3V power-supply levels in +3V to +5V µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX706P/R/S/T supervisory circuits provide the following four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6sec.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than the main supply.
4) An active-low manual-reset input.

The only difference between the MAX706R, MAX706S, and MAX706T is the reset-threshold voltage levels, which are 2.63V, 2.93V, and 3.08V, respectively. All have active-low reset output signals. The MAX706P is identical to the MAX706R, except its reset output signal is active-high.

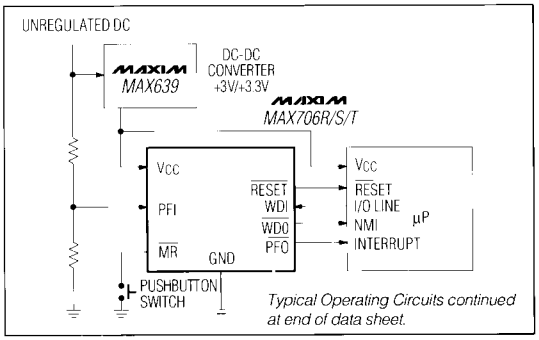
The MAX708R/S/T provide the same functions as the MAX706R/S/T, except they do not have a watchdog timer. Instead, they provide both $\overline{\text{RESET}}$ and RESET outputs. As with the MAX706, devices with R, S, and T suffixes have reset thresholds of 2.63V, 2.93V and 3.08V, respectively.

All seven devices are offered in 8-pin SO, DIP, and µMAX packages.

Applications

Battery-Powered Equipment
Portable Instruments
Computers
Controllers
Intelligent Instruments
Critical µP Power Monitoring

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

Features

- ♦ **µMAX Package: Smallest 8-Pin SO**
- ♦ **Precision Supply-Voltage Monitor**
  2.63V (MAX706P/R, MAX708R)
  2.93V (MAX706S, MAX708S)
  3.08V (MAX706T, MAX708T)
- ♦ **200ms Reset Time Delay**
- ♦ **Debounced TTL/CMOS-Compatible Manual-Reset Input**
- ♦ **100µA Quiescent Current**
- ♦ **Watchdog Timer (MAX706P/R/S/T only): 1.6sec Timeout**
- ♦ **Reset Output Signal:**
  Active-High Only (MAX706P)
  Active-Low Only (MAX706R/S/T)
  Active-High and Active-Low (MAX708R/S/T)
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **8-Pin Surface-Mount Package**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to VCC = 1V**

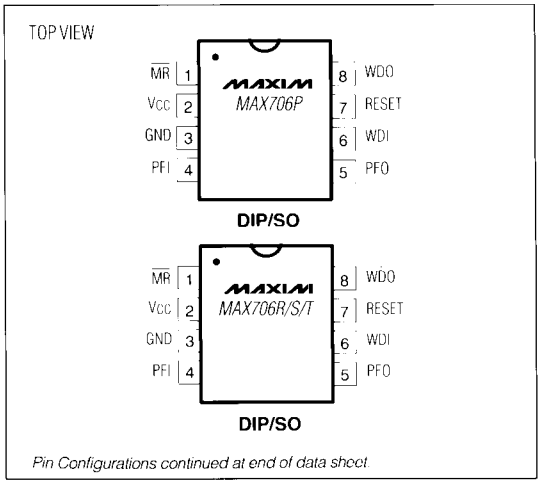
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX706PCPA	0°C to +70°C	8 Plastic DIP
MAX706PCSA	0°C to +70°C	8 SO
MAX706PCUA	0°C to +70°C	8 µMAX
MAX706PEPA	-40°C to +85°C	8 Plastic DIP
MAX706PESA	-40°C to +85°C	8 SO
MAX706PMJA	-55°C to +125°C	8 CERDIP*

Ordering Information continued at end of data sheet.

** Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Pin Configurations continued at end of data sheet.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current (all outputs) 20mA

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- µMAX (derate 4.1mW/°C above +70°C) 330mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C_ _ ..... 0°C to +70°C
- MAX70_E_ _ ..... -40°C to +85°C
- MAX70_M_ _ ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: The input voltage limits on PFI, WDI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX70_P/R: V_{CC} = 2.70V to 5.5V, MAX70_S: V_{CC} = 3.00V to 5.5V, MAX70_T: V_{CC} = 3.15V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}		MAX70_C	1.0		5.5	V
			MAX70_E/M	1.2		5.5	
Supply Current	I_{SUPPLY}	V_{CC} < 3.6V	MAX706_C		90	200	µA
			MAX706_E/M		90	300	
			MAX708_C		50	200	
			MAX708_E/M		50	300	
		V_{CC} < 5.5V	MAX706_C		135	350	
			MAX706_E/M		135	500	
			MAX708_C		65	350	
			MAX708_E/M		65	500	
Reset Threshold (Note 2)	V_{RST}		MAX70_P/R	2.55	2.63	2.70	V
			MAX70_S	2.85	2.93	3.00	
			MAX70_T	3.00	3.08	3.15	
Reset Threshold Hysteresis (Note 2)					20		mV
Reset Pulse Width (Note 2)	t_{RST}	MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V		140	200	280	ms
		V_{CC} = 5.0V			200		
$\overline{RESET}$ Output Voltage (MAX70_R/S/T)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	
	V_{OL}	MAX70_C: V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		MAX70_E/M: V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	
RESET Output Voltage (MAX706P)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 215µA	V_{CC} - 0.6			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	

ELECTRICAL CHARACTERISTICS (continued)

(MAX70_P/R: V_{CC} = 2.70V to 5.5V, MAX70_S: V_{CC} = 3.00V to 5.5V, MAX70_T: V_{CC} = 3.15V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

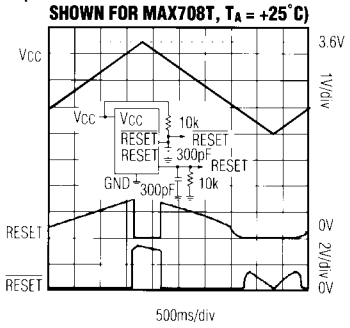
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET Output Voltage (MAX708_)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 1.2mA			0.4	
Watchdog Timeout Period (MAX706_)	t_{WD}	MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V		1.0	1.6	2.25	sec
WDI Pulse Width (MAX706_)	t_{WP}	V_{IL} = 0.4V, V_{IH} = 0.8 x V_{CC}	V_{RST}(max) < V_{CC} < 3.6V	100			ns
			4.5V < V_{CC} < 5.5V	50			
WDI Input Threshold (MAX706_)	V_{IL}	V_{RST} (max) < V_{CC} < 3.6V	Low			0.6	V
	V_{IH}		High	0.7 x V_{CC}			
	V_{IL}	V_{CC} = 5.0V	Low			0.8	
	V_{IH}		High	3.5			
WDI Input Current (MAX706_)		WDI = 0V or V_{CC}		-1.0	0.02	1.0	µA
$\overline{WDO}$ Output Voltage (MAX706_)	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 1.2mA			0.4	
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	V_{RST} (max) < V_{CC} < 3.6V	25	70	250	µA
			4.5V < V_{CC} < 5.5V	100	250	600	
$\overline{MR}$ Pulse Width	t_{MR}	V_{RST} (max) < V_{CC} < 3.6V		500			ns
		4.5V < V_{CC} < 5.5V		150			
MR Input Threshold	V_{IL}	V_{RST} (max) < V_{CC} < 3.6V	Low			0.6	V
	V_{IH}		High	0.7 x V_{CC}			
	V_{IL}	4.5V < V_{CC} < 5.5V	Low			0.8	
	V_{IH}		High	2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)	t_{MD}	V_{RST} (max) < V_{CC} < 3.6V				750	ns
		4.5V < V_{CC} < 5.5V				250	
PFI Input Threshold		MAX70_P/R: V_{CC} = 3.0V; MAX70_S/T: V_{CC} = 3.3V, PFI falling		1.20	1.25	1.30	V
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	V_{RST} (max) < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}		I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}		I_{SINK} = 3.2mA			0.4	

Note 2: Applies to both $\overline{RESET}$ in the MAX70_R/S/T, and RESET in the MAX706P and MAX708R/S/T.

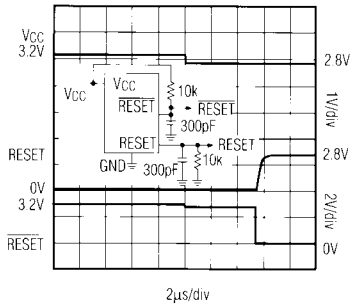
+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

Typical Operating Characteristics

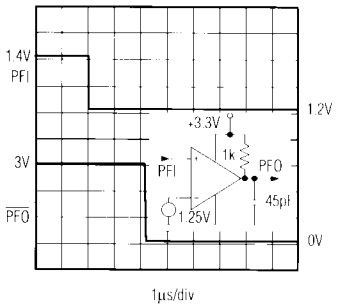
RESET, $\overline{\text{RESET}}$ OUTPUT VOLTAGES vs. SUPPLY VOLTAGE (RESET OUTPUTS AND RESET THRESHOLDS SHOWN FOR MAX708T, T_A = +25°C)



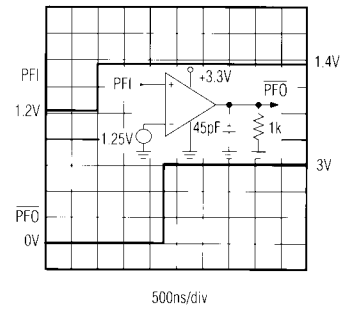
RESET, $\overline{\text{RESET}}$ RESPONSE TIMES



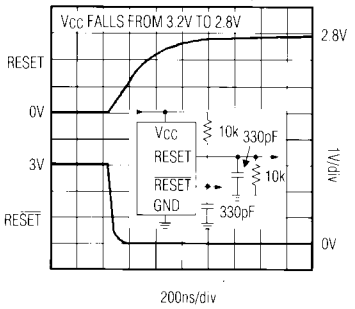
POWER-FAIL COMPARATOR ASSERTION RESPONSE TIME



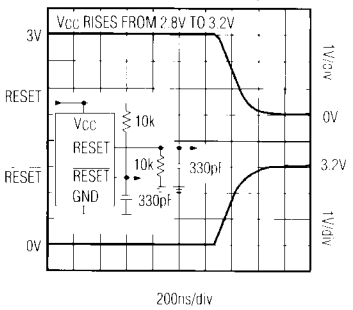
POWER-FAIL COMPARATOR DEASSERTION RESPONSE TIME



RESET, $\overline{\text{RESET}}$ RISE AND FALL TIMES (RESET ASSERTED)



RESET, RESET RISE AND FALL TIMES (RESET DEASSERTED)



Pin Description

PIN						NAME	FUNCTION
MAX706P		MAX706R/S/T		MAX708R/S/T			
DIP/SO	µMAX	DIP/SO	µMAX	DIP/SO	µMAX		
1	3	1	3	1	3	$\overline{MR}$	Manual-Reset Input. When pulled below 0.6V, $\overline{MR}$ triggers a reset pulse. It is TTL/CMOS-compatible when V_{CC} = 5V and can be shorted to ground with a switch. This active-low input has an internal 70µA pull-up current. Leave floating or connect to V_{CC} if not used.
2	4	2	4	2	4	V_{CC}	Supply-Voltage Input
3	5	3	5	3	5	GND	Ground
4	6	4	6	4	6	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ remains high. Connect PFI to GND when not used.
5	7	5	7	5	7	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low and sinks current; otherwise, $\overline{PFO}$ remains high. Leave unconnected if not used.
6	8	6	8	–	–	WDI	Watchdog Input. A rising or falling edge must occur at WDI within 1.6sec or $\overline{WDO}$ goes low (Figure 4). The internal watchdog timer is reset to zero when reset is asserted or when a transition occurs at WDI. The watchdog function cannot be disabled.
–	–	–	–	6	8	N.C.	No Connect—not internally connected.
–	–	7	1	7	1	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ remains low while V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains low for 200ms after the reset condition are terminated (Figure 3).
7	1	–	–	8	2	RESET	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains high for 200ms after the reset conditions are terminated (Figure 3).
8	2	8	2	–	–	$\overline{WDO}$	Watchdog Output. $\overline{WDO}$ goes low when a transition does not occur at WDI within 1.6sec, and remains low until a transition occurs at WDI (indicating the watchdog interrupt has been serviced). $\overline{WDO}$ also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output signal, WDO goes high as soon as V_{CC} exceeds the reset threshold.

Detailed Description

$\overline{RESET}$ and RESET Outputs

A microprocessor's (µP's) reset input starts it in a known state. When the µP is in an unknown state, it should be held in reset. The MAX706P/R/S/T and MAX708R/S/T assert reset when V_{CC} is low, preventing code execution errors during power-up, power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low and RESET is guaranteed to be a logic high. As V_{CC} rises, $\overline{RESET}$ and RESET remain asserted. Once V_{CC} exceeds the reset threshold, the internal timer causes $\overline{RESET}$ and RESET to be deasserted after a time equal to the reset pulse width, which is typically 200ms (Figure 3). If a power-fail or brownout condition occurs (i.e. V_{CC} drops below the reset threshold), $\overline{RESET}$ and RESET are asserted. As long as V_{CC} remains below the reset threshold, the internal timer is continually reset, causing the $\overline{RESET}$ and RESET outputs to remain asserted. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-down, once V_{CC} drops below the reset threshold, $\overline{RESET}$ and RESET are guaranteed to be asserted for $V_{CC} \geq 1V$.

The MAX706P provides a RESET signal, the MAX706R/S/T provide a $\overline{RESET}$ signal, and the MAX708R/S/T provide both RESET and $\overline{RESET}$.

Watchdog Timer (MAX706P/R/S/T)

The MAX706P/R/S/T watchdog circuit monitors the µP's activity. If the µP does not toggle the Watchdog Input (WDI) within 1.6sec, the Watchdog Output (WDO) goes low (Figure 4). If the reset signal is asserted, the watchdog timer will be reset to zero and disabled. As soon as reset is released, the timer starts counting. WDI can detect pulses as narrow as 100ns with a 2.7V supply and 50ns with a 4.5V supply.

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

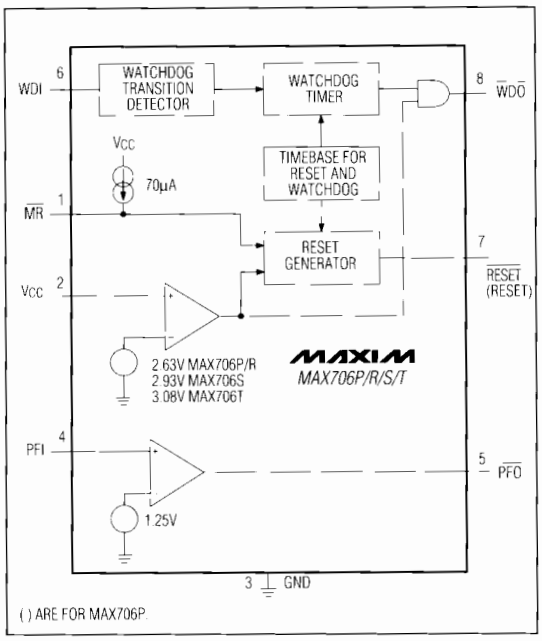


Figure 1. MAX706P/R/S/T Block Diagram

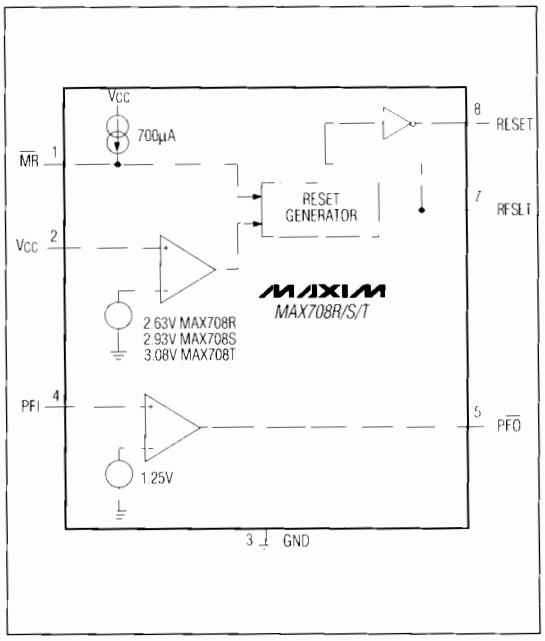


Figure 2. MAX708R/S/T Block Diagram

WDO can be connected to the non-maskable interrupt (NMI) input of a µP. When VCC drops below the reset threshold, WDO immediately goes low, even if the watchdog timer has not timed out (Figure 3). Normally, this would trigger an NMI, but since reset is asserted simultaneously, the NMI is overridden. WDO can instead be connected to MR to generate a reset pulse when the watchdog times out.

Manual Reset

The Manual-Reset (MR) input allows RESET and RESET to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. MR can be driven by an external logic line since it is TTL/CMOS compatible. The minimum MR input pulse width is 500ns when VCC = +3V and 150ns when VCC = +5V. Leave MR floating or tie to VCC when not used.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference. The power-fail comparator has 10mV of hysteresis which prevents repeated triggering of the Power-Fail Output (PFO).

To build an early-warning power-failure circuit, use the Power- Fail Comparator Input (PFI) to monitor the unregulated DC supply voltage (see *Typical Operating Circuit*). Connect the PFI pin to a resistor-divider network such that the voltage at PFI falls below 1.25V just before the regulator drops out. Use PFO to interrupt the µP so it can prepare for an orderly power-down.

Regulated and unregulated voltages can be monitored by simply adjusting the PFI resistor-divider network values to the appropriate ratio. In addition, the reset signal can be asserted at voltages other than the VCC reset threshold, as shown in Figure 5. Connect PFO to MR to initiate a reset pulse when the 12V supply drops below a user-specified threshold (11V in this example) or when VCC falls below the reset threshold.

Applications Information

Operation with +3V and +5V Supplies

The MAX706P/R/S/T and MAX708R/S/T provide voltage monitoring at the reset threshold (2.63V to 3.08V) when powered from either +3V or +5V. They are ideal in porta-

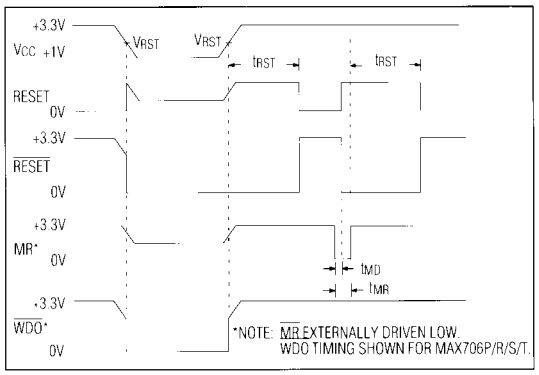


Figure 3. RESET, RESET, MR and WDO Timing

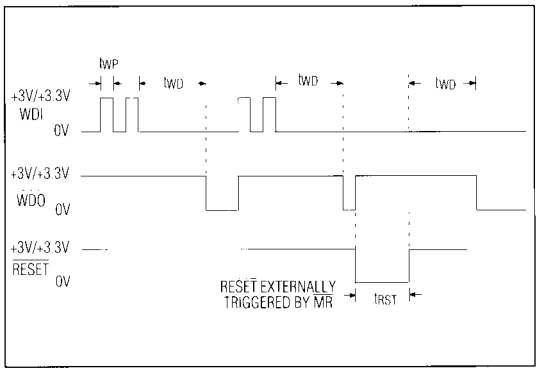
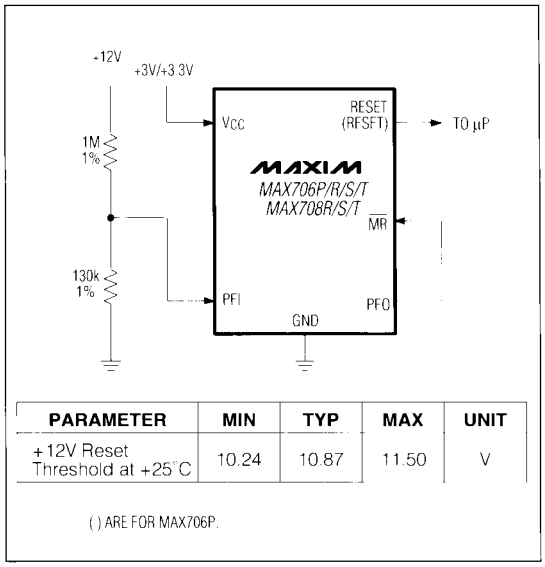


Figure 4. MAX706P/R/S/T Watchdog Timing

ble-instrument applications where power can be supplied from either a +3V battery or an AC-DC wall adapter that generates +5V (a +5V supply allows a µP or microcontroller to run faster than a +3V supply). With a +3V supply, these ICs consume less power, but output drive capability is reduced, the MR-to-RESET delay time increases, and the MR minimum pulse width increases. The *Electrical Characteristics* table provides specifications for operation with both +3V and +5V supplies.

Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX706R/S/T and MAX708R/S/T RESET output no longer sinks current; it becomes an open circuit. High-impedance, CMOS logic inputs can drift to undetermined voltages if left as open circuits. If a pull-down resistor is added to the RESET pin, as shown in Figure 6, any stray charge or leakage currents will flow to ground, holding RESET low. Resistor



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.24	10.87	11.50	V

( ) ARE FOR MAX706P.

Figure 5. Monitoring Both +3V/+3.3V and +12V

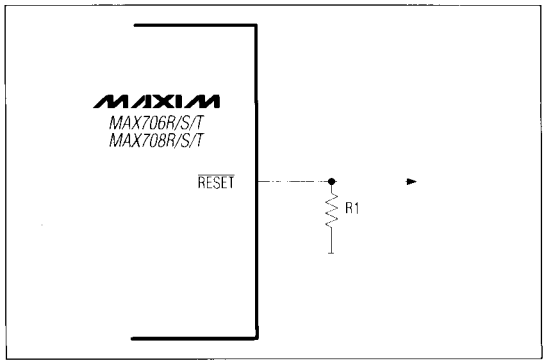


Figure 6. RESET Valid to Ground Circuit

value R1 is not critical, but it should not load RESET and should be small enough to pull RESET and the input it is driving to ground. 100kΩ is suggested for R1.

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when VIN is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI sees 1.25V when VIN falls to the desired trip point (VTRIP). Resistor R3 adds hysteresis. R3 will typically be an order of

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

magnitude greater than R1 or R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA max PFI input current does not shift the trip point significantly. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit of Figure 8. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

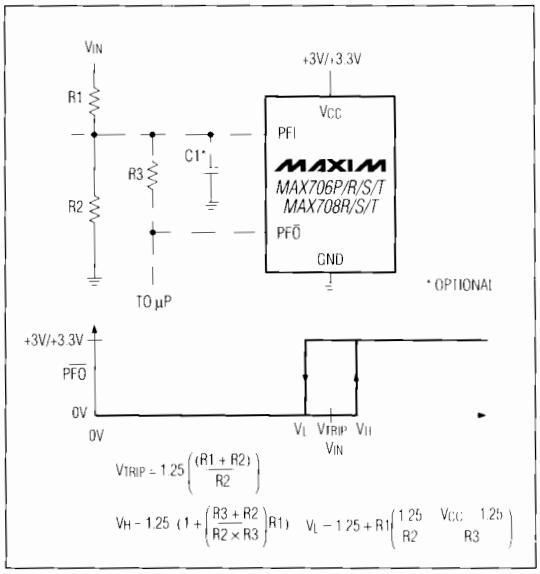


Figure 7. Adding Hysteresis to the Power-Fail Comparator

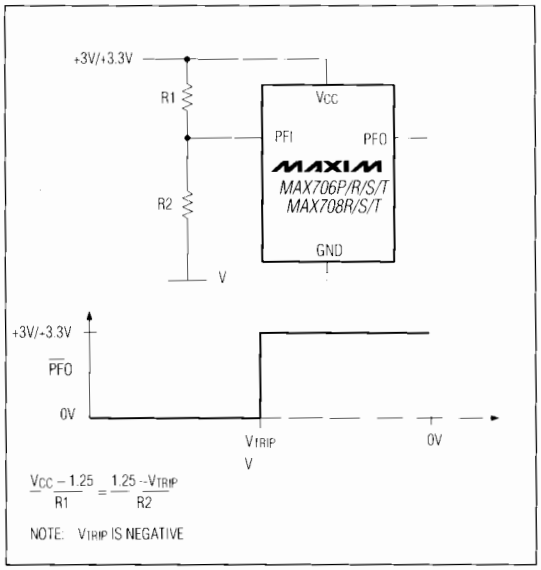
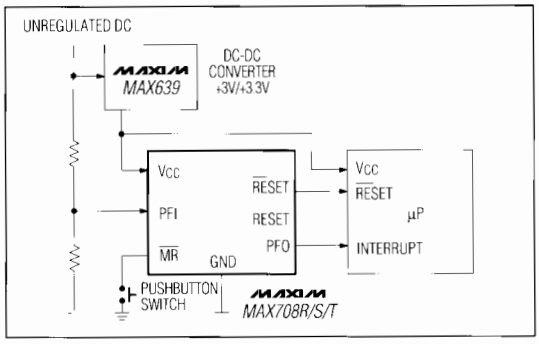


Figure 8. Monitoring a Negative Voltage

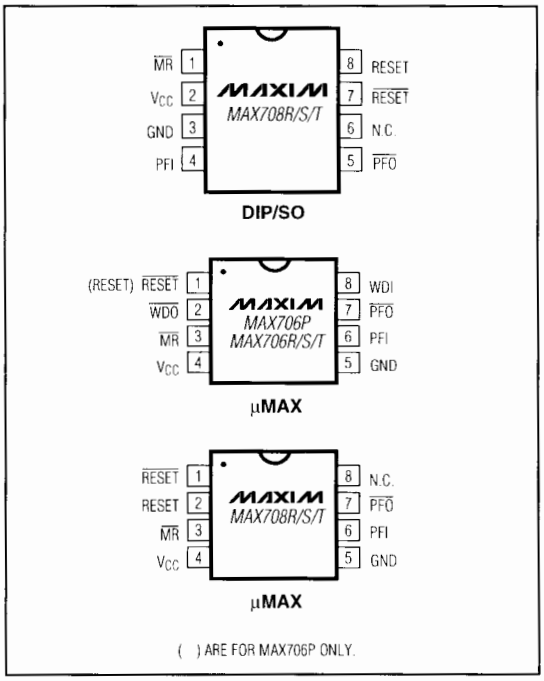
Typical Operating Circuits (continued)



Chip Information

TRANSISTOR COUNT: 572

Pin Configurations (continued)



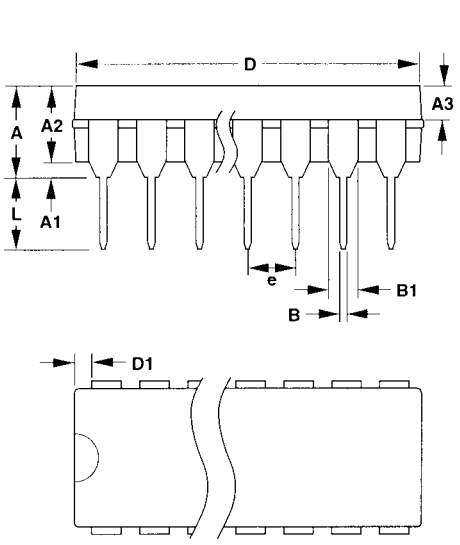
+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX706RCPA	0°C to +70°C	8 Plastic DIP
MAX706RCSA	0°C to +70°C	8 SO
MAX706RCUA	0°C to +70°C	8 µMAX
MAX706REPA	-40°C to +85°C	8 Plastic DIP
MAX706RESA	-40°C to +85°C	8 SO
MAX706RMJA	-55°C to +125°C	8 CERDIP*
MAX706SCPA	0°C to +70°C	8 Plastic DIP
MAX706SCSA	0°C to +70°C	8 SO
MAX706SCUA	0°C to +70°C	8 µMAX
MAX706SEPA	-40°C to +85°C	8 Plastic DIP
MAX706SESA	-40°C to +85°C	8 SO
MAX706SMJA	-55°C to +125°C	8 CERDIP*
MAX706TCPA	0°C to +70°C	8 Plastic DIP
MAX706TCSA	0°C to +70°C	8 SO
MAX706TCUA	0°C to +70°C	8 µMAX
MAX706TEPA	-40°C to +85°C	8 Plastic DIP
MAX706TESA	-40°C to +85°C	8 SO
MAX706TMJA	-55°C to +125°C	8 CERDIP*
MAX708RCPA	0°C to +70°C	8 Plastic DIP
MAX708RCSA	0°C to +70°C	8 SO
MAX708RCUA	0°C to +70°C	8 µMAX
MAX708REPA	-40°C to +85°C	8 Plastic DIP
MAX708RESA	-40°C to +85°C	8 SO
MAX708RMJA	-55°C to +125°C	8 CERDIP*
MAX708SCPA	0°C to +70°C	8 Plastic DIP
MAX708SCSA	0°C to +70°C	8 SO
MAX708SCUA	0°C to +70°C	8 µMAX
MAX708SEPA	-40°C to +85°C	8 Plastic DIP
MAX708SESA	-40°C to +85°C	8 SO
MAX708SMJA	-55°C to +125°C	8 CERDIP*
MAX708TCPA	0°C to +70°C	8 Plastic DIP
MAX708TCSA	0°C to +70°C	8 SO
MAX708TCUA	0°C to +70°C	8 µMAX
MAX708TEPA	-40°C to +85°C	8 Plastic DIP
MAX708TESA	-40°C to +85°C	8 SO
MAX708TMJA	-55°C to +125°C	8 CERDIP*

** Contact factory for availability and processing to MIL-STD-883.*

Package Information

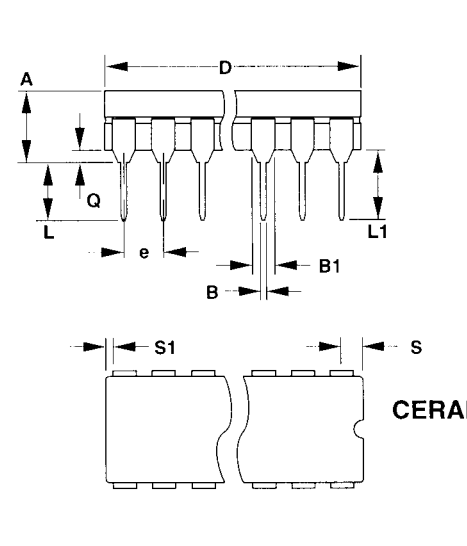


Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES		MILLIMETERS	
			MIN	MAX	MIN	MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A



CERDIP
CERAMIC DUAL-IN-LINE
PACKAGE
(0.300 in.)

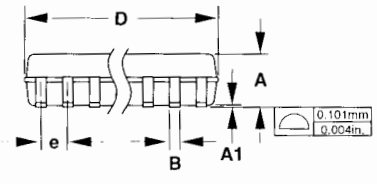
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

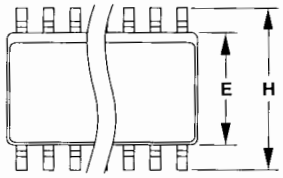
DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

21-0045A

+3V Voltage Monitoring, Low-Cost, µP Supervisory Circuits

Package Information (continued)



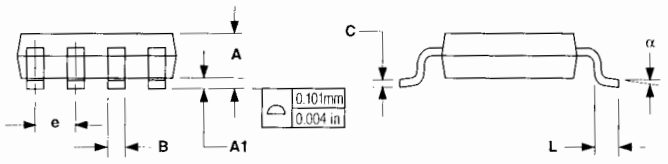


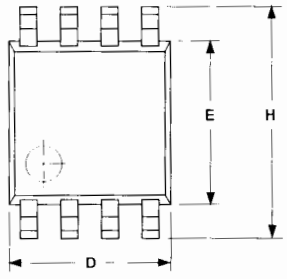
Narrow SO SMALL-OUTLINE PACKAGE (0.150 in.)

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A





8-PIN µMAX MICROMAX SMALL-OUTLINE PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
E	0.116	0.120	2.95	3.05
e	0.0256		0.65	
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

21-0036D