19-2829; Rev 1; 7/03

MAXIM

Anything-to-LVDS Dual 2 x 2 Crosspoint Switches

General Description

The MAX9390/MAX9391 dual 2 x 2 crosspoint switches perform high-speed, low-power, and low-noise signal distribution. The MAX9390/MAX9391 multiplex one of two differential input pairs to either or both low-voltage differential signaling (LVDS) outputs for each channel. Independent enable inputs turn on or turn off each differential output pair.

Four LVCMOS/LVTTL logic inputs (two per channel) control the internal connections between inputs and outputs. This flexibility allows for the following configurations: 2 x 2 crosspoint switch, 2:1 mux, 1:2 splitter, or dual repeater. This makes the MAX9390/MAX9391 ideal for protection switching in fault-tolerant systems, loopback switching for diagnostics, fanout buffering for clock/data distribution, and signal regeneration.

Fail-safe circuitry forces the outputs to a differential low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9390 provides high-level input fail-safe detection for LVDS, HSTL, and other GND-referenced differential inputs. The MAX9391 provides low-level input fail-safe detection for LVPECL, CML, and other V_{CC}-referenced differential inputs.

Ultra-low 82ps$_{(P-P)}$ (max) pseudorandom bit sequence (PRBS) jitter ensures reliable communications in high-speed links that are highly sensitive to timing error, especially those incorporating clock-and-data recovery, or serializers and deserializers. The high-speed switching performance guarantees 1.5GHz operation and less than 65ps (max) skew between channels.

LVDS inputs and outputs are compatible with the TIA/EIA-644 LVDS standard. The LVDS outputs drive 100Ω loads. The MAX9390/MAX9391 are offered in a 32-pin TQFP and 5mm x 5mm thin QFN package with exposed paddle and operate over the extended temperature range (-40°C to +85°C).

Also refer to the MAX9392/MAX9393 with flow-through pinout.

Applications

High-Speed Telecom/Datacom Equipment

Central-Office Backplane Clock Distribution

DSLAM

Protection Switching

Fault-Tolerant Systems

Functional Diagram and Typical Operating Circuit appear at end of data sheet.

Features

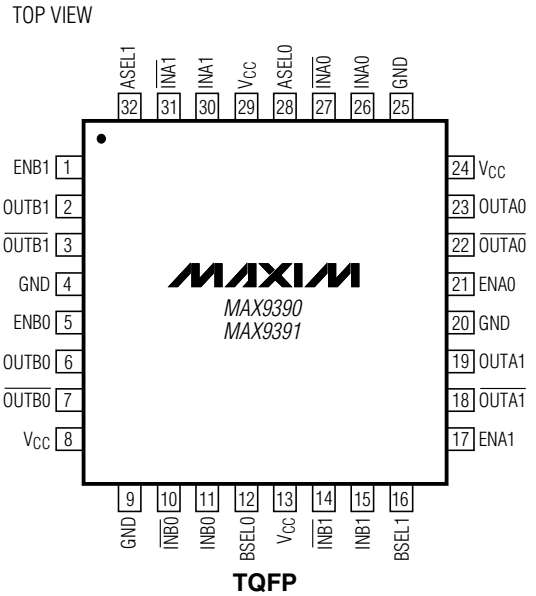
- **1.5GHz Operation with 250mV Differential Output Swing**
- **2ps$_{(RMS)}$ (max) Random Jitter**
- **AC Specifications Guaranteed for 150mV Differential Input**
- **Signal Inputs Accept Any Differential Signaling Standard**
- **LVDS Outputs for Clock or High-Speed Data**
- **High-Level Input Fail-Safe Detection (MAX9390)**
- **Low-Level Input Fail-Safe Detection (MAX9391)**
- **+3.0V to +3.6V Supply Voltage Range**
- **LVCMOS/LVTTL Logic Inputs Control Signal Routing**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9390EHJ	-40°C to +85°C	32 TQFP
MAX9390ETJ*	-40°C to +85°C	32 Thin QFN
MAX9391EHJ	-40°C to +85°C	32 TQFP
MAX9391ETJ*	-40°C to +85°C	32 Thin QFN

**Future product—contact factory for availability.*

Pin Configurations



Pin Configurations continued at end of data sheet.

Anything-to-LVDS Dual 2 x 2 Crosspoint Switches

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.1V
IN_ _, $\overline{IN\_\_}$, OUT_ _, $\overline{OUT\_\_}$, EN_ _, _SEL_ to GND.....-0.3V to (V_{CC} + 0.3V)
IN_ _ to $\overline{IN\_\_}$.....±3V
Short-Circuit Duration (OUT_ _, $\overline{OUT\_\_}$) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
32-Pin QFP (derate 13.1mW/°C above +70°C).....1047mW
32-Pin 5mm x 5mm Thin QFN (derate 21.3mW/°C above +70°C).....1702mW
Junction-to-Ambient Thermal Resistance in Still Air
32-Pin QFP.....+76.4°C/W
32-Pin 5mm x 5mm Thin QFN.....+47°C/W
Junction-to-Case Thermal Resistance
32-Pin 5mm x 5mm Thin QFN.....+2°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection (Human Body Model)
(IN_ _, $\overline{IN\_\_}$, OUT_ _, $\overline{OUT\_\_}$, EN_ _, SEL_ _) .....±2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, EN_ _ = V_{CC}, V_{CM} = 0.05V to (V_{CC} - 0.6V) (MAX9390), V_{CM} = 0.6V to (V_{CC} - 0.05V) (MAX9391) T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVCMOS/LVTTL INPUTS (EN_ _, _SEL_)							
Input High Voltage	V_{IH}			2.0		V_{CC}	V
Input Low Voltage	V_{IL}			0		0.8	V
Input High Current	I_{IH}	V_{IN} = +2.0V to V_{CC}		0		20	µA
Input Low Current	I_{IL}	V_{IN} = 0 to +0.8V		0		10	µA
DIFFERENTIAL INPUTS (IN_ _, $\overline{IN\_\_}$)							
Differential Input Voltage	V_{ID}	$V_{ILD} \geq 0$ and $V_{IHD} \leq V_{CC}$, Figure 1		0.1		3.0	V
Input Common-Mode Range	V_{CM}	MAX9390		0.05		V_{CC} - 0.6	V
		MAX9391		0.6		V_{CC} - 0.05	
Input Current	$I_{IN\_\_}$, $I_{\overline{IN\_\_}}$	MAX9390	$\|V_{ID}\| \leq 3.0V$	-75		+10	µA
		MAX9391	$\|V_{ID}\| \leq 3.0V$	-10		+100	
LVDS OUTPUTS (OUT_ _, $\overline{OUT\_\_}$)							
Differential Output Voltage	V_{OD}	R_L = 100Ω, Figure 2		250	350	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	ΔV_{OD}	Figure 2			1.0	50	mV
Offset Common-Mode Voltage	V_{OS}	Figure 2		1.125	1.25	1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	ΔV_{OS}	Figure 2			1.0	50	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, EN_ _ = V_{CC}, V_{CM} = 0.05V to (V_{CC} - 0.6V) (MAX9390), V_{CM} = 0.6V to (V_{CC} - 0.05V) (MAX9391) T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, T_A = +25°C.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current (Either Output Shorted to GND)	$\|I_{OS}\|$	V_{ID} = ±100mV (Note 4)	$V_{OUT\_\_}$ or $V_{\overline{OUT\_\_}}$ = 0		30	40	mA
			$V_{OUT\_\_}$ = $V_{\overline{OUT\_\_}}$ = 0		18	24	
Output Short-Circuit Current (Outputs Shorted Together)	$\|I_{OSB}\|$	V_{ID} = ±100mV, $V_{OUT\_\_}$ = $V_{\overline{OUT\_\_}}$ (Note 4)			5.0	12	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	R_L = 100Ω, EN_ _ = V_{CC}			68	98	mA
		R_L = 100Ω, EN_ _ = V_{CC}, switching at 670MHz (1.34Gbps)			68	98	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, $f_{IN} \le$ 1.34GHz, t_{R_IN} = t_{F_IN} = 125ps, R_L = 100Ω ±1%, $|V_{ID}| \ge$ 150mV, V_{CM} = +0.075V to (V_{CC} - 0.6V) (MAX9390 only), V_{CM} = +0.6V to (V_{CC} - 0.075V) (MAX9391 only), EN_ _ = V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, f_{IN} = 1.34GHz, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SEL to Switched Output	t_{SWITCH}	Figure 3			1.1	ns
Disable, Time to Differential Output Low	t_{PHD}	Figure 4			1.7	ns
Enable, Time to Differential Output High	t_{PDH}	Figure 4			1.7	ns
Switching Frequency	f_{MAX}	$V_{OD} \ge$ 250mV	1.50	2.20		GHz
Low-to-High Propagation Delay	t_{PLH}	Figures 1, 5	294	409	565	ps
High-to-Low Propagation Delay	t_{PHL}	Figures 1, 5	286	402	530	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figures 1, 5 (Note 6)		7	97	ps
Output-to-Output Skew	t_{CCS}	Figures 5, 6 (Note 7)		10	65	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	Figures 1, 5; f_{IN} = 100MHz	112	153	185	ps
Output High-to-Low Transition Time (80% to 20%)	t_F	Figures 1, 5; f_{IN} = 100MHz	112	153	185	ps
Added Random Jitter	t_{RJ}	$f_{IN\_\_}$ = 1.34GHz, clock pattern (Note 8)			2	$ps_{(RMS)}$
Added Deterministic Jitter	t_{DJ}	1.34Gbps, 2^{23} - 1 PRBS (Note 8)		55	82	$ps_{(P-P)}$

Note 1: Measurements obtained with the device in thermal equilibrium. All voltages referenced to GND except V_{ID}, V_{OD}, and ΔV_{OD}.
Note 2: Current into the device defined as positive. Current out of the device defined as negative.
Note 3: DC parameters tested at T_A = +25°C and guaranteed by design and characterization for T_A = -40°C to +85°C.
Note 4: Current through either output.
Note 5: Guaranteed by design and characterization. Limits set at ±6 sigma.
Note 6: t_{SKEW} is the magnitude difference of differential propagation delays for the same output over same conditions. $t_{SKEW} = |t_{PHL} - t_{PLH}|$.
Note 7: Measured between outputs of the same device at the signal crossing points for a same-edge transition, under the same conditions.
Note 8: Device jitter added to the differential input signal.

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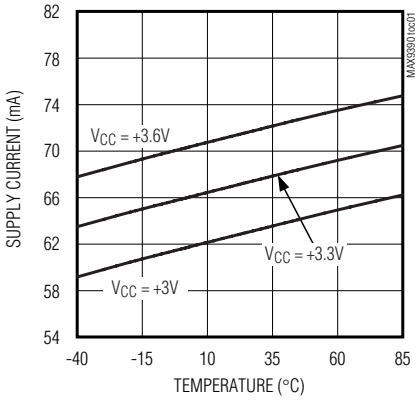
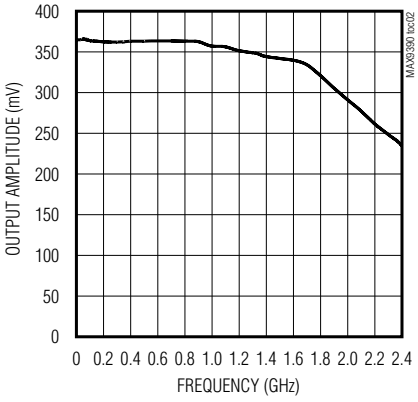
Typical Operating Characteristics

(V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.2V, f_{IN} = 1.34GHz, T_A = +25°C.)

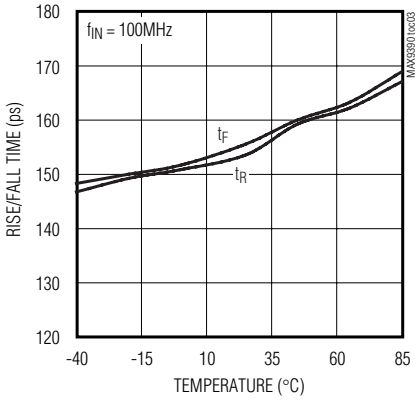
SUPPLY CURRENT vs. TEMPERATURE



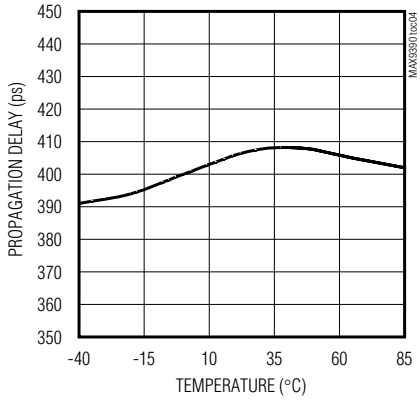
OUTPUT AMPLITUDE vs. FREQUENCY



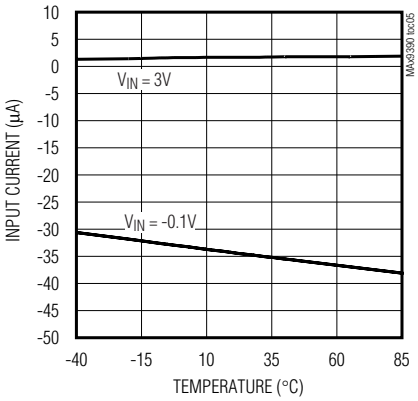
OUTPUT RISE AND FALL TIMES vs. TEMPERATURE



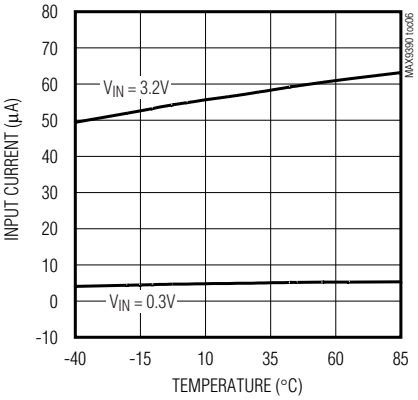
PROPAGATION DELAY vs. TEMPERATURE



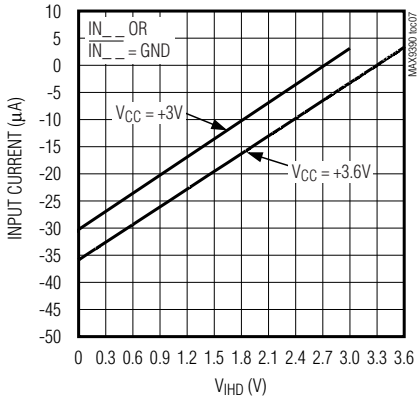
MAX9390 DIFFERENTIAL INPUT CURRENT vs. TEMPERATURE



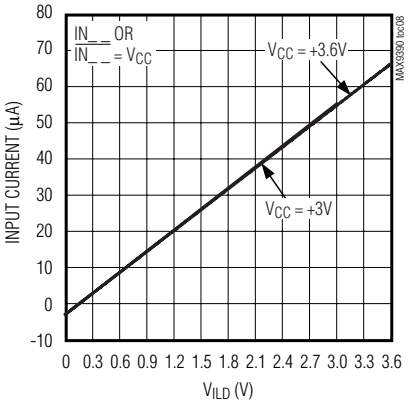
MAX9391 DIFFERENTIAL INPUT CURRENT vs. TEMPERATURE



MAX9390 INPUT CURRENT vs. V_{IHD}



MAX9391 DIFFERENTIAL INPUT CURRENT vs. V_{ILD}



Pin Description

PIN	NAME	FUNCTION
1	ENB1	B1 Output Enable. Drive ENB1 high to enable the B1 LVDS outputs. An internal 435kΩ resistor pulls ENB1 low when unconnected.
2	OUTB1	B1 LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTB1 and $\overline{OUTB1}$ at the receiver inputs to ensure proper operation.
3	$\overline{OUTB1}$	B1 LVDS Inverting Output. Connect a 100Ω termination resistor between OUTB1 and $\overline{OUTB1}$ at the receiver inputs to ensure proper operation.
4, 9, 20, 25	GND	Ground
5	ENB0	B0 Output Enable. Drive ENB0 high to enable the B0 LVDS outputs. An internal 435kΩ resistor pulls ENB0 low when unconnected.
6	OUTB0	B0 LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTB0 and $\overline{OUTB0}$ at the receiver inputs to ensure proper operation.
7	$\overline{OUTB0}$	B0 LVDS Inverting Output. Connect a 100Ω termination resistor between OUTB0 and $\overline{OUTB0}$ at the receiver inputs to ensure proper operation.
8, 13, 24, 29	V_{CC}	Power-Supply Input. Bypass each V_{CC} to GND with 0. 1µF and 0.01µF ceramic capacitors. Install both bypass capacitors as close to the device as possible, with the 0.01µF capacitor closest to the device.
10	$\overline{INB0}$	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Inverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
11	INB0	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Noninverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
12	BSEL0	Input Select for B0 Output. Selects the differential input to reproduce at the B0 differential outputs. Connect BSEL0 to GND or leave open to select the INB0 ($\overline{INB0}$) set of inputs. Connect BSEL0 to V_{CC} to select the INB1 ($\overline{INB1}$) set of inputs. An internal 435kΩ resistor pulls BSEL0 low when unconnected.
14	$\overline{INB1}$	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Inverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
15	INB1	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Noninverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
16	BSEL1	Input Select for B1 Output. Selects the differential input to reproduce at the B1 differential outputs. Connect BSEL1 to GND or leave open to select the INB0 ($\overline{INB0}$) set of inputs. Connect BSEL1 to V_{CC} to select the INB1 ($\overline{INB1}$) set of inputs. An internal 435kΩ resistor pulls BSEL1 low when unconnected.

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Pin Description (continued)

PIN	NAME	FUNCTION
17	ENA1	A1 Output Enable. Drive ENA1 high to enable the A1 LVDS outputs. An internal 435kΩ resistor pulls ENA1 low when unconnected.
18	$\overline{OUTA1}$	A1 LVDS Inverting Output. Connect a 100Ω termination resistor between OUTA1 and $\overline{OUTA1}$ at the receiver inputs to ensure proper operation.
19	OUTA1	A1 LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTA1 and $\overline{OUTA1}$ at the receiver inputs to ensure proper operation.
21	ENA0	A0 Output Enable. Drive ENA0 high to enable the A0 LVDS outputs. An internal 435kΩ resistor pulls ENA0 low when unconnected.
22	$\overline{OUTA0}$	A0 LVDS Inverting Output. Connect a 100Ω termination resistor between OUTA0 and $\overline{OUTA0}$ at the receiver inputs to ensure proper operation.
23	OUTA0	A0 LVDS Noninverting Output. Connect a 100Ω termination resistor between OUTA0 and $\overline{OUTA0}$ at the receiver inputs to ensure proper operation.
26	INA0	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Noninverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
27	$\overline{INA0}$	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Inverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
28	ASEL0	Input Select for A0 Output. Selects the differential input to reproduce at the A0 differential outputs. Connect ASEL0 to GND or leave open to select the INA0 ($\overline{INA0}$) set of inputs. Connect ASEL0 to V_{CC} to select the INA1 ($\overline{INA1}$) set of inputs. An internal 435kΩ resistor pulls ASEL0 low when unconnected.
30	INA1	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Noninverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
31	$\overline{INA1}$	LVDS/HSTL (MAX9390) or LVPECL/CML (MAX9391) Inverting Input. An internal 128kΩ resistor to V_{CC} pulls the input high when unconnected (MAX9390). An internal 68kΩ resistor to GND pulls the input low when unconnected (MAX9391).
32	ASEL1	Input Select for A1 Output. Selects the differential input to reproduce at the A1 differential outputs. Connect ASEL1 to GND or leave open to select the INA0 ($\overline{INA0}$) set of inputs. Connect ASEL1 to V_{CC} to select the INA1 ($\overline{INA1}$) set of inputs. An internal 435kΩ resistor pulls ASEL1 low when unconnected.
—	EP	Exposed Paddle (QFN Package Only). Connect to GND for optimal thermal and EMI characteristics.

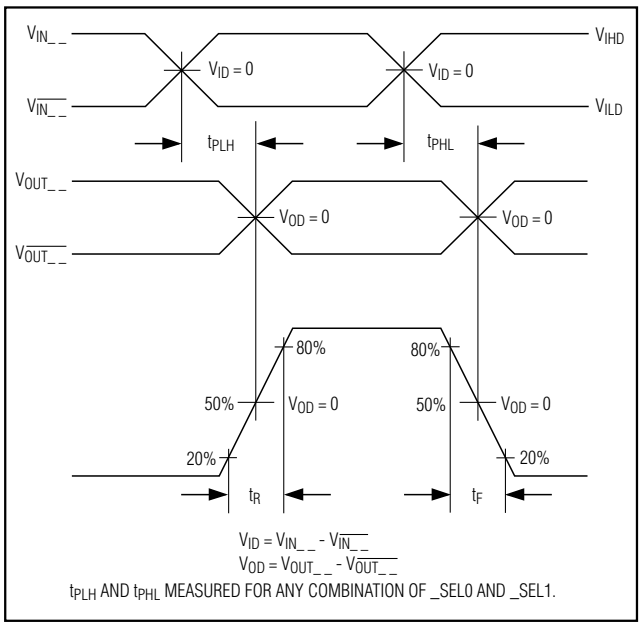


Figure 1. Output Transition Time and Propagation Delay Timing Diagram

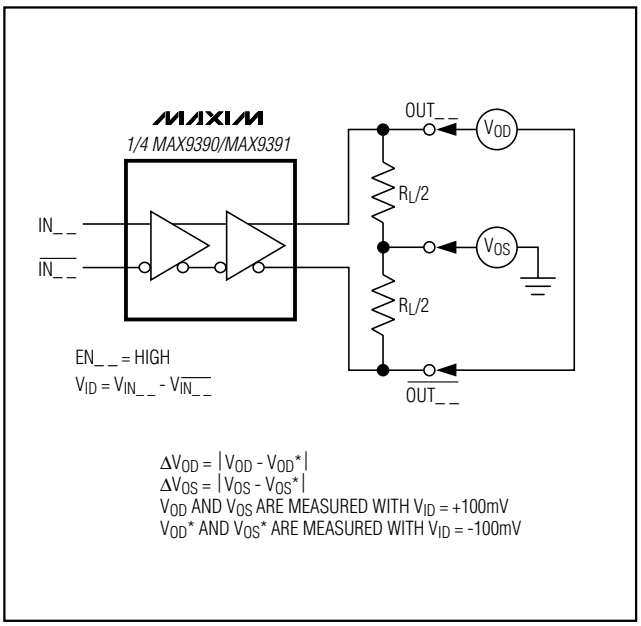


Figure 2. Test Circuit for V_{OD} and V_{OS}

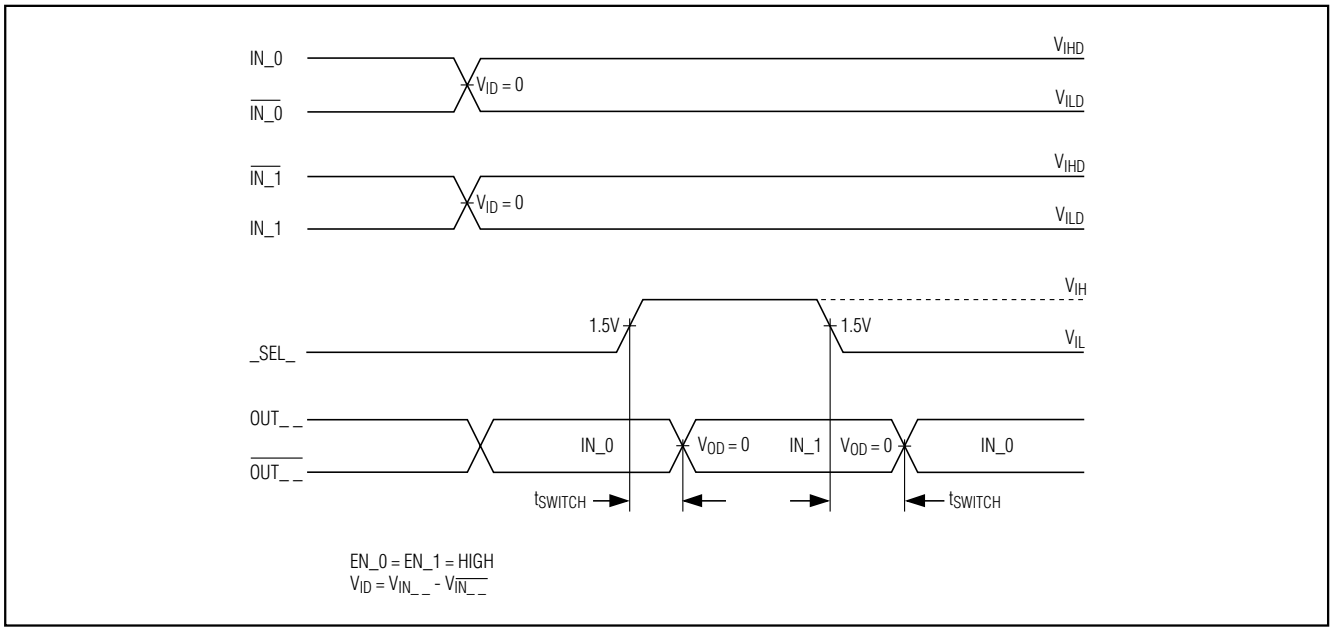


Figure 3. Input to Rising/Falling Edge Select and Mux Switch Timing Diagram

Anything-to-LVDS Dual 2 x 2 Crosspoint Switches

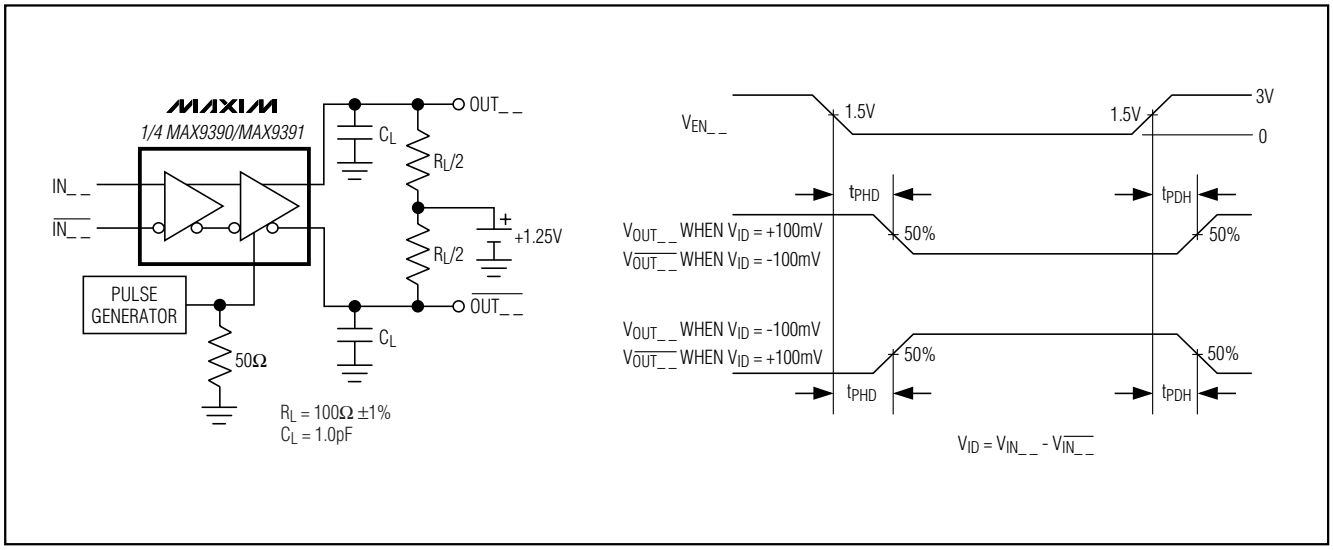


Figure 4. Output Active-to-Disable and Disable-to-Active Test Circuit and Timing Diagram

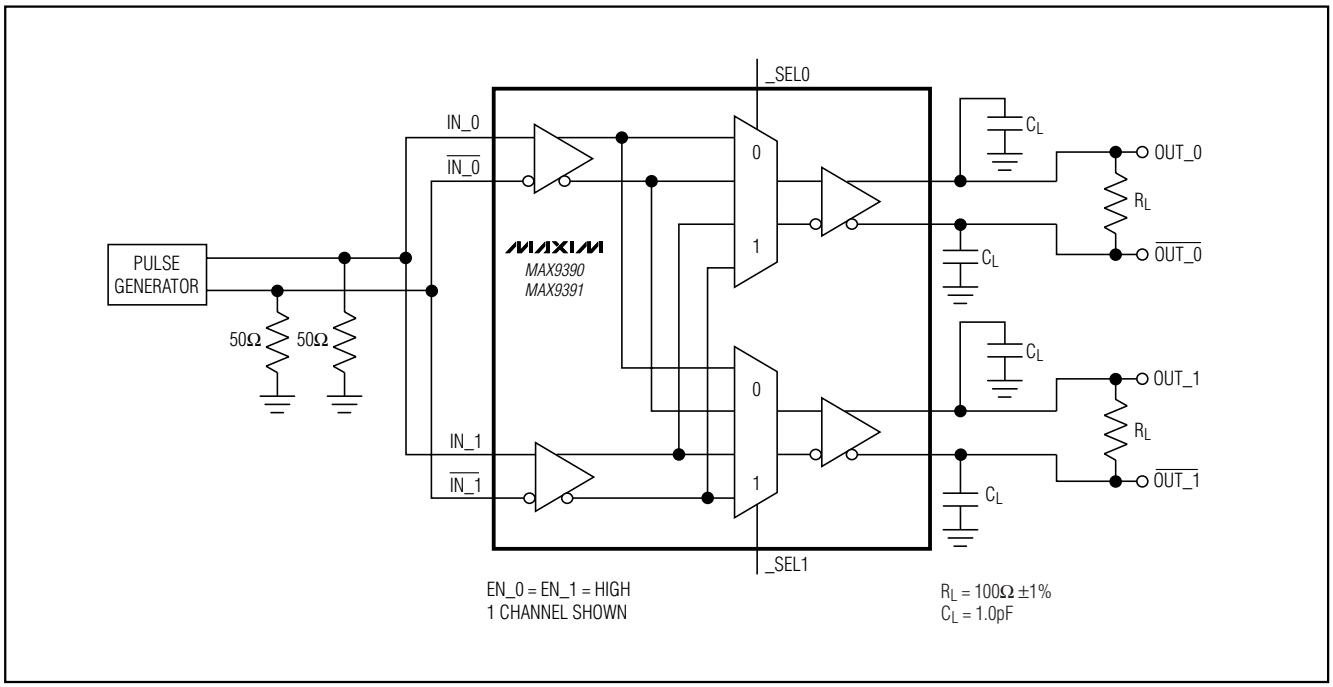


Figure 5. Output Transition Time, Propagation Delay, and Output Channel-to-Channel Skew Test Circuit

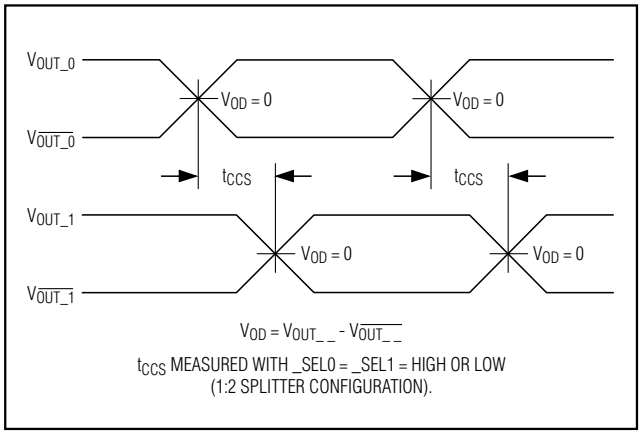


Figure 6. Output Channel-to-Channel Skew

Detailed Description

The LVDS interface standard provides a signaling method for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 standard. LVDS utilizes a lower voltage swing than other communication standards, achieving higher data rates with reduced power consumption, while reducing EMI emissions and system susceptibility to noise.

The MAX9390/MAX9391 1.5GHz dual 2 x 2 crosspoint switches optimize high-speed, low-power, point-to-point interfaces. The MAX9390 accepts LVDS and HSTL signals, while the MAX9391 accepts LVPECL and CML signals. Both devices route the input signals to either or both LVDS outputs.

When configured as a 1:2 splitter, the outputs repeat the selected inputs. This configuration creates copies of signals for protection switching. When configured as a repeater, the device operates as a two-channel buffer. Repeating restores signal amplitude, allowing isolation of media segments or longer media drive. When configured as a 2:1 mux, select primary or backup signals to provide a protection-switched, fault-tolerant application.

Input Fail-Safe

The differential inputs of the MAX9390/MAX9391 possess internal fail-safe protection. Fail-safe circuitry forces the outputs to a differential low condition for undriven inputs or when the common-mode voltage exceeds the specified range. The MAX9390 provides high-level input fail-safe detection for LVDS, HSTL, and other GND-referenced differential inputs. The MAX9391 provides low-level input fail-safe detection for LVPECL, CML, and other V_{CC}-referenced differential inputs.

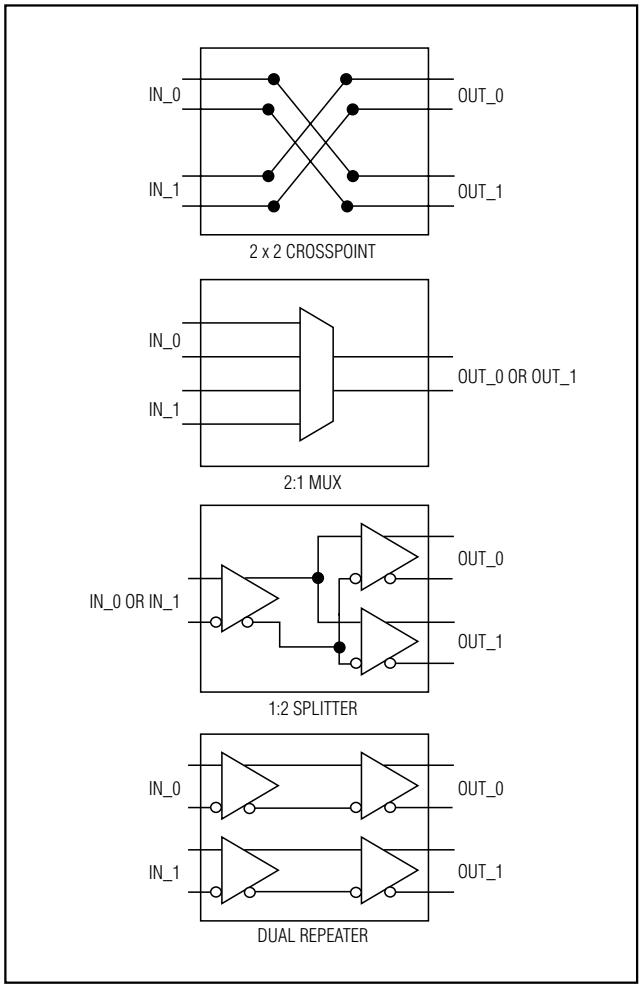


Figure 7. Programmable Configurations

Select Function

The _SEL_ logic inputs control the input and output signal connections. Two logic inputs control the signal routing for each channel. _SEL0 and _SEL1 allow the devices to be configured as a differential crosspoint switch, 2:1 mux, dual repeater, or 1:2 splitter (Figure 7). See Table 1 for mode-selection settings (insert A or B for the _). Channels A and B possess separate select inputs, allowing different configurations for each channel.

Enable Function

The EN_ _ logic inputs enable and disable each set of differential outputs. Connect EN_ 0 to V_{CC} to enable the OUT_0/$\overline{OUT\_0}$ differential output pair. Connect EN_0 to GND to disable the OUT_0/$\overline{OUT\_0}$ differential output pair. The differential output pairs assert to a differential low condition when disabled.

Anything-to-LVDS Dual 2 x 2 Crosspoint Switches

Table 1. Input/Output Function Table

_SEL0	_SEL1	OUT_0 / $\overline{OUT}$_0	OUT_1 / $\overline{OUT}$_1	MODE
0	0	IN_0 / $\overline{IN}$_0	IN_0 / $\overline{IN}$_0	1:2 splitter
0	1	IN_0 / $\overline{IN}$_0	IN_1 / $\overline{IN}$_1	Repeater
1	0	IN_1 / $\overline{IN}$_1	IN_0 / $\overline{IN}$_0	Switch
1	1	IN_1 / $\overline{IN}$_1	IN_1 / $\overline{IN}$_1	1:2 splitter

Applications Information

Differential Inputs

The MAX9390/MAX9391 inputs accept any differential signaling standard within the specified common-mode voltage range. The fail-safe feature detects common-mode input signal levels and generates a differential output low condition for undriven inputs or when the common-mode voltage exceeds the specified range. Leave unused inputs unconnected or connect to V_{CC} for the MAX9390 or to GND for the MAX9391.

Expanding the Number of LVDS Output Ports

Cascade devices to make larger switches. Consider the total propagation delay and total jitter when determining the maximum allowable switch size.

Power-Supply Bypassing

Bypass each V_{CC} to GND with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors in parallel as close to the device as possible. Install the 0.01µF capacitor closest to the device.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9390/MAX9391. Connect each input and output to a 50Ω characteristic impedance trace. Maintain the distance between differential traces and eliminate sharp corners to avoid discontinuities in differential impedance and maximize common-mode noise immunity. Minimize the number of vias on the differential input and output traces to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Output Termination

Terminate LVDS outputs with a 100Ω resistor between the differential outputs at the receiver inputs. LVDS outputs require 100Ω termination for proper operation.

Ensure that the output currents do not exceed the current limits specified in the *Absolute Maximum Ratings*. Observe the total thermal limits of the MAX9390/MAX9391 under all operating conditions.

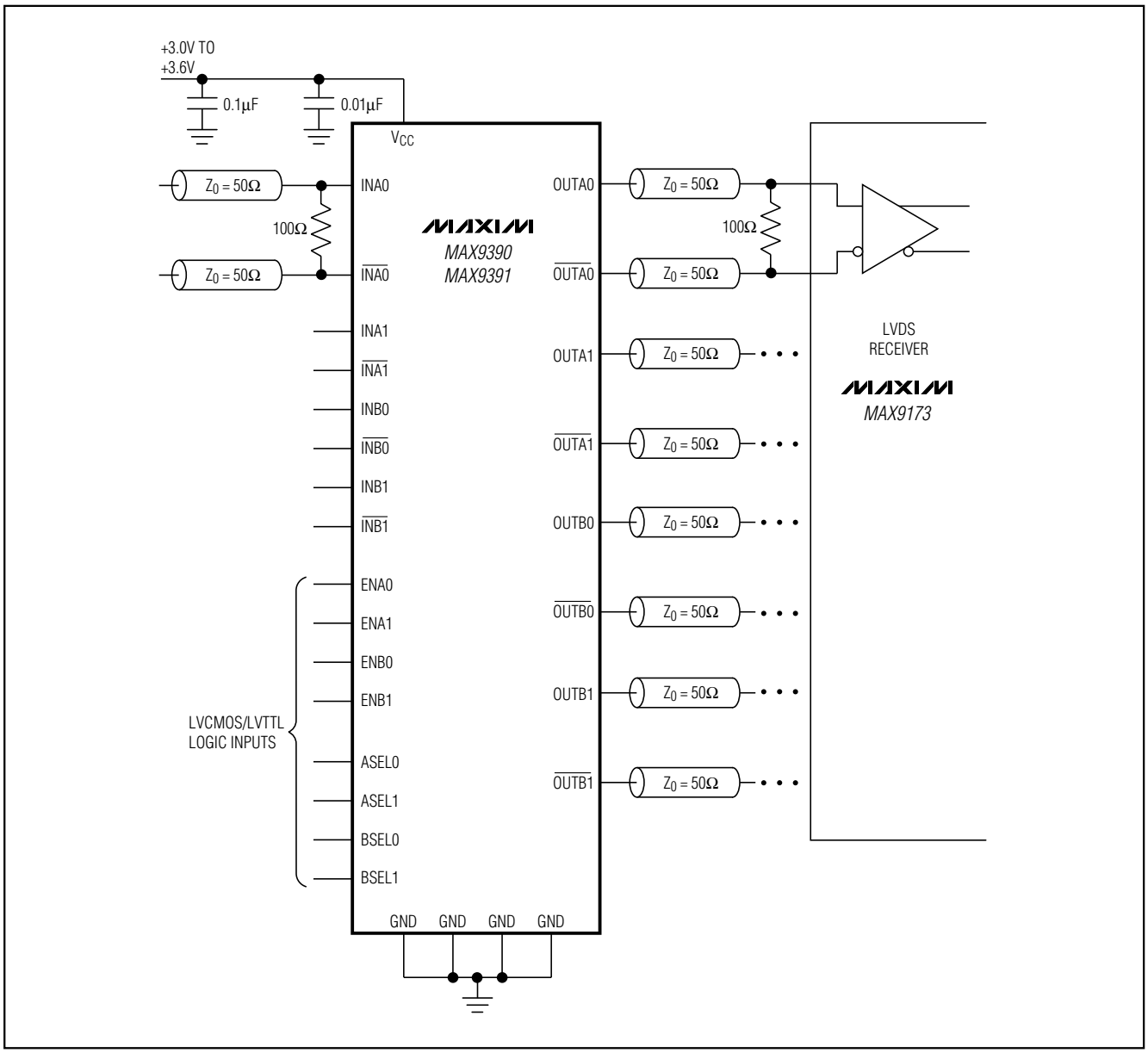
Cables and Connectors

Use matched differential impedance for transmission media. Use cables and connectors with matched differential impedance to minimize impedance discontinuities. Avoid the use of unbalanced cables. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects.

Board Layout

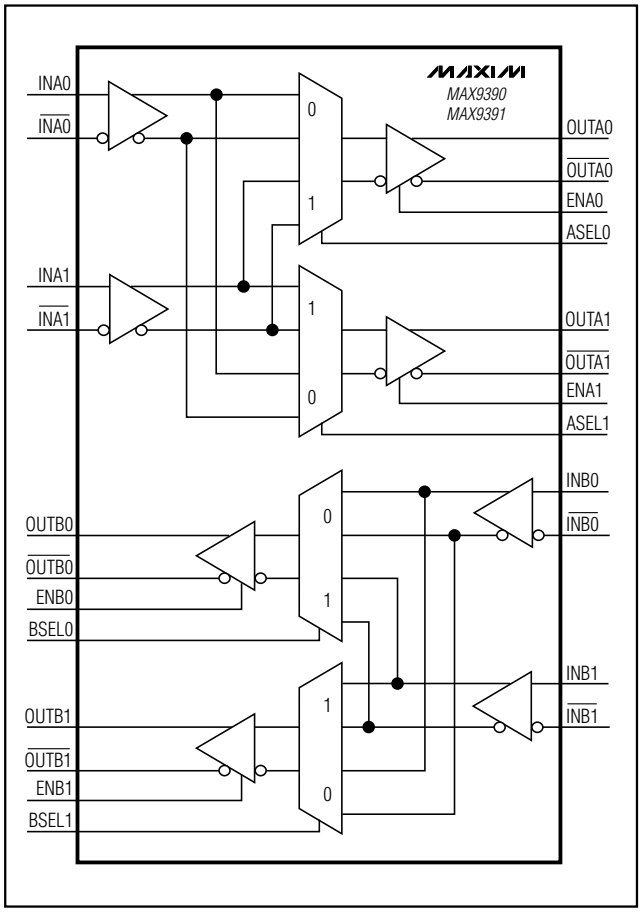
Use a four-layer printed circuit (PC) board providing separate signal, power, and ground planes for high-speed signaling applications. Bypass V_{CC} to GND as close to the device as possible. Install termination resistors as close to receiver inputs as possible. Match the electrical length of the differential traces to minimize signal skew.

Typical Operating Circuit

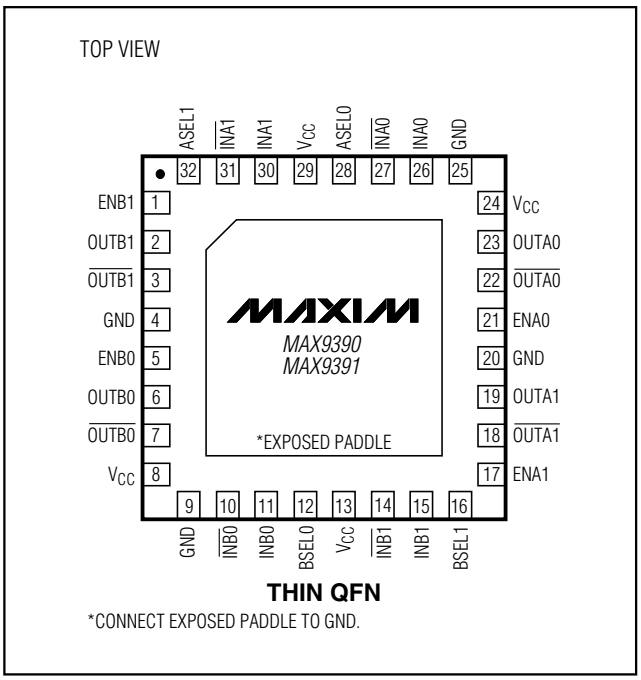


Anything-to-LVDS Dual 2 x 2 Crosspoint Switches

Functional Diagram



Pin Configurations (continued)



Chip Information

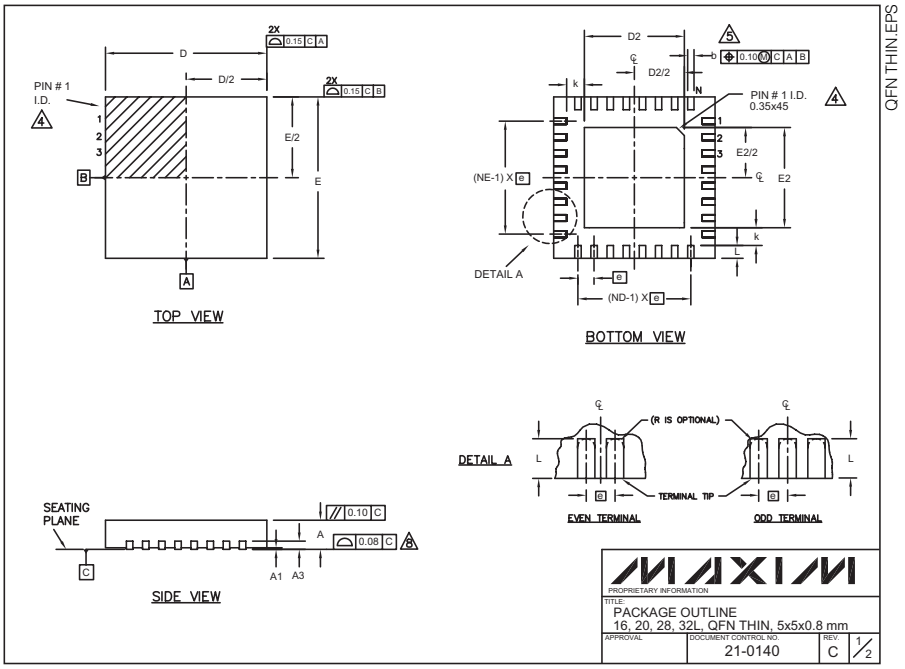
TRANSISTOR COUNT: 1565

PROCESS: Bipolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

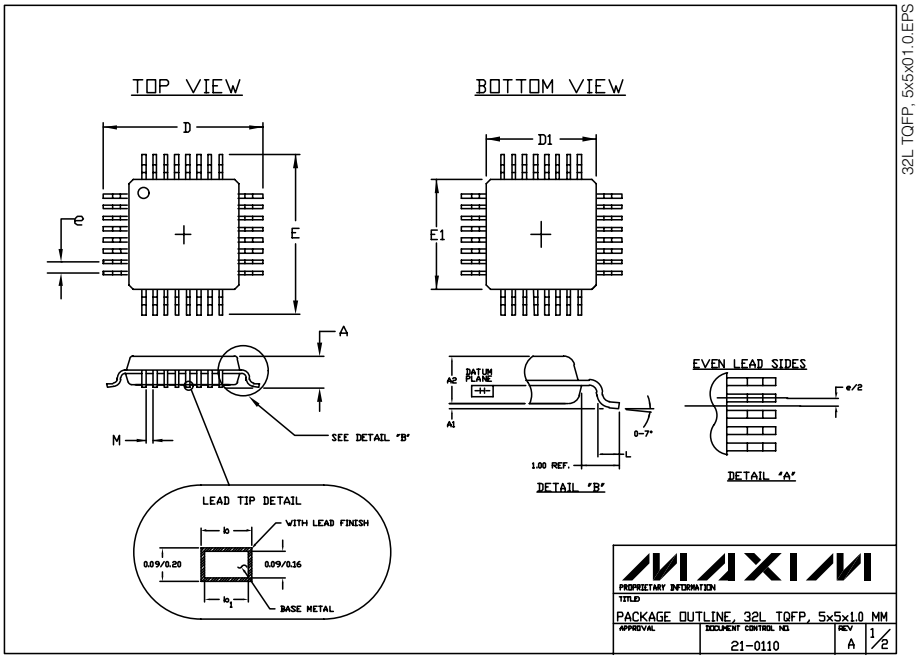
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0140
REV.
C
2/2

Anything-to-LVDS Dual 2 x 2 Crosspoint Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS	
	DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~~	1.20
A1	0.05	0.15
A2	0.95	1.05
D	7.00 BSC.	
D1	5.00 BSC.	
E	7.00 BSC.	
E1	5.00 BSC.	
L	0.45	0.75
M	0.15	~~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0110
REV
A
2/2