## MB508

### 2.3GHz TWO MODULUS PRESCALER

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The Fujitsu MB508 is a 2.3 GHz two modulus prescaler used with a frequency synthesizer to form a Phase Locked Loop (PLL) and divides the input frequency by a modulus of $128 / 130,256 / 258$ or $512 / 514$. The output level is 1.6 V peak to peak ECL level. The ultra high frequency operation provides wide application, such as Direct Broadcasting Satellite System, CATV system, UHF Transceiver, etc.

## FEATURES

- High Frequency Operation:
- Input Signal Amplitude:
- Pulse Swallow Function: 128/130, 256/258, 512/514
- Power Dissipation: 120mW typ.
- Wide Operation Temperature: $-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$
- Stable Output Amplitude: $\quad \mathrm{V}_{\text {OUT }}=1.6 \mathrm{~V}_{\mathrm{p}-\mathrm{p}}$ typ.
- Complete PLL synthesizer circuit with the Fujitsu MB87001A, PLL synthesizer system block IC
- Standard Plastic 8-pin Dual-In-Line Package or Flat Package


## ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating | Symbol | Value | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | -0.5 to +7.0 | V |
| Input Voltage | $\mathrm{V}_{\mathrm{IN}}$ | -0.5 to $\mathrm{V}_{\mathrm{CC}}$ | V |
| Output Current | $\mathrm{I}_{\mathrm{O}}$ | 10 | mA |
| Operating Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |
| Storage Temperature | $\mathrm{T}_{\mathrm{STG}}$ | -55 to +125 | ${ }^{\circ} \mathrm{C}$ |

Note: Permanentdevice damage may occurifthe above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.


## PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.


Figure 1. MB508 Block Diagram

## PIN DESCRIPTION

| Pin Number | Symbol |  |
| :---: | :---: | :--- |
| 1 | IN | Input |
| 2 | V $_{\text {CC }}$ | Powercriptions |
| 3 | SW1 | Divide Ratio Control Input (See Divide Ratio Table) |
| 4 | OUT | Output |
| 5 | GND | Ground |
| 6 | MC | Modulus Control Input (See Divide Ratio Table) |
| 7 | SW2 | Divide Ratio Control Input (See Divide Ratio Table) |
| 8 | $\mathbb{N}$ | Complementary Input |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Values |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min. | Typ. | Max. |  |
| Power Supply Voltage | $\mathrm{V}_{\mathrm{CC}}$ | 4.5 | 5.0 | 5.5 | V |
| Output Current | lo |  | 1.2 |  | mA |
| Operating Temperature | $\mathrm{T}_{\mathrm{A}}$ | -40 |  | +85 | ${ }^{\circ} \mathrm{C}$ |
| Load Capacitance | $\mathrm{C}_{\mathrm{L}}$ |  |  | 12 | pF |

## ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

| Parameter | Symbol | Condition | Values |  |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min. | Typ. | Max. |  |
| Power Supply Current | ICC |  |  | 24 |  | mA |
| Output Amplitude | $\mathrm{V}_{\mathrm{O}}$ |  | 1.0 | 1.6 |  | $V_{p-p}$ |
| Input Frequency | $\mathrm{f}_{\mathrm{IN}}$ | with input coupling capacitor 1000pF | 100 |  | 2300 | MHz |
| Input Signal Amplitude | Pina | $\begin{gathered} \mathrm{f}_{\mathrm{IN}}=1800 \mathrm{MHz} \text { to } \\ 2300 \mathrm{MHz} \end{gathered}$ | -4 |  | 5.5 | dBm |
|  | $\mathrm{P}_{\text {INB }}$ | $\begin{gathered} \mathrm{f}_{\mathrm{IN}}=100 \mathrm{MHz} \text { to } \\ 1800 \mathrm{MHz} \end{gathered}$ | -16 |  | 10 |  |
| High Level Input Voltage for MC | $\mathrm{V}_{\text {IHM }}$ |  | 2.0 |  |  | V |
| Low Level Input Voltage for MC | $\mathrm{V}_{\text {ILM }}$ |  |  |  | 0.8 | V |
| High Level Input Voltage for SW | $\mathrm{V}_{\mathrm{IHS}}{ }^{\text {* }}$ |  | $V_{C C}-0.1$ | $\mathrm{V}_{\mathrm{Cc}}$ | $\mathrm{V}_{C C}+0.1$ | V |
| Low Level Input Voltage for SW | $\mathrm{V}_{\text {ILS }}$ |  | Open |  |  | V |
| High Level Input Current for MC | IIHM | $\mathrm{V}_{\mathrm{IH}}=2.0 \mathrm{~V}$ |  |  | 0.4 | mA |
| Low Level Input Current for MC | $I_{\text {ILM }}$ | $\mathrm{V}_{\mathrm{IL}}=0.8 \mathrm{~V}$ | -0.2 |  |  | mA |
| High Level Input Current for SW | $\mathrm{I}_{\text {IHS }}$ | $\mathrm{V}_{\mathrm{IH}}=\mathrm{V}_{\mathrm{CC}}$ |  |  | 250 | $\mu \mathrm{A}$ |
| Modulus Set-up Time MC to Output at 2.3 GHz Operation | ${ }_{\text {t }}$ SET |  |  | 18 | 28 | ns |

Note: *Design Guarantee


Figure 2. Test Circuit

## TIMING CHART (2 MODULUS)

Example: Divide ratio = 128/130


Note: When divide of 130 is selected, positive pulse is applied by two to 66 .
The typical set up time is 18 ns from the MC signal input to the timing of change of prescaler divide ratio.


Figure 3. Input Signal Amplitude vs. Input Frequency


Figure 4. Typical Application Example

## PACKAGE DIMENSIONS

(Suffix: -P)

## 8-LEAD PLASTIC DUAL IN-LINE PACKAGE <br> (CASE No: DIP-08P-M01)



## PACKAGE DIMENSIONS (Continued)

## (Suffix: -PF)

## 8-LEAD PLASTIC FLAT PACKAGE

 (CASE No: FPT-08P-M01)

Dlmensions in inches (millimeters)

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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Complete information sufficient for construction purposes is not necessarily given.

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