FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-13104-1E

*Memory FRAM*

**CMOS**

# 1 M Bit (64 K×16)

# MB85R1002

## ■ DESCRIPTIONS

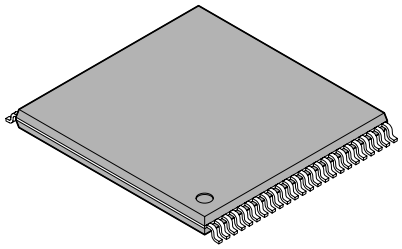
The MB85R1002 is an FRAM (Ferroelectric Random Access Memory) chip in a configuration of 65,536 words x 16 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
Unlike SRAM, MB85R1002 is able to retain data without back-up battery.
The memory cells used for the MB85R1002 has improved at least $10^{10}$ times of read/write access, significantly outperforming FLASH memory and $E^2$PROM in endurance.
The MB85R1002 uses a pseudo - SRAM interface compatible with conventional asynchronous SRAM.

## ■ FEATURES

- Bit configuration : 65,536 words x 16 bits
- Read/write endurance : $10^{10}$ times
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : -20 °C to +85 °C
- $\overline{LB}$ and $\overline{UB}$ data byte control
- 48-pin, TSOP(1) plastic package

## ■ PACKAGE

48-pin plastic TSOP(1)



(FPT-48P-M25)

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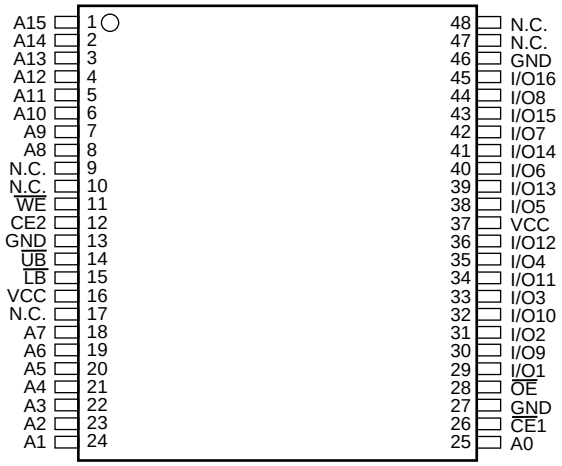
## ■ PIN ASSIGNMENT

(TOP VIEW)

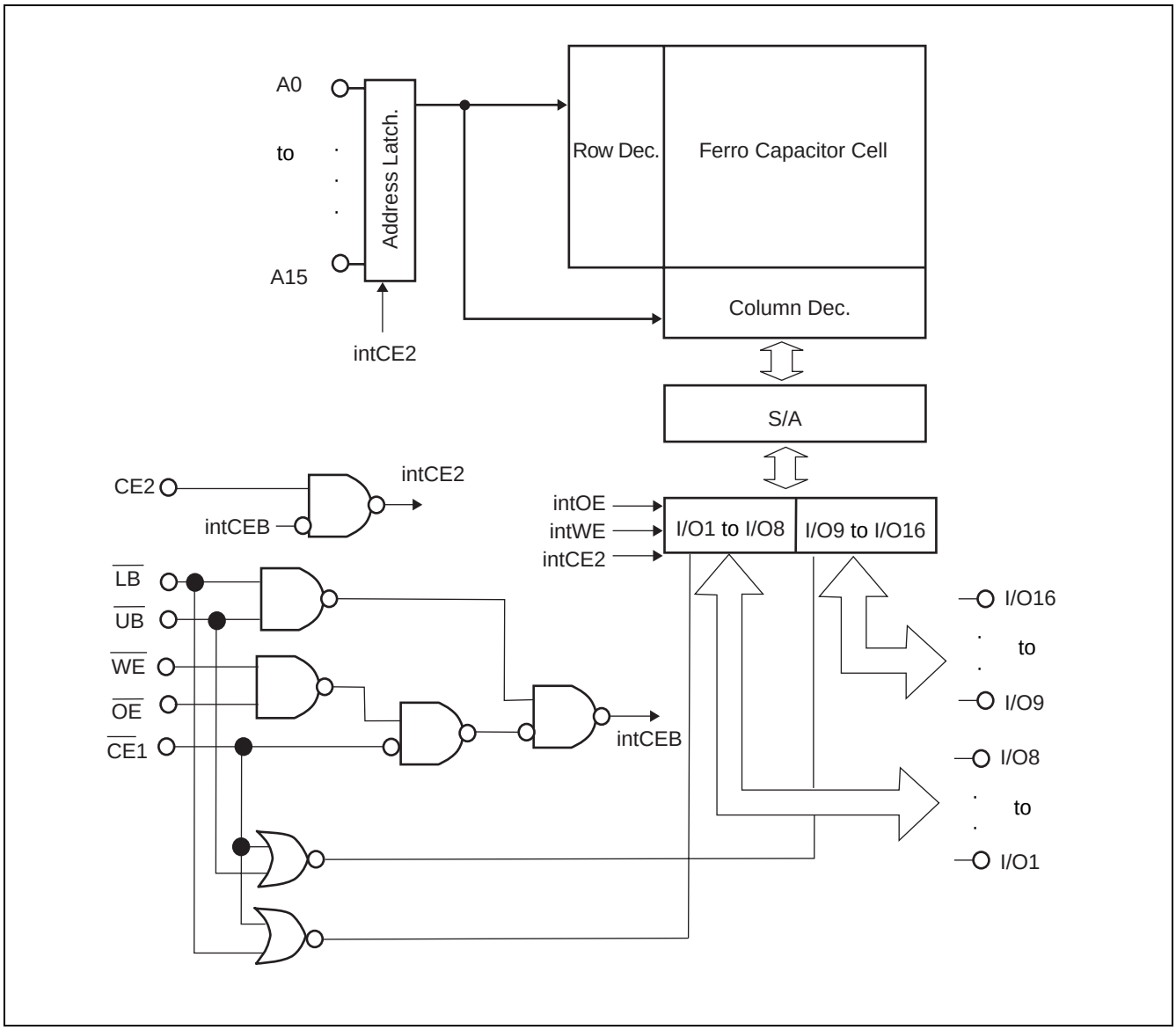



(FPT-48P-M25)

## ■ PIN DESCRIPTION

| Pin name | Function |
|---|---|
| A0 to A15 | Adderss In |
| I/O1 to I/O16 | Data Input/Output |
| $\overline{CE}$1 | Chip Enable 1 in |
| CE2 | Chip Enable 2 in |
| $\overline{WE}$ | Write Enable in |
| $\overline{OE}$ | Output Enable in |
| $\overline{LB}$, $\overline{UB}$ | Data Byte Control in |
| VCC | Power Supply |
| GND | Ground |

## ■ BLOCK DIAGRAM



## ■ FUNCTION TRUTH TABLE

| Mode | $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | $I/O_1$ to $I/O_8$ | $I/O_9$ to $I/O_{16}$ | Supply Current |
|---|---|---|---|---|---|---|---|---|---|
| Standby Pre-charge | H | X | X | X | X | X | High-Z | High-Z | Standby ($I_{SB}$) |
| | X | L | X | X | X | X | | | |
| | X | X | H | H | X | X | | | |
| | X | X | X | X | H | H | | | |
| Read | ↓ L | H ↑ | H | L | L | L | Dout | Dout | Operation ($I_{CC}$) |
| | | | | | L | H | Dout | High-Z | |
| | | | | | H | L | High-Z | Dout | |
| Read (Pseudo-SRAM, $\overline{OE}$ control) | L | H | H | ↓ | L | L | Dout | Dout | |
| | | | | | L | H | Dout | High-Z | |
| | | | | | H | L | High-Z | Dout | |
| Write | ↓ L | H ↑ | L | X | L | L | Din | Din | |
| | | | | | L | H | Din | High-Z | |
| | | | | | H | L | High-Z | Din | |
| Write (Pseudo-SRAM, $\overline{WE}$ control) | L | H | ↓ | H | L | L | Din | Din | |
| | | | | | L | H | Din | High-Z | |
| | | | | | H | L | High-Z | Din | |
| Output Disable | L | H | H | H | X | X | High-Z | High-Z | |

Notes : L = $V_{IL}$, H = $V_{IH}$, X can be either $V_{IL}$ or $V_{IH}$, High-Z = High Impedance

↓ : Latch address at falling edge, ↑ : Latch address at rising edge

## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Supply Voltage | $V_{CC}$ | –0.5 | +4.0 | V |
| Input Voltage | $V_{IN}$ | –0.5 | $V_{CC}$ + 0.5 | V |
| Output Voltage | $V_{OUT}$ | –0.5 | $V_{CC}$ + 0.5 | V |
| Ambient Operating Temperature | $T_A$ | –20 | +85 | °C |
| Storage Temperature | $T_{stg}$ | –40 | +125 | °C |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

($V_{CC}$ = 3.0 V to 3.6 V, $T_A$ = –20 °C to +85 °C)

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| Input Voltage (high) | $V_{IH}$ | $V_{CC}$ x 0.8 | — | $V_{CC}$ + 0.5 | V |
| Input Voltage (low) | $V_{IL}$ | –0.5 | — | +0.6 | V |
| Ambient Operating Temperature | $T_A$ | – 20 | — | +85 | °C |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC CHARACTERISTICS

($V_{CC}$ = 3.0 V to 3.6 V, $T_A$ = –20 °C to +85 °C)

| Parameter | Symbol | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input Leakage Current | $\|I_{LI}\|$ | $V_{IN}$ = 0 V to $V_{CC}$ | — | — | 10 | µA |
| Output Leakage Current | $\|I_{LO}\|$ | $V_{OUT}$ = 0 V to $V_{CC}$, $\overline{CE}1$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$ | — | — | 10 | µA |
| Supply Current | $I_{CC}$ | $\overline{CE}1$ = 0.2 V, CE2 = $V_{CC}$–0.2 V, $I_{out}$ = 0 mA*1 | — | — | 10 | mA |
| Standby Current | $I_{SB}$ | $\overline{CE}1 \geq V_{CC}$–0.2 V | — | 10 | 100 | µA |
| | | CE2 ≤ 0.2 V*2 | | | | |
| | | $\overline{OE} \geq V_{CC}$–0.2 V, $\overline{WE} \geq V_{CC}$–0.2 V*2 | | | | |
| | | $\overline{LB} \geq V_{CC}$–0.2 V, $\overline{UB} \geq V_{CC}$–0.2 V*2 | | | | |
| Output Voltage (high) | $V_{OH}$ | $I_{OH}$ = –2.0 mA | $V_{CC}$ x 0.8 | — | — | V |
| Output Voltage (low) | $V_{OL}$ | $I_{OL}$ = 2.0 mA | — | — | 0.4 | V |

*1 : $I_{out}$ : Output current

*2 : All other inputs ($\overline{CE}1$, CE2, $\overline{OE}$, $\overline{WE}$, $\overline{LB}$, $\overline{UB}$) should be at CMOS levels, i.e., H ≥ $V_{CC}$ – 0.2 V, L ≤ 0.2 V.

### 2. AC TEST CONDITIONS

Supply Voltage : 3.0 V to 3.6 V
Operating Temperature : –20 °C to +85 °C
Input Voltage Amplitude : 0.3 V to 2.7 V
Input Rising Time : 10 ns
Input Falling Time : 10 ns
Input Evaluation Level : 2.0 V / 0.8 V
Output Evaluation Level : 2.0 V / 0.8 V
Output Impedance : 50 pF

#### (1) Read Operation

($V_{CC}$ = 3.0 V to 3.6 V, $T_A$ = –20 °C to +85 °C)

| Parametere | symbol | Value | | unit |
|---|---|---|---|---|
| | | Min | Max | |
| Read Cycle time | $t_{RC}$ | 250 | — | ns |
| $\overline{CE}1$ Active Time | $t_{CA1}$ | 210 | 2,000 | ns |
| CE2 Active Time | $t_{CA2}$ | 210 | 2,000 | ns |
| $\overline{OE}$ Active Time | $t_{RP}$ | 210 | 2,000 | ns |
| $\overline{LB}$, $\overline{UB}$ Active Time | $t_{BP}$ | 210 | 2,000 | ns |
| Pre-charge Time | $t_{PC}$ | 40 | — | ns |
| Address Setup Time | $t_{AS}$ | 10 | — | ns |
| Address Hold Time | $t_{AH}$ | 50 | — | ns |
| $\overline{OE}$ Setup Time | $t_{ES}$ | 10 | — | ns |
| $\overline{LB}$, $\overline{UB}$ Setup Time | $t_{BS}$ | 10 | — | ns |
| $\overline{CE}1$ Access Time | $t_{CE1}$ | — | 100 | ns |
| CE2 Access Time | $t_{CE2}$ | — | 100 | ns |
| $\overline{OE}$ Access Time | $t_{OE}$ | — | 100 | ns |
| $\overline{OE}$ Output Floating Time | $t_{OHZ}$ | — | 25 | ns |

**(2) Write Operation**

($V_{CC}$ = 3.0 V to 3.6 V, $T_A$ = –20 °C to +85 °C)

| Parameter | Symbol | Value | | Notes |
|---|---|---|---|---|
| | | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 250 | — | ns |
| $\overline{CE}$1 Active Time | $t_{CA1}$ | 210 | 2,000 | ns |
| CE2 Active Time | $t_{CA2}$ | 210 | 2,000 | ns |
| $\overline{LB}$, $\overline{UB}$ Active Time | $t_{BP}$ | 210 | 2,000 | ns |
| Pre-Charge Time | $t_{PC}$ | 40 | — | ns |
| Address Setup Time | $t_{AS}$ | 10 | — | ns |
| Address Hold Time | $t_{AH}$ | 50 | — | ns |
| $\overline{LB}$, $\overline{UB}$ Setup Time | $t_{BS}$ | 10 | — | ns |
| Write Pulse Width | $t_{WP}$ | 210 | — | ns |
| Data Setup Time | $t_{DS}$ | 10 | — | ns |
| Data Hold Time | $t_{DH}$ | 50 | — | ns |
| Write Setup Time | $t_{WS}$ | 0 | — | ns |

**(3) Power ON/OFF Sequence**

| Parameter | Sym-bol | Value | | | Units |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $\overline{CE}$1 LEVEL holding time in Power OFF | $t_{pd}$ | 85 | — | — | ns |
| $\overline{CE}$1 LEVEL holding time in Power ON | $t_{pu}$ | 85 | — | — | ns |
| Power interval * | $t_{pi}$ | 0.5 | — | — | s |

* : Condition for power detection circuit to function

## 3. Pin Capacitance

(f = 1 MHz, $T_A$ = +25 °C)

| Parameter | Symbol | Test Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = GND | — | — | 10 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = GND | — | — | 10 | pF |

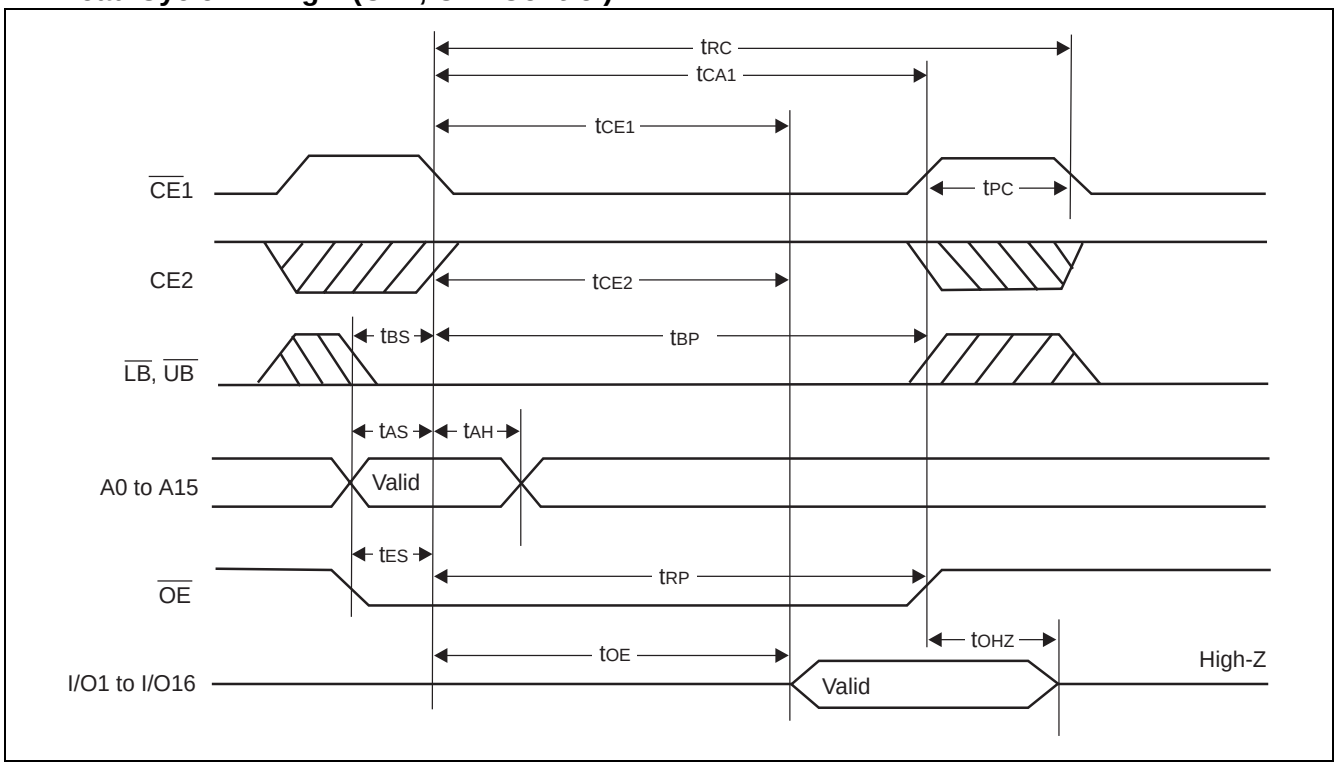
## 4. Reliability

Data retention 10 years ($T_A$ = 0 °C to +55 °C)

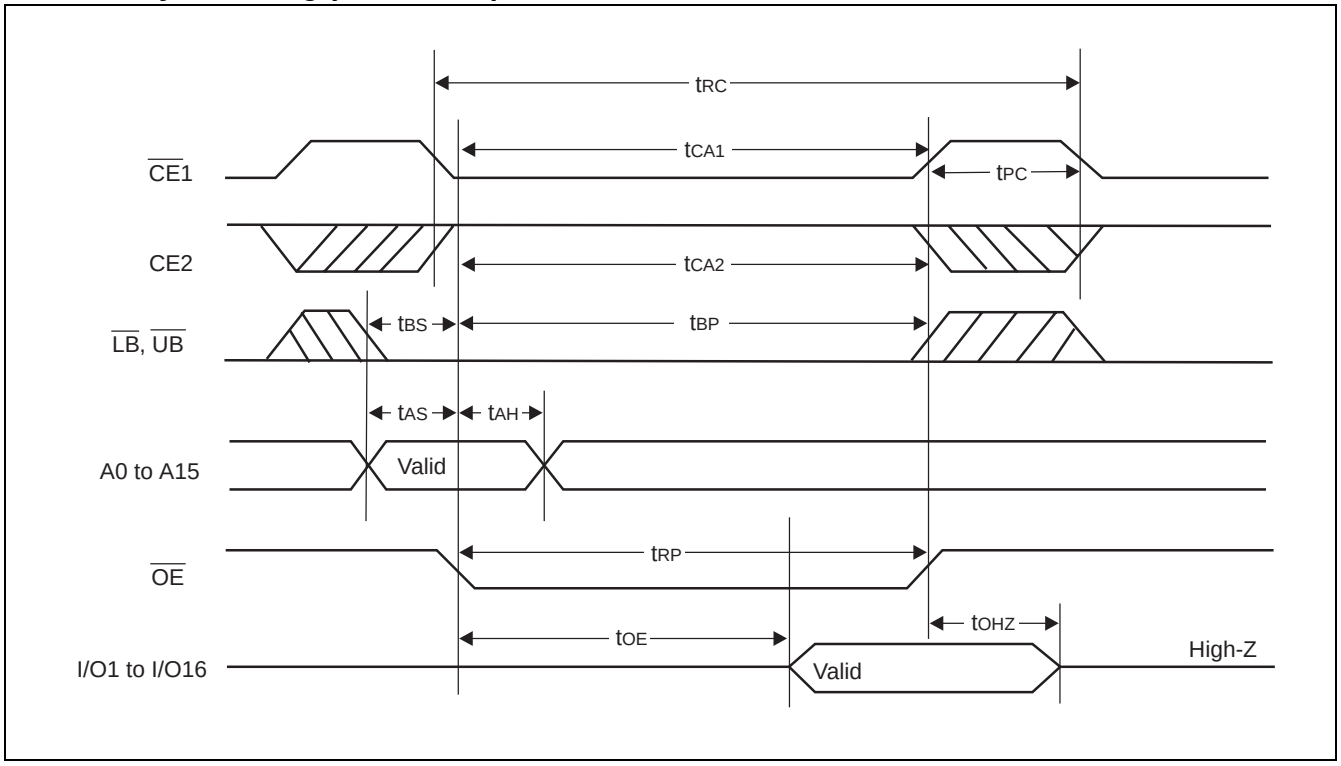
Access endurance $10^{10}$ times ($T_A$ = –20 °C to +85 °C)

## ■ TIMING DIAGRAMS

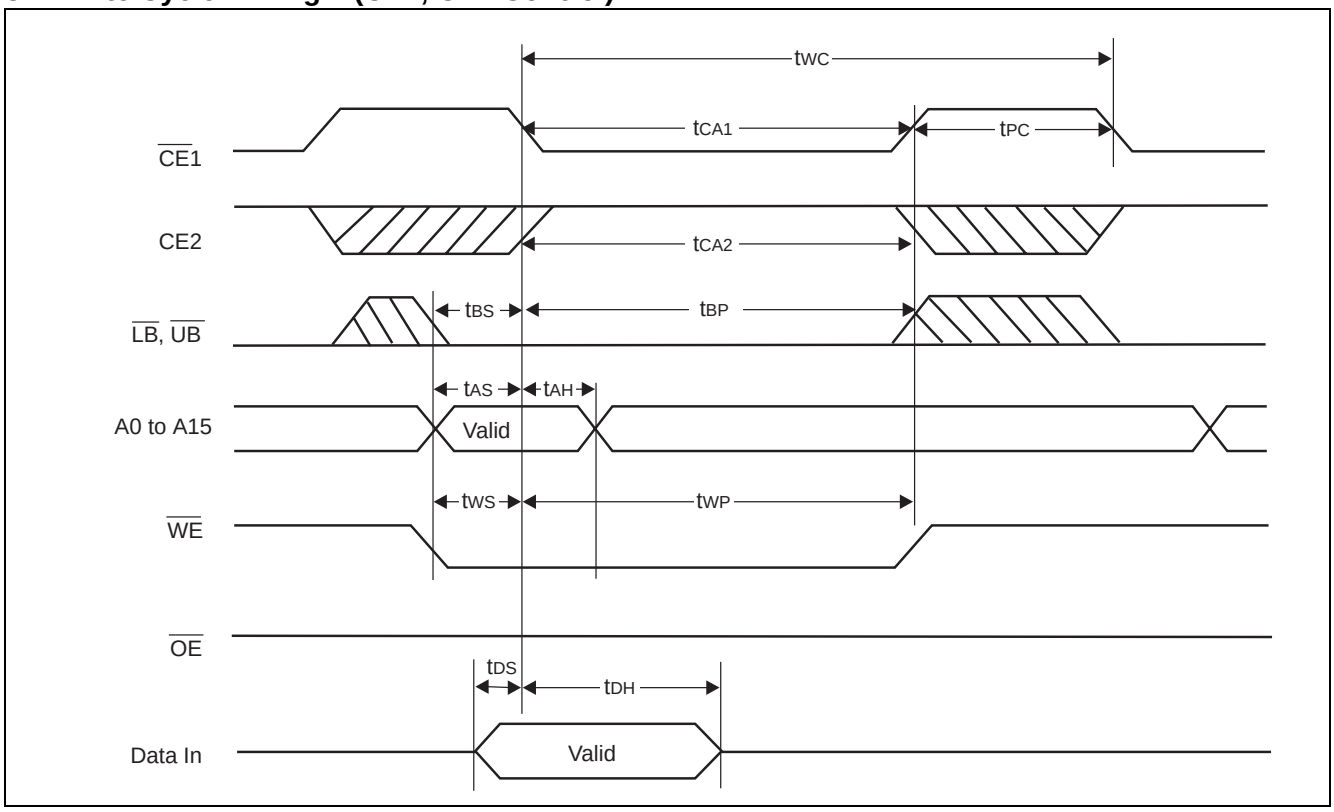
### 1. Read Cycle Timing 1 ($\overline{CE}$1, CE2 Control)



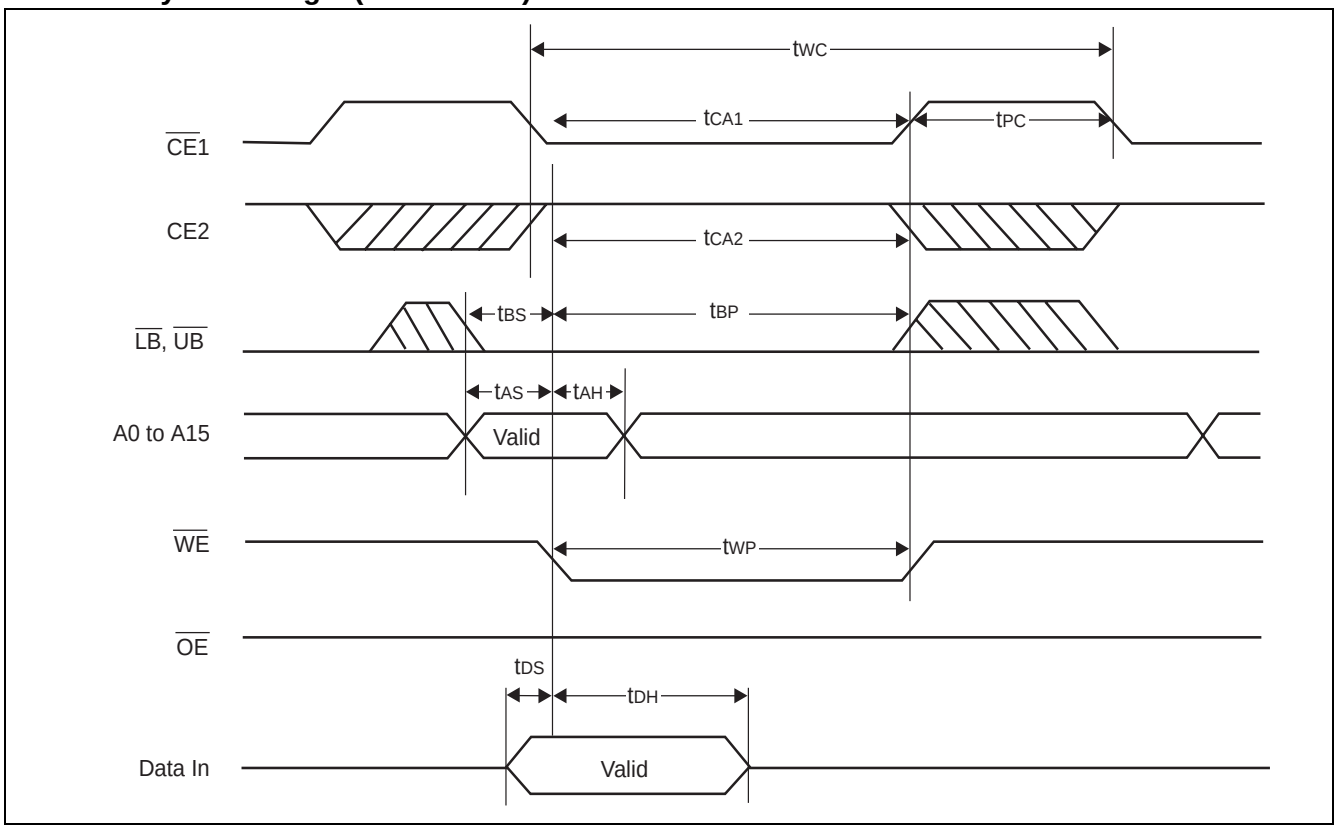

### 2. Read Cycle Timing ($\overline{OE}$ Control)



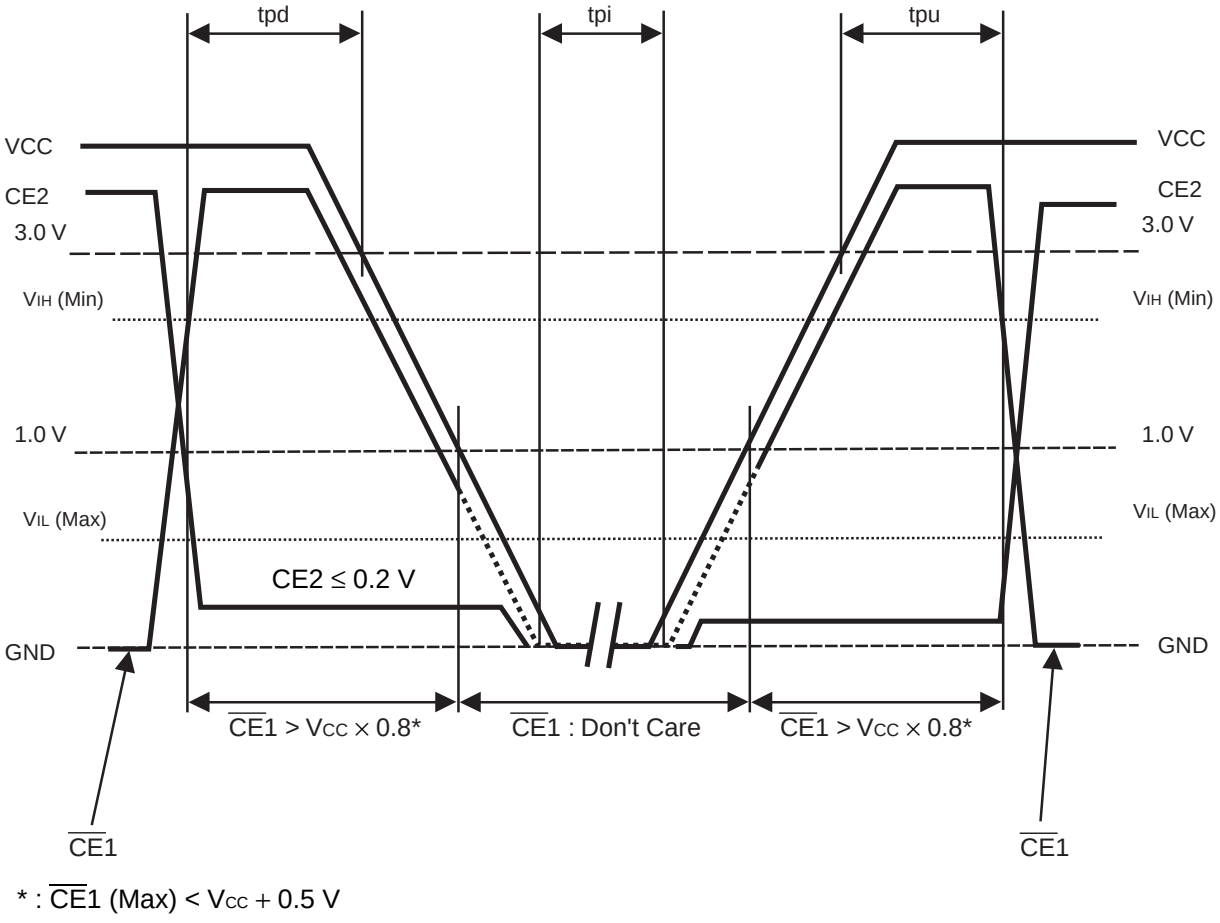
### 3. Write Cycle Timing 1 ($\overline{CE}$1, CE2 Control)




### 4. Write Cycle Timing 1 ($\overline{WE}$ Control)



## ■ POWER ON/OFF SEQUENCE




## ■ NOTES ON USE

After IR reflow, the hold of data that was written before IR reflow is not guaranteed.

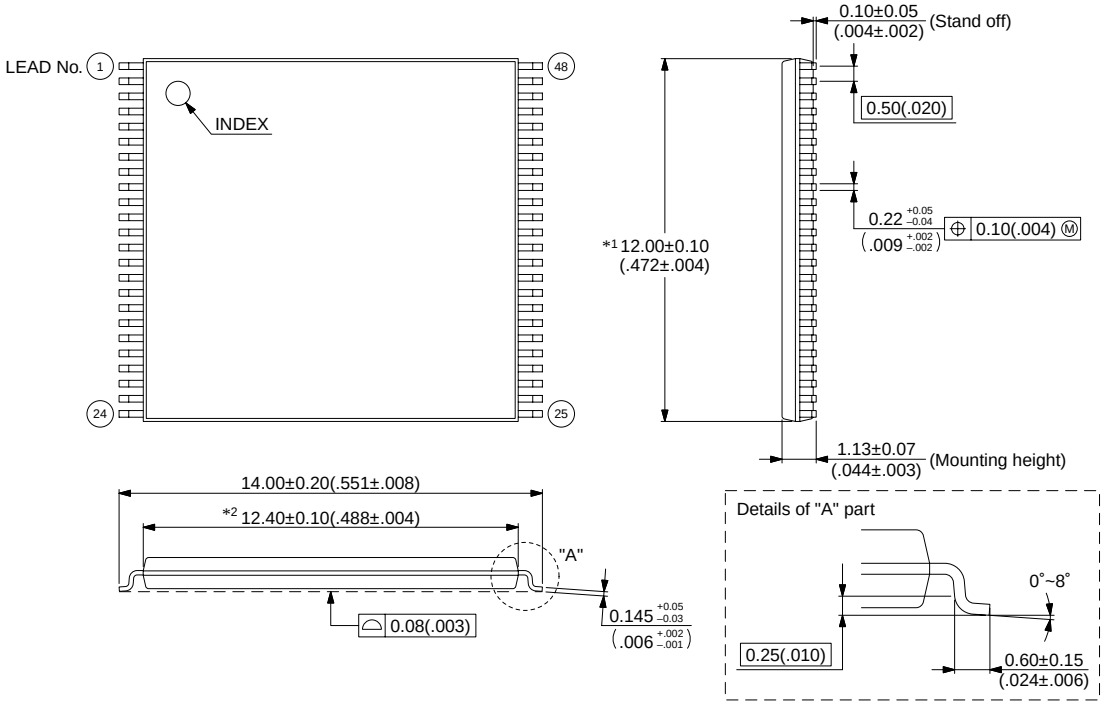
## ■ ORDERING INFOMATION

| Part number | Package | Remarks |
|---|---|---|
| MB85R1002PFTN | 48-pin plastic TSOP(1)<br>(FPT-48P-M25) | |

## ■ PACKAGE DIMENTION

48-pin plastic TSOP(1)
(FPT-48P-M25)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.






Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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