FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12537-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89670R/670AR Series

MB89673R/673AR/675R/675AR
MB89677AR/P677A/PV670A

■ OUTLINE

The MB89670R/670AR series has been developed as a line of proprietary 8-bit, single-chip microcontrollers.

In addition to the F²MC*-8L family CPU core which can operate at low voltage but at high speed, the microcontrollers contain pheripheral functions such as timers, a serial interface, a 10-bit A/D converter, a UART, an 8/16-bit up/down counter/timer, and an external interrupt.

The MB89670R/670AR series is applicable to a wide range of applications from consumer appliances to industrial equipment, including portable devices.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- High-speed processing at low voltage
- Minimum execution time: 0.4 µs@3.5 V, 0.8 µs@2.7 V, 2.0 µs@2.2 V
- I/O ports: max. 69 channels

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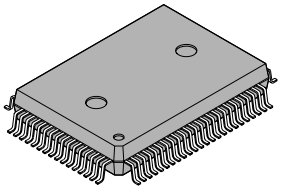
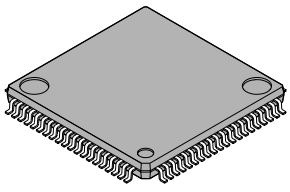
■ PACKAGE

80-pin Plastic QFP



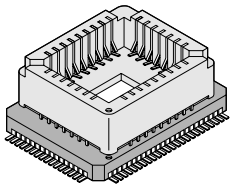
(FPT-80P-M06)

80-pin Plastic LQFP



(FPT-80P-M11)

80-pin Ceramic MQFP



(MQP-80C-P01)

(Continued)

- Timers: 9 channels (MB89675AR/677AR/P677A/PV670A: 12 channels)
  8-bit PWM timer: 3 channels (MB89675AR/677AR/P677A/PV670A: 6 channels) (also usable as a reload timer or 8-bit PWM timer)
  16-bit timer/counter
  21-bit timebase timer
  8/16-bit timer (8 bits × 2 channels or 16 bits)
  8/16-bit up/down counter/timer (8 bits × 2 channels or 16 bits)
- 2-channel serial interfaces
  8-bit synchronized serial: 1 channel (Switchable transfer direction allows communication with various equipment.)
  UART: 1 channel (internal full-duplex double buffer)
- External interrupts: 8 channels
  Eight channels are independent and capable of wake-up from low-power consumption modes (with an edge detection function).
- Buzzer output
- 10-bit A/D converter
  Input: 8 channels
- Low-power consumption modes
  Stop mode (Oscillation stops to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce the current consumption to approx. 1/3 of normal.)
- Bus interface function
  Including hold and ready functions

■ PRODUCT LINEUP

Item \ Part number	MB89673R[*1]	MB89673AR	MB89675R[*1]	MB89675AR	MB89677AR	MB89P677A	MB89PV670A
Classification	Mass-produced products (mask ROM products)					One-time PROM product (for development)	Piggyback/ evaluation product (for development)
ROM size	8 K × 8 bits (internal mask ROM)		16 K × 8 bits (internal mask ROM)		32 K × 8 bits (internal mask ROM)		48 K × 8 bits (external ROM)
RAM size	384 × 8 bits		512 × 8 bits		1 K × 8 bits		
CPU functions	The number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.4 µs@10 MHz to 6.4 µs@10 MHz Interrupt processing time: 3.6 µs@10 MHz to 57.6 µs@10 MHz						
Ports	Output ports (N-channel open-drain): 14 (12 also serve as peripherals.) Output ports (CMOS): 8 (All also serve as peripherals.) I/O ports (N-channel open-drain): 7 (All also serve as peripherals.) I/O ports (CMOS): 32 (All also serve as peripherals.) Input ports: 8 (All also serve as peripherals.) Total: 69						
Option	Specify when ordering masking					Set with EPROM programmer	Setting not possible
Timebase timer	21 bits (0.81 ms, 3.27 ms, 26.21 ms, 419 ms@10 MHz)						
8/16-bit up/down counter/timer	8 bits × 2 channels or 16 bits × 1 channel Timer operation Up/down counter operation Phase difference counting (double mode, quadruple mode)						
16-bit timer/counter	16-bit timer operation 16-bit event counter operation (edge selectable)						
8/16-bit timer/counter	8 bits × 2 channels or 16 bits × 1 channel Reload timer operation (toggled output capable) Event counter operation						
8-bit PWM timer 1, 2	8 bits × 2 channels reload timer operation (toggled output capable) 8 bits × 2 channels PWM operation (four frequencies fixed) 8 bits × 1 channel PPG operation (variable frequency) Capable of output switching between 2 channels in any mode						
8-bit PWM timer 3, 4, 5, 6	8-bit reload timer operation (toggled output capable) 8-bit PWM operation (four frequencies fixed) Capable of output switching between 2 channels in any mode						
8-bit serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks)						

(Continued)

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Item \ Part number	MB89673R*1	MB89673AR	MB89675R*1	MB89675AR	MB89677AR	MB89P677A	MB89PV670A
UART	Variable data length (7 or 8 bits) On-chip baud rate generator Error detection function On-chip full-duplex double buffer NRZ transfer format CLK synchrnous/asynchronous data transfer capable						
10-bit A/D converter	10 bits × 8 channels						
External interrupt	8 channels (Rising edge/falling edge)						
Power supply voltage*2	2.2 V to 6.0 V					2.7 V to 6.0 V	
EPROM for use	—						MBM27C512-20TV

*1: 8-bit PWM timer 4, 5, and 6 are not provided for the MB89673R/MB89675R.
*2: The minimum operating voltage varies with the operating frequency, the function, and the connected ICE.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89673R MB89675R	MB89673AR MB89675AR MB89677AR	MB89P677A	MB89PV670A
FPT-80P-M06	○	○	○	×
FPT-80P-M11	○	○	○	×*
MQP-80C-P01	×	×	×	○

○ : Available × : Not available

* : Lead pitch converter sockets (manufacturer: Sun Hayato Co., Ltd.) are available
80QF-80QF2-8L-UP
+ (MQP-80C-P01 or FPT-80P-M06) → for conversion to FPT-80P-M11
80QF-80QF2-8L-DWN

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, make sure of its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89P677A, the program area starts from address 8007_H, while on the MB89677AR and MB89PV670A starts from 8000_H.

  (On the MB89P677A, the option setting data can be read by reading the addresses "8000_H" to "8006_H", while on the MB89677AR and MB89PV670A, addresses 8000_H to 8006_H could also be used as a program ROM. However, do not use these addresses in order to maintain compatibility of the MB89P677A.)
- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV670A, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following point:

- Options are fixed on the MB89PV670A.

4. Differences between the MB89670/670A and MB89670R/670AR Series

- Memory access area

  Memory access area of both the MB89677A and MB89677AR is the same.

  The access are of the MB89673 is different from that of the MB89673R and MB89673AR respectively in the external bus mode. See below.

Address	Memory area	
	MB89673	MB89673R/673AR
0000_H to $007F_H$	I/O area	I/O area
0080_H to $01FF_H$	RAM area	RAM area
0200_H to $027F_H$	External area	Access prohibited
0280_H to $BFFF_H$		External area
$C000_H$ to $DFFF_H$		Access prohibited
$E000_H$ to $FFFF_H$	ROM area	ROM area

- Electrical specifications/characteristics
  Electrical specifications/characteristics of the MB89673R/673AR/677AR are the same with that of the MB89670/670A series.
- The other specifications
  Both the MB89673R/673AR/677AR and the MB89670/670A series are the same.

■ CORRESPONDENCE BETWEEN THE MB89670/670A SERIES AND MB89670R/670AR SERIES

- The MB89670R/670AR series is the reduction version of the MB89670/670A series.
- The MB89670/670A and MB89670R/670AR sereis consist of the following products:

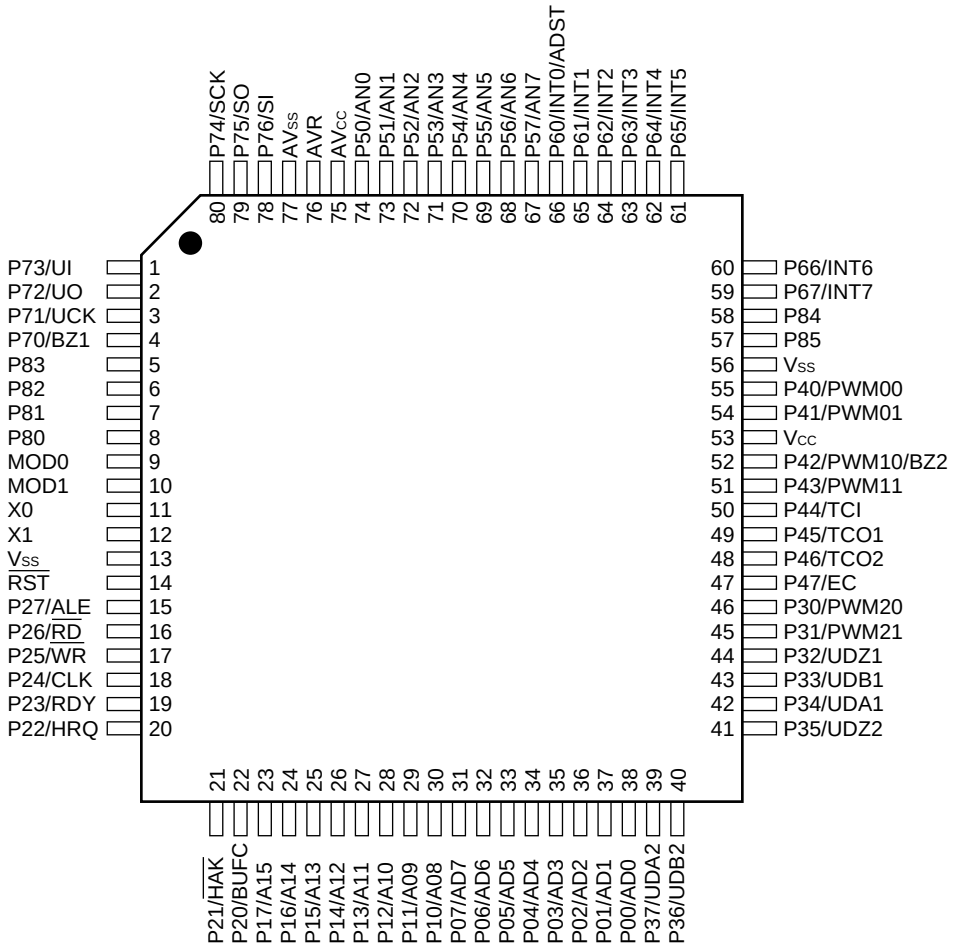
MB89670/ 670A series	MB89673	—	—	—	MB89677A	MB89P677A	MB89PV670A
MB89670R/ 670AR series	MB89673R	MB89673AR	MB89675R	MB89675AR	MB89677AR		

- Differences between the MB89670A/670AR series and MB89670/670R series
  8-bit PWM timer 4, 5, and 6 is not provided for the MB89670/670R series.
  See the table below for the provided 8-bit PWM timer and the corresponding pin for the MB89670A/670AR series and MB89670/670R series.

Function	Pin name for MB89670A/670AR series	Pin name for MB89670/670R series
8-bit PWM timer 1	P40/PWM00	P40/PWM00, P41/PWM01
8-bit PWM timer 2	P42/PWM10/BZ2	P42/PWM10/BZ2, P43/PWM11
8-bit PWM timer 3	P30/PWM20	P30/PWM20, P31/PWM21
8-bit PWM timer 4	P31/PWM21	—
8-bit PWM timer 5	P41/PWM01	—
8-bit PWM timer 6	P43/PWM11	—

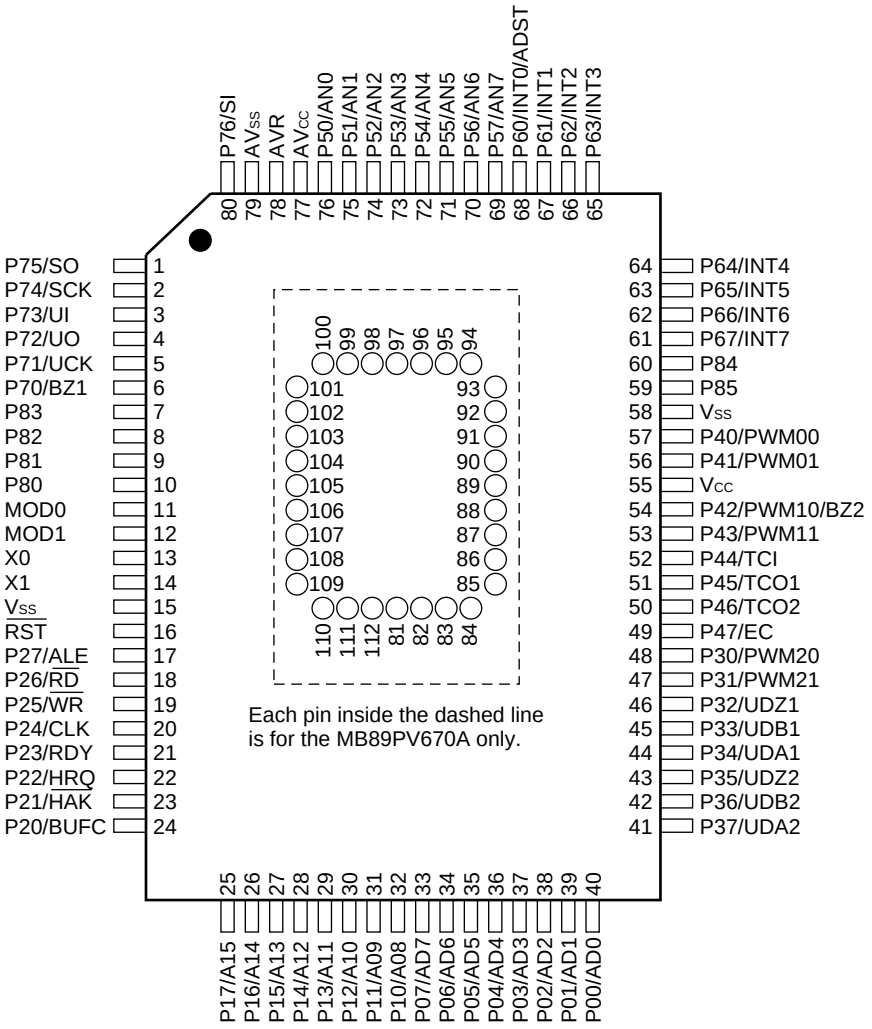
■ PIN ASSIGNMENT

(Top view)



(FPT-80P-M11)

(Top view)



(FPT-80P-M06)

(MQP-80C-P01)

- **Pin assignment on package top (MB89PV670A only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	A2	97	N.C.	105	$\overline{OE}$/V_{PP}
82	A15	90	A1	98	O4	106	N.C.
83	A12	91	A0	99	O5	107	A11
84	A7	92	N.C.	100	O6	108	A9
85	A6	93	O1	101	O7	109	A8
86	A5	94	O2	102	O8	110	A13
87	A4	95	O3	103	$\overline{CE}$	111	A14
88	A3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2 MQFP*3			
11	13	X0	A	Clock oscillator pins
12	14	X1		
9	11	MOD0	B	Operating mode selection pins Connect directly to V_{CC} or V_{SS}.
10	12	MOD1		
14	16	$\overline{RST}$	C	Reset I/O pin This pin is of a N-ch open-drain output type with pull-up resistor and a hysteresis input type. "L" is output from this pin by an internal reset source. The internal circuit is initialized by the input of "L".
38 to 31	40 to 33	P00/AD0 to P07/AD7	D	General-purpose I/O ports When an external bus is used, these ports function as multiplex pins of lower address output and data I/O.
30 to 23	32 to 25	P10/A08 to P17/A15	D	General-purpose I/O ports When an external bus is used, these ports function as upper address output pins.
22	24	P20/BUFC	F	General-purpose output port When an external bus is used, this port can also be used as a buffer control output by setting the BCTR.
21	23	P21/$\overline{HAK}$	F	General-purpose output port When an external bus is used, this port can also be used as a hold acknowledge output by setting the BCTR.
20	22	P22/HRQ	D	General-purpose output port When an external bus is used, this port can also be used as a hold request input by setting the BCTR.
19	21	P23/RDY	D	General-purpose output port When an external bus is used, this port functions as a ready input.
18	20	P24/CLK	F	General-purpose output port When an external bus is used, this port functions as a clock output.
17	19	P25/$\overline{WR}$	F	General-purpose output port When an external bus is used, this port functions as a write signal output.
16	18	P26/$\overline{RD}$	F	General-purpose output port When an external bus is used, this port functions as a read signal output.
15	17	P27/ALE	F	General-purpose output port When an external bus is used, this port functions as an address latch signal output.

(Continued)

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2 MQFP*3			
46	48	P30/PWM20	D	General-purpose I/O port Also serves as the PWM20 output for the 8-bit PWM timer.
45	47	P31/PWM21	D	General-purpose I/O port Also serves as the PWM21 output for the 8-bit PWM timer.
44	46	P32/UDZ1	E	General-purpose I/O port Also serves as the Z-phase input for the 8/16-bit up/down counter/timer.
43	45	P33/UDB1	E	General-purpose I/O port Also serves as the B-phase input for the 8/16-bit up/down counter/timer.
42	44	P34/UDA1	E	General-purpose I/O ports Also serves as the A-phase input for the 8/16-bit up/down counter/timer.
41	43	P35/UDZ2	E	General-purpose I/O port Also serves as the Z-phase input for the 8/16-bit up/down counter/timer.
40	42	P36/UDB2	E	General-purpose I/O port Also serves as the B-phase input for the 8/16-bit up/down counter/timer.
39	41	P37/UDA2	E	General-purpose I/O port Also serves as the A-phase input for the 8/16-bit up/down counter/timer.
55	57	P40/PWM00	D	General-purpose I/O port Also serves as the PWM00 output for the 8-bit PWM timer.
54	56	P41/PWM01	D	General-purpose I/O port Also serves as the PWM01 output for the 8-bit PWM timer.
52	54	P42/PWM10/ BZ2	D	General-purpose I/O port Also serves as the PWM10 and the BZ2 output for the 8-bit PWM timer.
51	53	P43/PWM11	D	General-purpose I/O port Also serves as the PWM11 output for the 8-bit PWM timer.
50	52	P44/TCI	E	General-purpose I/O port Also serves as the TCI input for the 8/16-bit timer/counter.
49	51	P45/TCO1	D	General-purpose I/O port Also serves as the TCO1 output for the 8/16-bit timer/counter.
48	50	P46/TCO2	D	General-purpose I/O port Also serves as the TCO2 output for the 8/16-bit timer/counter.

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*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

(Continued)

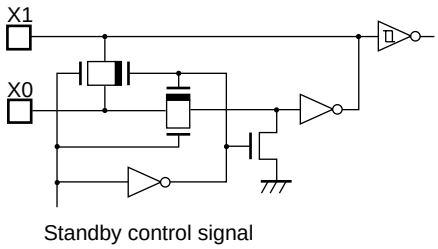
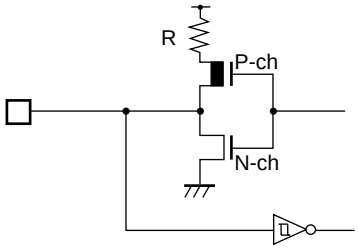
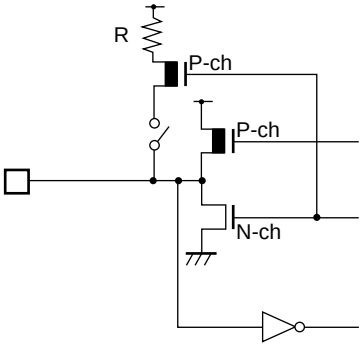
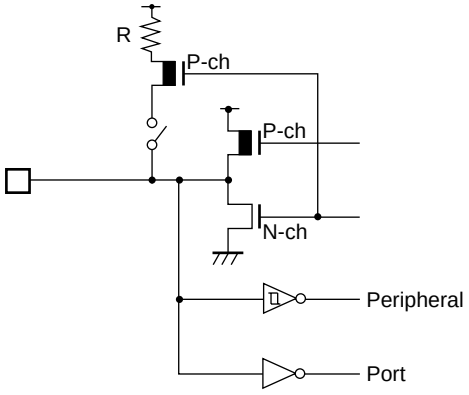
Pin no.		Pin name	Circuit type	Function
LQFP*1	QFP*2 MQFP*3			
47	49	P47/EC	E	General-purpose I/O port Also serves as the input for the16-bit timer/counter. The EC input is of a hysteresis input type.
74 to 67	76 to 69	P50/AN0 to P57/AN7	I	N-ch open-drain output ports Also serve as the analog inputs for the 10-bit A/D converter.
66	68	P60/INT0/ ADST	J	General-purpose input port The software pull-up resistor is provided. Also serves as an external interrupt input (INT0) and an 10-bit A/D converter external start-up. This port is of a hysteresis input type.
65 to 59	67 to 61	P61/INT1 to P67/INT7	J	General-purpose input ports A software pull-up resistor is provided. Also serve as external interrupt inputs (INT1 to INT7). These ports are of a hysteresis input type.
4	6	P70/BZ1	G	N-ch open-drain I/O port Also serves as a buzzer output.
3	5	P71/UCK	K	N-ch open-drain I/O port Also serves as a UART clock I/O (UCK), switchable to CMOS.
2	4	P72/UO	K	N-ch open-drain I/O port Also serves as a UART data output (UO), switchable to CMOS.
1	3	P73/UI	G	N-ch open-drain I/O port Also serves as a UART data input (UI).
80	2	P74/SCK	K	N-ch open-drain I/O port Also serves as the clock I/O (SCK) for the 8-bit serial I/O, switchable to CMOS.
79	1	P75/SO	K	N-ch open-drain I/O port Also serves as the data output (SO) for the 8-bit serial I/O, switchable to CMOS.
78	80	P76/SI	G	N-ch open-drain I/O port Also serves as the data input (SI) for the 8-bit serial I/O.
8 to 5, 57, 58	10 to 7, 59, 60	P80 to P83, P85, P84	H	N-ch open-drain output ports
53	55	V_{CC}	—	Power supply pin
13, 56	15, 58	V_{SS}	—	Power supply (GND) pin
75	77	AV_{CC}	—	A/D converter power supply pin Use this pin at the same voltage as V_{CC}.
76	78	AVR	—	A/D converter reference voltage input pin
77	79	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.

*1: FPT-80P-M11
*2: FPT-80P-M06
*3: MQP-80C-P01

- **External EPROM pins (MB89PV670A only)**

Pin no.	Pin name	I/O	Function
82 83 84 85 86 87 88 89 90 91	A15 A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}/V_{PP}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	
111	A14	O	
112	V_{CC}	O	
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type • Oscillation feedback resistor of approximately 1 MΩ at 5.0 V
B		
C		• Output pull-up resistor (P-ch) of approximately 50 kΩ at 5.0 V • Hysteresis input
D		• CMOS output • CMOS inout • Pull-up resistor optional (except P22 and P23)
E		• CMOS output • CMOS input • The peripheral is of a hysteresis input type. • Pull-up resistor optional

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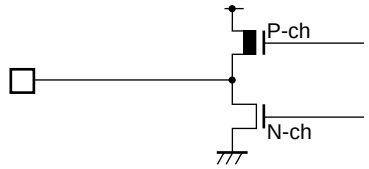
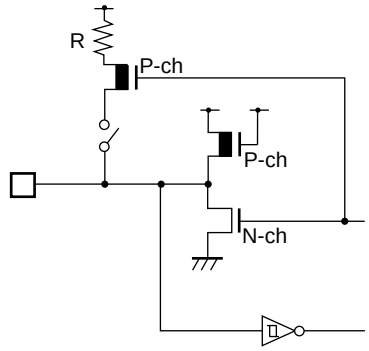
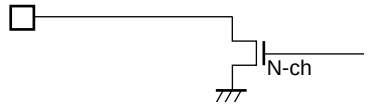
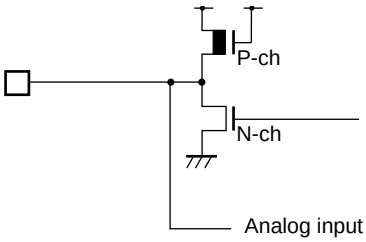
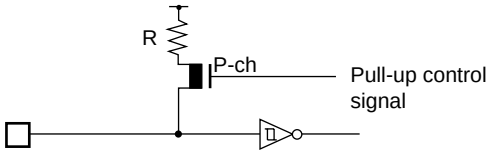
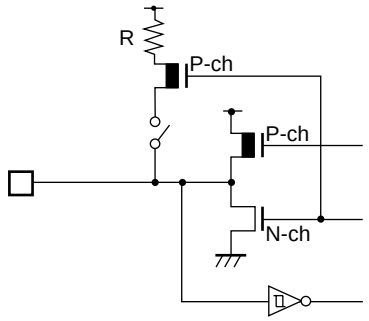
Type	Circuit	Remarks
F		• CMOS output
G		• N-ch open-drain output • Hysteresis input • Pull-up resistor optional
H		• N-ch open-drain output
I		• N-ch open-drain output • Analog input
J		• Hysteresis input • With software pull-up resistor
K		• CMOS output • Hysteresis input • Pull-up resistor optional

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P677A

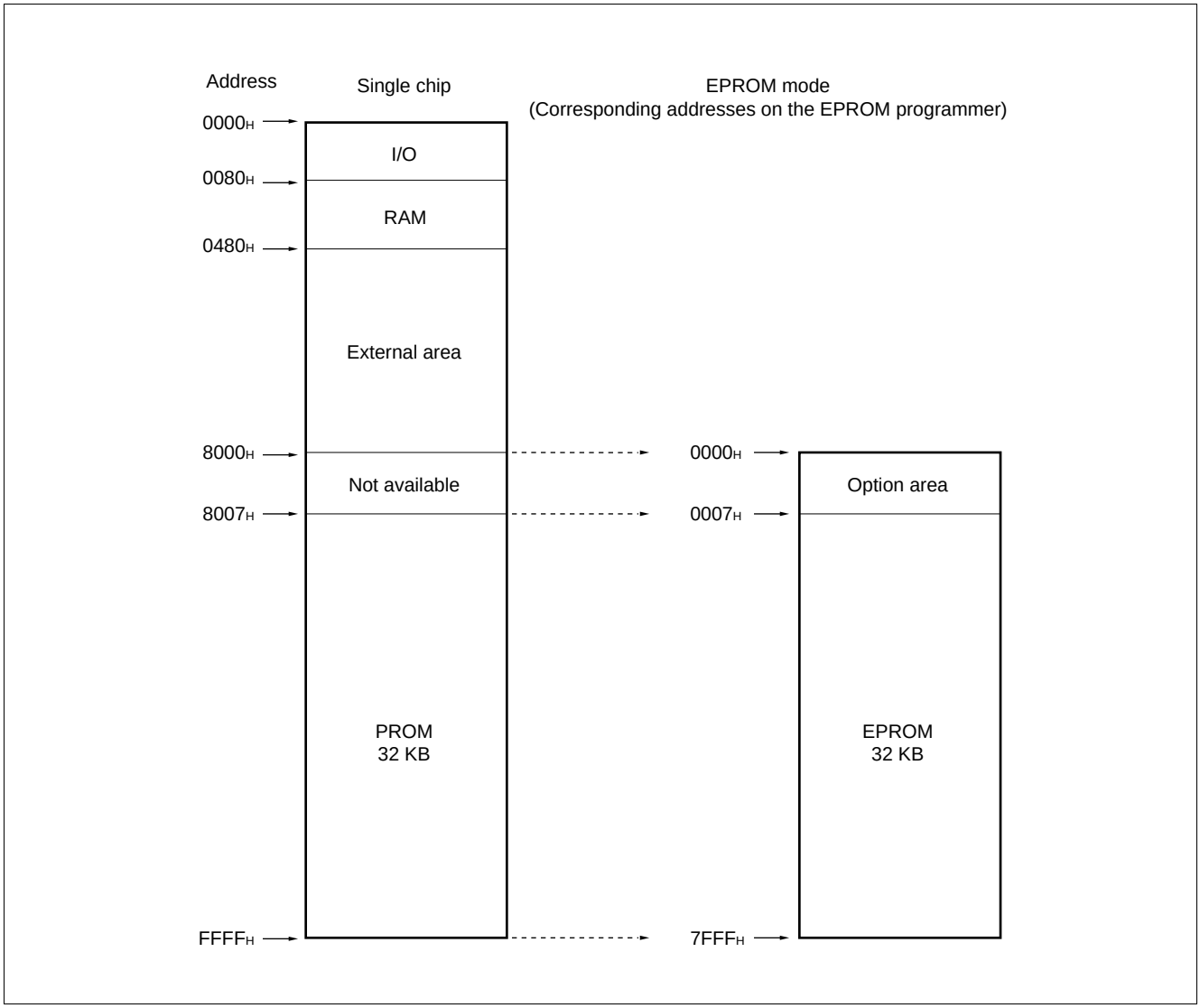
The MB89P677A is an OTPROM version of the MB89670R/670AR series.

1. Features

- 32-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in the EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in the EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P677A functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

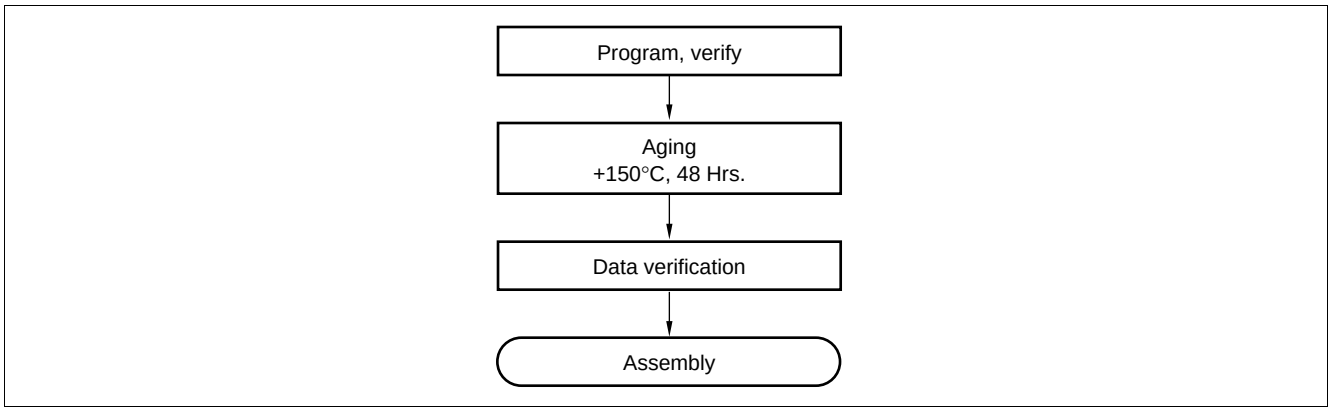
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0007_H to $7FFF_H$ (note that addresses 8007_H to $FFFF_H$ while operating as a single chip assign to 0007_H to $7FFF_H$ in the EPROM mode).
Load option data into addresses 0000_H to 0006_H of the EPROM programmer. (For information about each corresponding option, see “7. Setting OTPROM Options.”)

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

Due to the nature of the blanked OTPROM microcomputer, bit programming test can’t be conducted as Fujitsu’s shipping test. Therefore a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Part number	MB89P677APF	MB89P677PFM
Package	QFP-80	QFP-80
Compatible socket adapter Sun Hayato Co., Ltd.	ROM-80QF-28DP-8L2	ROM-80QF2-28DP-8L

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Note: Depending on the EPROM programmer, inserting a capacitor of about 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

7. Setting OTPROM Options

The programming procedure is the same as that for the PROM.

Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

- **OTPROM option bit map**

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0000_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization time 00: $2^4/F_C$ 10: $2^{17}/F_C$	 01: $2^{14}/F_C$ 11: $2^{18}/F_C$
0001_H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
0002_H	P37 Pull-up 1: No 0: Yes	P36 Pull-up 1: No 0: Yes	P35 Pull-up 1: No 0: Yes	P34 Pull-up 1: No 0: Yes	P33 Pull-up 1: No 0: Yes	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0003_H	P47 Pull-up 1: No 0: Yes	P46 Pull-up 1: No 0: Yes	P45 Pull-up 1: No 0: Yes	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
0004_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
0005_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
0006_H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	P04 to P07 Pull-up 1: No 0: Yes	P00 to P03 Pull-up 1: No 0: Yes	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes

Notes:
- Each bit is set to “1” as the initialized value.
- Do not write “0” to the vacant bit.
  The read value of the vacant bit is “1”, unless “0” is written to it.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

2. Programming Socket Adapter

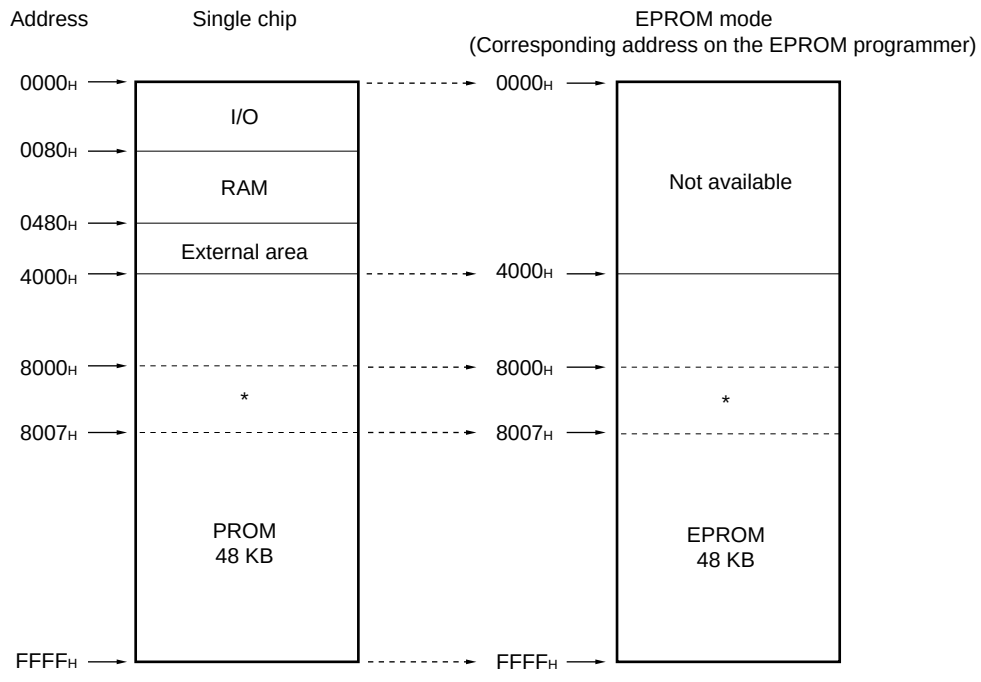
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

3. Memory Space

Memory space in each mode is diagrammed below.



*: Note: For the MB89P677A, this area is an option setting area.

4. Programming to the EPROM

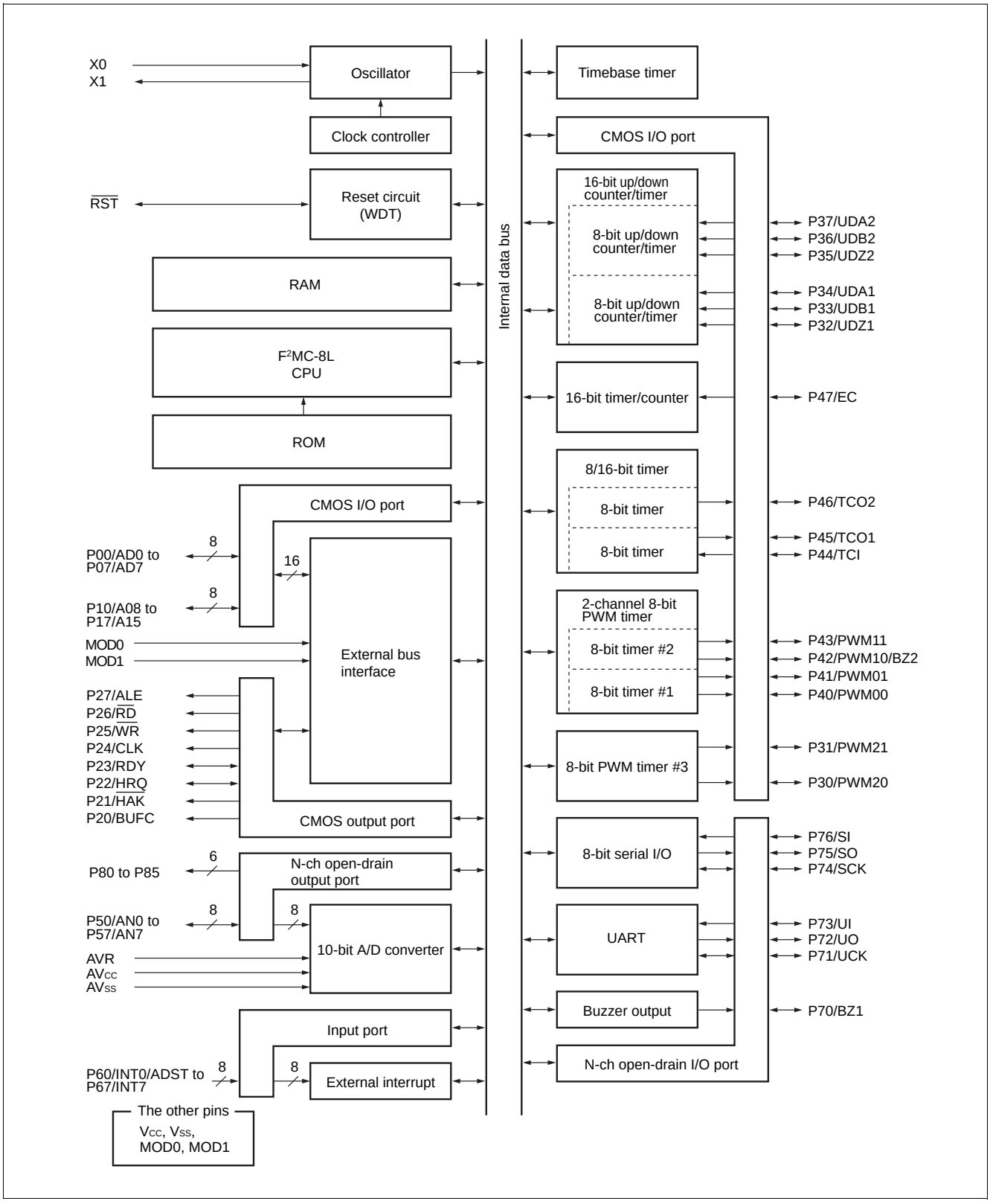
(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 4000_H to $FFFF_H$.

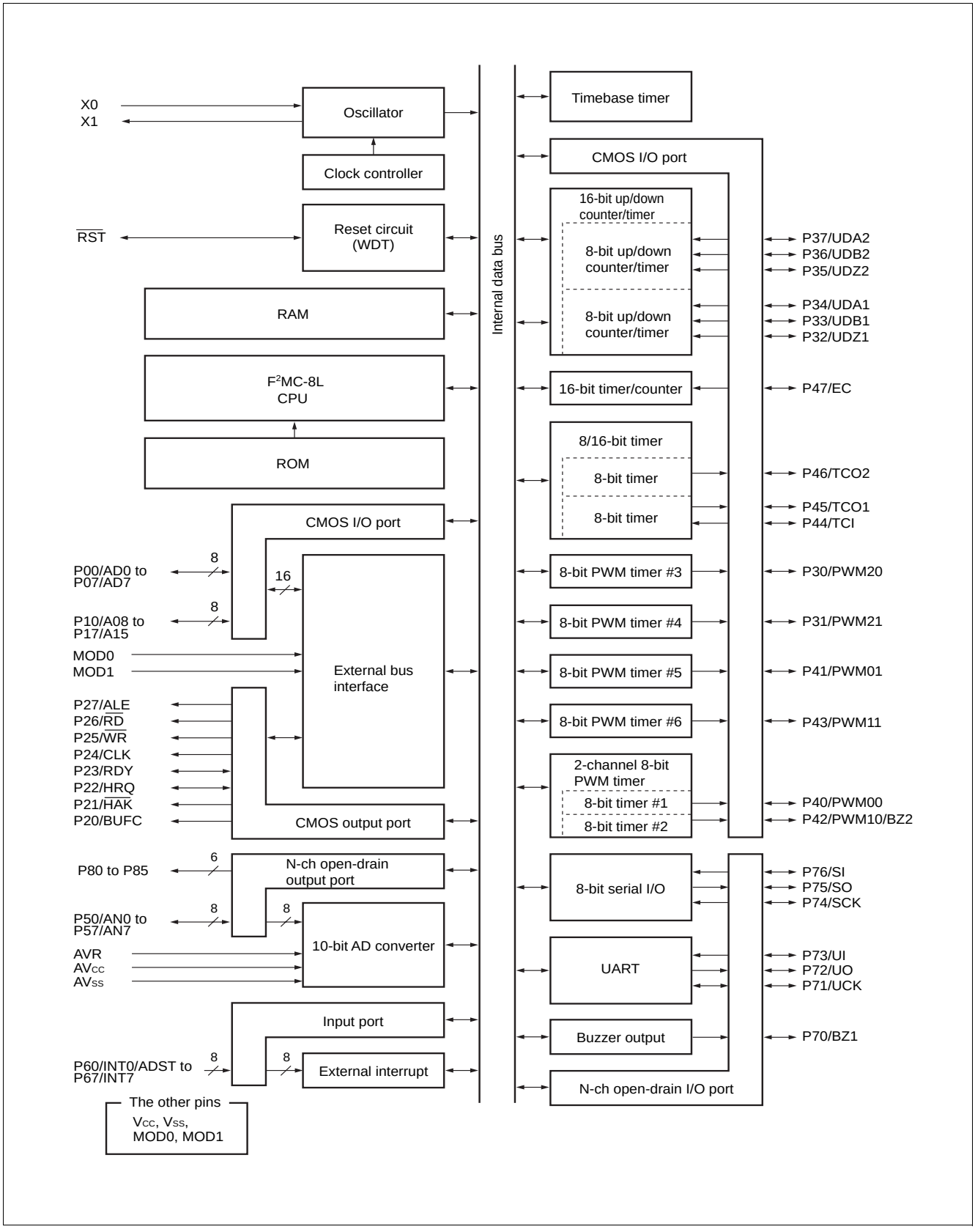
(3) Program to 4000_H to $FFFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

1. Block Diagram of MB89673R/89675R



2. Block Diagram of MB89673AR /89675AR/89677AR/89P677A/89PV670A

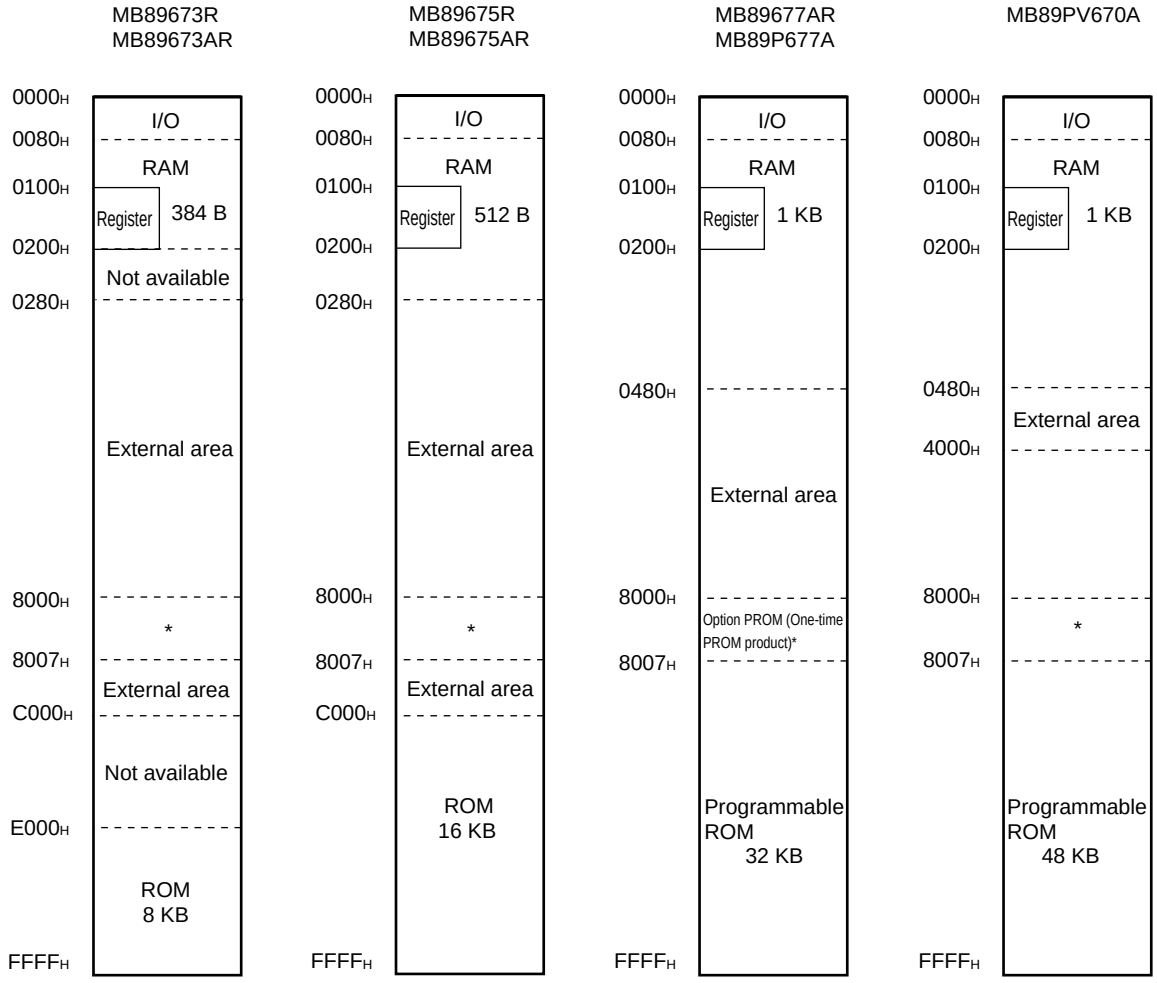


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89670R/670AR series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated at the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is allocated from exactly the opposite end of I/O area, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address within the program area. The memory space of the MB89670R/670AR series is structured as illustrated below.

• **Memory Space**

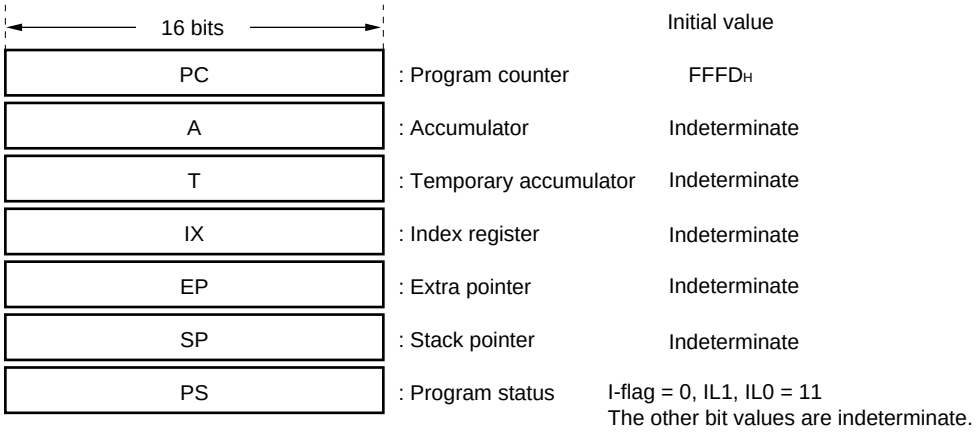


*: Since addresses 8000H to 8006H for the MB89P677A comprise an option area, pay attention to use this area for the other products in this series.

2. Registers

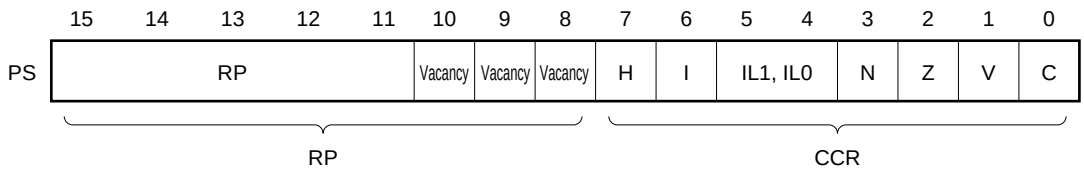
The F²MC-8L family has two types of registers; dedicated hardware registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating the instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



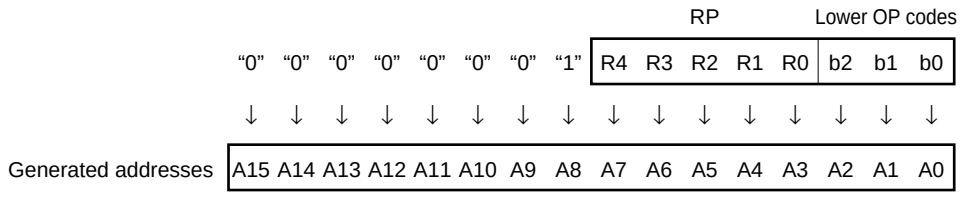
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

• Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, IL0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

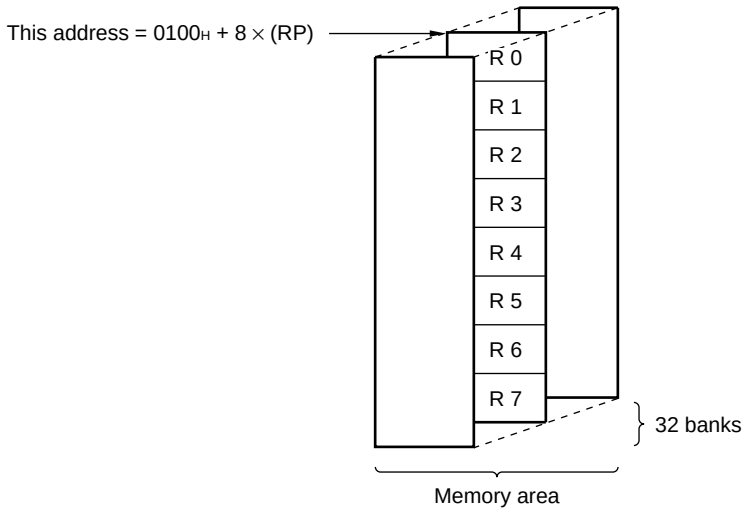
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are of 8 bits each and allocated in the register banks of the memory. One bank contains eight registers and up to 32 banks can be used on every product of the MB89670R/670AR series. The bank currently in use is indicated by the register bank pointer (RP).

• **Register Bank Configuration**



■ I/O MAP

Address	Read/Write	Register abbreviation	Register name
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H	(R/W)	PDR1	Port 1 data register
03H	(W)	DDR1	Port 1 data direction register
04H	(R/W)	PDR2	Port 2 data register
05H	(W)	BCTR	External bus pin control register
06H	(Vacancy)		
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBTC	Timebase timer control register
0BH	(Vacancy)		
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 data direction register
0EH	(R/W)	PDR4	Port 4 data register
0FH	(W)	DDR4	Port 4 data direction register
10H	(R/W)	PDR5	Port 5 data register
11H	(R)	PDR6	Port 6 data register
12H	(R/W)	PPCR	Port 6 pull-up control register
13H	(R/W)	PDR7	Port 7 data register
14H	(R/W)	PDR8	Port 8 data/port 7 swiching register
15H	(R/W)	BZCR	Buzzer register
16H	(R/W)	CNTR #3	PWM control register #3
17H	(R/W)	COMP #3	PWM compare register #3
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer count register (H)
1AH	(R/W)	TCLR	16-bit timer count register (L)
1BH	(Vacancy)		
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH to 1FH	(Vacancy)		

(Continued)

Address	Read/Write	Register abbreviation	Register name
20H	(R/W)	ADC1	A/D converter control register 1
21H	(R/W)	ADC2	A/D converter control register 2
22H	(R/W)	ADCH	A/D converter data register H
23H	(R/W)	ADCL	A/D converter data register L
24H	(R/W)	T2CR	Timer 2 control register
25H	(R/W)	T1CR	Timer 1 control register
26H	(R/W)	T2DR	Timer 2 data register
27H	(R/W)	T1DR	Timer 1 data register
28H	(R/W)	CNTR1	PWM 1 control register
29H	(R/W)	CNTR2	PWM 2 control register
2AH	(R/W)	CNTR3	PWM 3 control register
2BH	(W)	COMR2	PWM 2 compare register
2CH	(W)	COMR1	PWM 1 compare register
2DH to 2FH	(Vacancy)		
30H	(R) (W)	UDCR1 RCR1	Up/down counter register 1 Reload compare register1
31H	(R) (W)	UDCR2 RCR2	Up/down counter register 2 Reload compare register2
32H	(R/W)	CCRA1	Counter control register A1
33H	(R/W)	CCRA2	Counter control register A2
34H	(R/W)	CCRB1	Counter control register B1
35H	(R/W)	CCRB2	Counter control register B2
36H	(R/W)	CSR1	Counter status register 1
37H	(R/W)	CSR2	Counter status register 2
38H	(R/W)	EIC1	External interrupt 1 control register 1
39H	(R/W)	EIC2	External interrupt 1 control register 2
3AH	(R/W)	EIE2	External interrupt 2 control register
3BH	(R/W)	EIF2	External interrupt 2 flag register
3CH to 3FH	(Vacancy)		

(Continued)

(Continued)

Address	Read/Write	Register abbreviation	Register name
40H	(R/W)	USMR	UART serial mode register
41H	(R/W)	USCR	UART serial rate control register
42H	(R/W)	USTR	UART status register
43H	(R) (W)	RXDR TXDR	UART receiving data register UART transmitting data register
44H	(Vacancy)		
45H	(R/W)	RRDR	Baud rate generator reload data register
46H to 47H	(Vacancy)		
48H*	(R/W)	CNTR #4	PWM control register #4
49H*	(R/W)	COMP #4	PWM compare register #4
4AH*	(R/W)	CNTR #5	PWM control register #5
4BH*	(R/W)	COMP #5	PWM compare register #5
4CH*	(R/W)	CNTR #6	PWM control register #6
4DH*	(R/W)	COMP #6	PWM compare register #6
4E to 7BH	(Vacancy)		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	(Vacancy)		

* : For the MB89673R/675R, these are (vacancies).

Note: Do not use (vacancies).

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Rated value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	*
	AV_{CC}	V_{SS} – 0.3	V_{CC} + 0.3	V	*
A/D converter reference input voltage	AVR	V_{SS} – 0.3	V_{CC} + 0.3	V	AVR must not exceed "AV_{CC} + 0.3 V".
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	Except P80 to P85
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P80 to P85
"L" level maximum output current	I_{OL}	—	20	mA	
"L" level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating rate)
	I_{OLAV2}	—	8	mA	Average value (operating current × operating rate) P80 to P85
"L" level total maximum output current	$\sum I_{OL}$	—	100	mA	
"L" level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
"H" level maximum output current	I_{OH}	—	–20	mA	
"H" level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating rate)
"H" level total maximum output current	$\sum I_{OH}$	—	–50	mA	
"H" level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

* : Use AV_{CC} and V_{CC} set at the same voltage.
Take care that AVR does not exceed "AV_{CC} + 0.3 V" and AV_{CC} does not exceed V_{CC}, such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

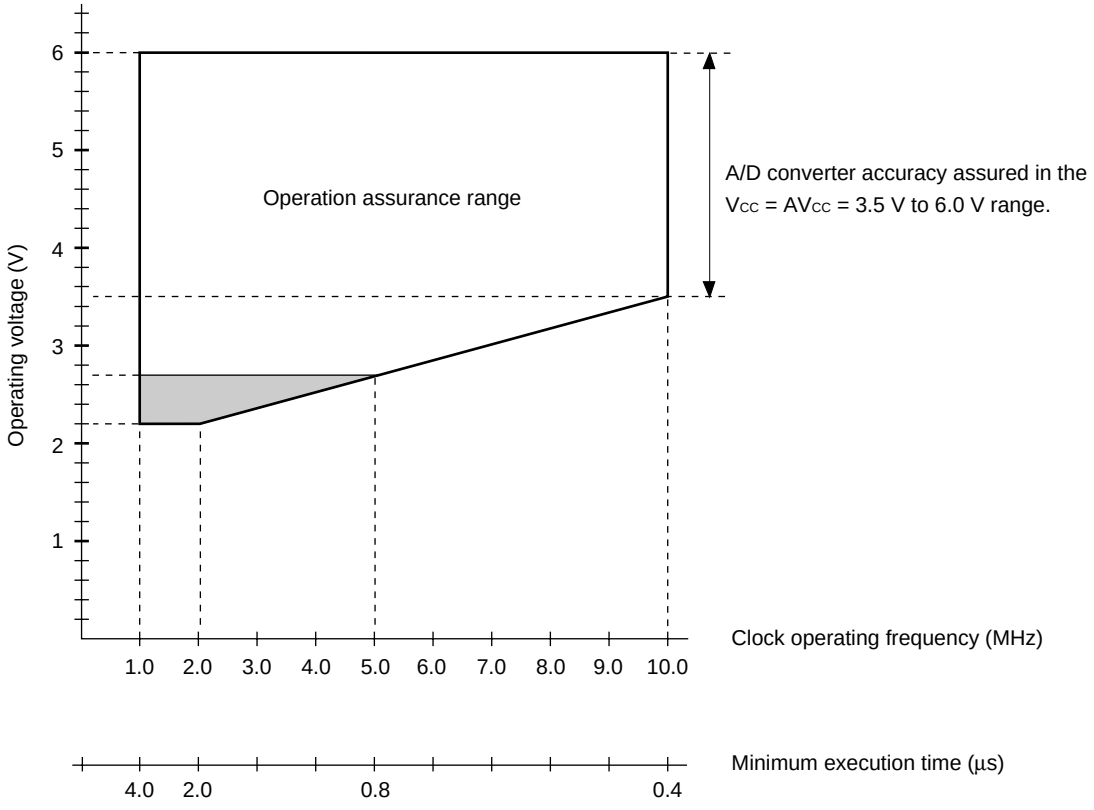
2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Rated value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*	6.0	V	Normal operation assurance range MB89673R/673AR/675R/675AR/677AR
		2.7*	6.0	V	Normal operation assurance range MB89PV670A/P677A
		1.5	6.0	V	Retains the RAM state in the stop mode
A/D converter reference input voltage	AVR	0.0	AV_{CC}	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

Figure 1 Operating Voltage vs. Clock Operating Frequency



Note: The shaded area is additional operating assurance range only for the MB89673R/673AR/675R/675AR/677AR.

The horizontal line of the graph in the figure 1 indicates the operating frequency of the external oscillator and the lower horizontal line indicates the min. instruction execution time = 4/F_C.

In the case of changing the operating clock with the clock gear function, be sure to convert it into the min. instruction execution time on the lower horizontal line since the operating voltage range is dependent on the min. instruction execution time.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin name	Condition	Rated value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P30 to P37, P40 to P47	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	P32 to P37, P44, and P47 are of a port input type.
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, P32 to P37, P44, P47, P60 to P67, P70 to P76		0.8 V_{CC}	—	V_{CC} + 0.3	V	P32 to P37, P44, and P47 are of a peripheral input type.
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47		V_{SS} – 0.3	—	0.3 V_{CC}	V	P32 to P37, P44, and P47 are of a port input type.
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, P32 to P37, P44, P47, P60 to P67, P70 to P76		V_{SS} – 0.3	—	0.2 V_{CC}	V	P32 to P37, P44, and P47 are of a peripheral input type.
Open-drain output pin applied voltage	V_D	P80 to P85		V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P71, P72, P74, P75	I_{OH} = –2.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P76	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P80 to P85	I_{OL} = 10 mA	—	—	0.5	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P76, MOD0, MOD1	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor option
	I_{LI2}	P80 to P85	0.0 V < V_I < V_{CC}	—	—	±1	µA	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P60 to P67, P70 to P76, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor option

(Continued)

(Continued)

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC1}	V_{CC}	F_C = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	12	20	mA	
	I_{CC2}		F_C = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1	2	mA	MB89673R/673AR/675R/675AR/677AR/PV670A
				—	1.5	2.5	mA	MB89P677A
	I_{CCS1}		Sleep mode: F_C = 10 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.4 µs	—	3	7	mA	
	I_{CCS2}		Sleep mode: F_C = 10 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 6.4 µs	—	1	1.5	mA	
	I_{CCH}		V_{CC} = 3.0 V, T_A = +25°C, Stop mode	—	—	1	mA	
	I_A	AV_{CC}	F_C = 10 MHz, When A/D converter starts	—	6	8	mA	
	I_{AH}		F_C = 10 MHz, T_A = +25°C, When A/D converter is at a stop	—	—	1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The measurement conditions of the power supply current are as follows.
The external clock is used.
The output pins are open.
V_{CC} is upon the condition above the table.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

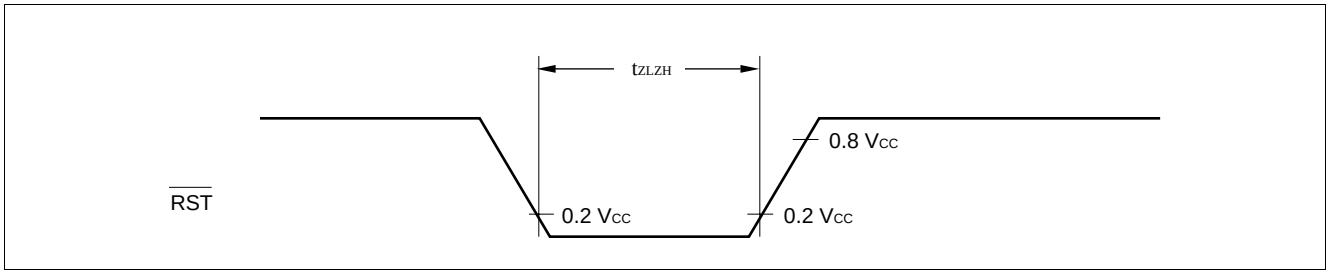
Note: The current consumption of connected EPROM and ICE is not considered on MB89PV670A.

4. AC Characteristics

(1) Reset Timing

($AV_{CC} = V_{CC} = 5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Rated value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

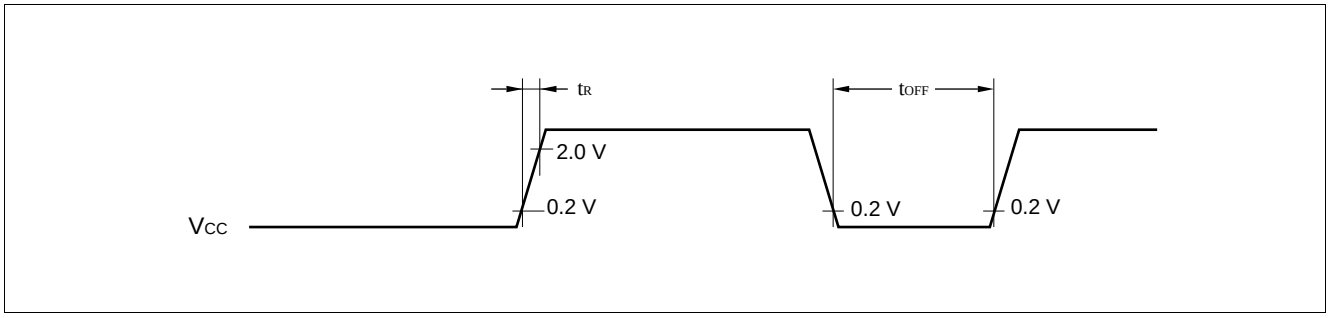


(2) Specifications for Power-on Reset

($AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Rated value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Min. internal time to next power-on reset

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

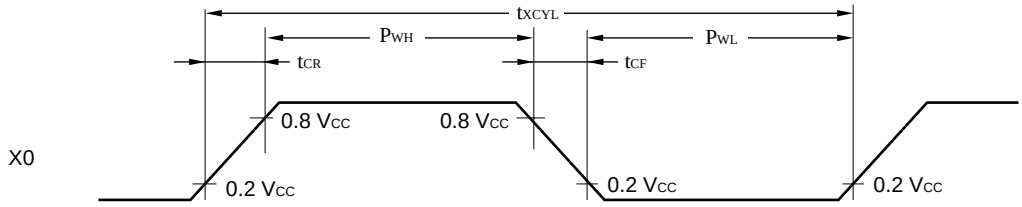


(3) Clock Timing

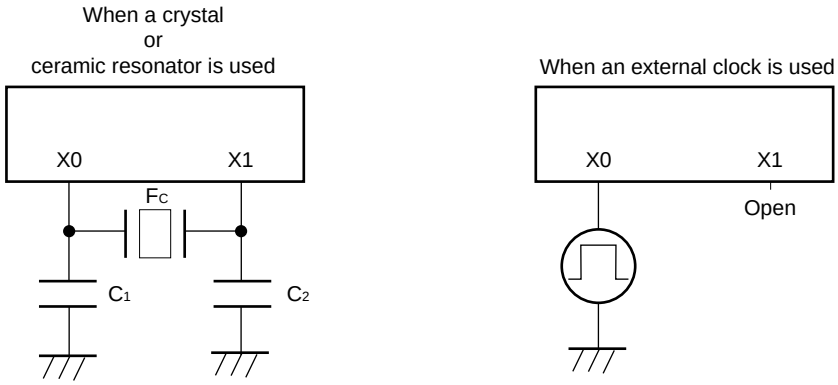
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	10	MHz	
Clock cycle time	t_{XCYL}	X0, X1		100	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	10	ns	External clock

• Clock Timing Conditions



• Clock Configurations



(4) Instruction Cycle

(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

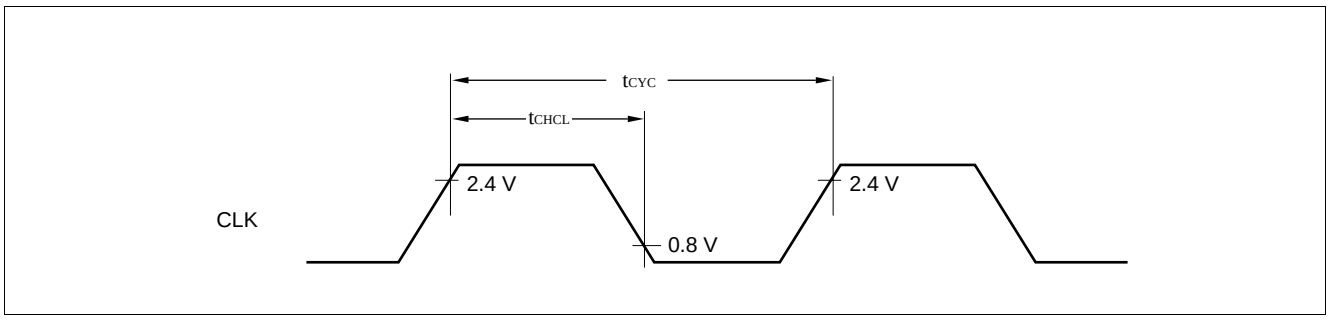
Parameter	Symbol	Rated value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_C, 8/F_C, 16/F_C, 64/F_C	µs	(4/F_C) t_{inst} = 0.4 µs when operating at F_C = 10 MHz

(5) Clock Output Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	1/2 t_{inst}*	—	µs	
CLK ↑ → CLK ↓	t_{CHCL}	CLK		1/4 t_{inst} – 0.07	1/4 t_{inst}	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

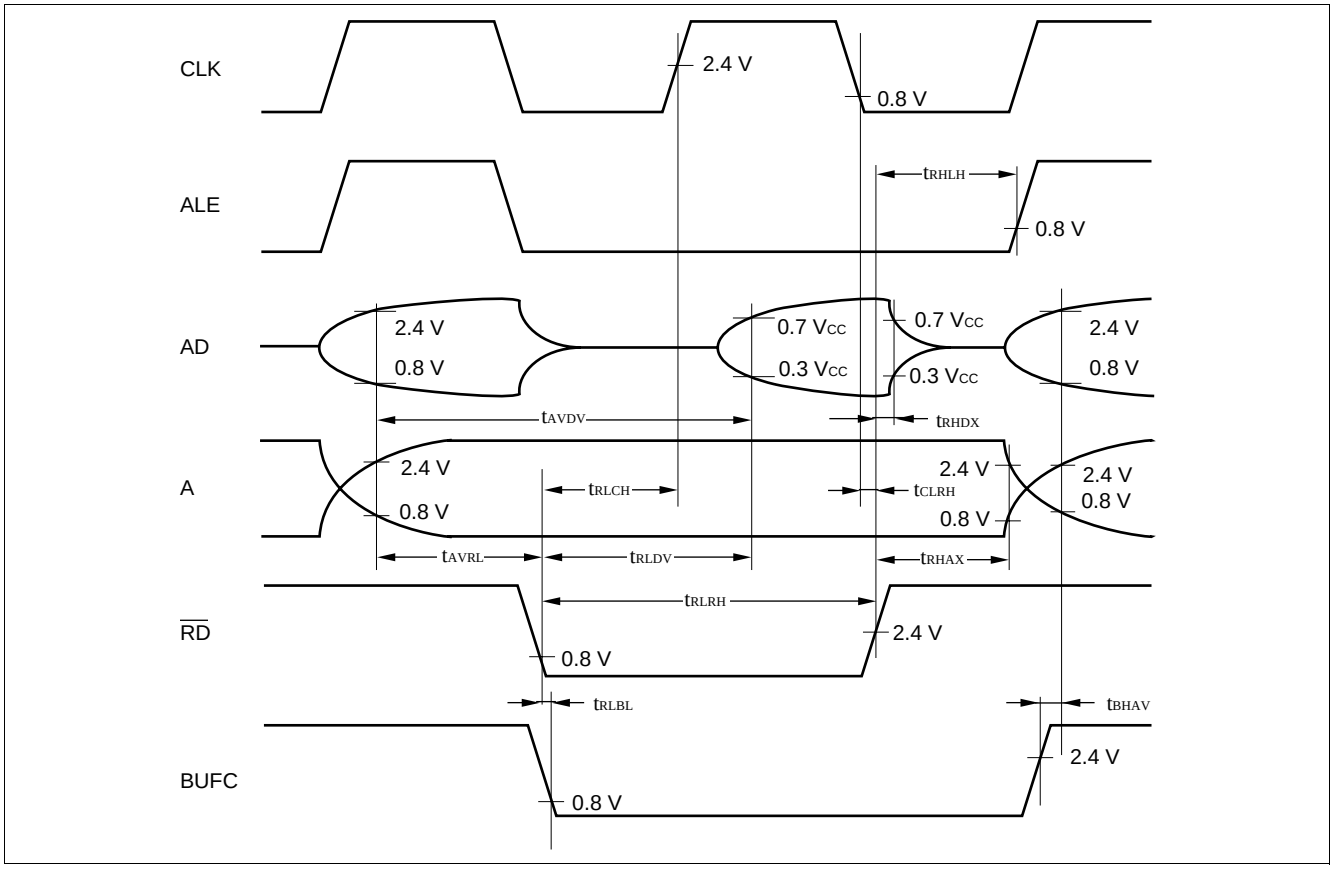


(6) Bus Read Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
Valid address → $\overline{RD}$ ↓ time	t_{AVRL}	$\overline{RD}$, A15 to A08, AD7 to AD0	—	1/4 t_{inst}* – 0.06	—	µs	
$\overline{RD}$ pulse width	t_{RLRH}	$\overline{RD}$		1/2 t_{inst}* – 0.02	—	µs	
Valid address → Data read time	t_{AVDV}	AD7 to AD0, A15 to A08		—	1/2 t_{inst}*	µs	No wait
$\overline{RD}$ ↓ → Data read time	t_{RLDV}	$\overline{RD}$, AD7 to AD0		—	1/2 t_{inst}* – 0.08	µs	No wait
$\overline{RD}$ ↑ → Data hold time	t_{RHDX}	AD7 to AD0, $\overline{RD}$		0	—	ns	
$\overline{RD}$ ↑ → ALE ↑ time	t_{RHLH}	$\overline{RD}$, ALE		1/4 t_{inst}* – 0.04	—	µs	
$\overline{RD}$ ↑ → Address loss time	t_{RHAX}	$\overline{RD}$, A15 to A08		1/4 t_{inst}* – 0.04	—	µs	
$\overline{RD}$ ↓ → CLK ↑ time	t_{RLCH}	$\overline{RD}$, CLK		1/4 t_{inst}* – 0.04	—	µs	
CLK ↓ → $\overline{RD}$ ↑ time	t_{CLRH}	$\overline{RD}$, CLK		0	—	ns	
$\overline{RD}$ ↓ → BUFC ↓ time	t_{RLBL}	$\overline{RD}$, BUFC		–5	—	ns	
BUFC ↑ → Valid address time	t_{BHAV}	A15 to A08, AD7 to AD0, BUFC		5	—	ns	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



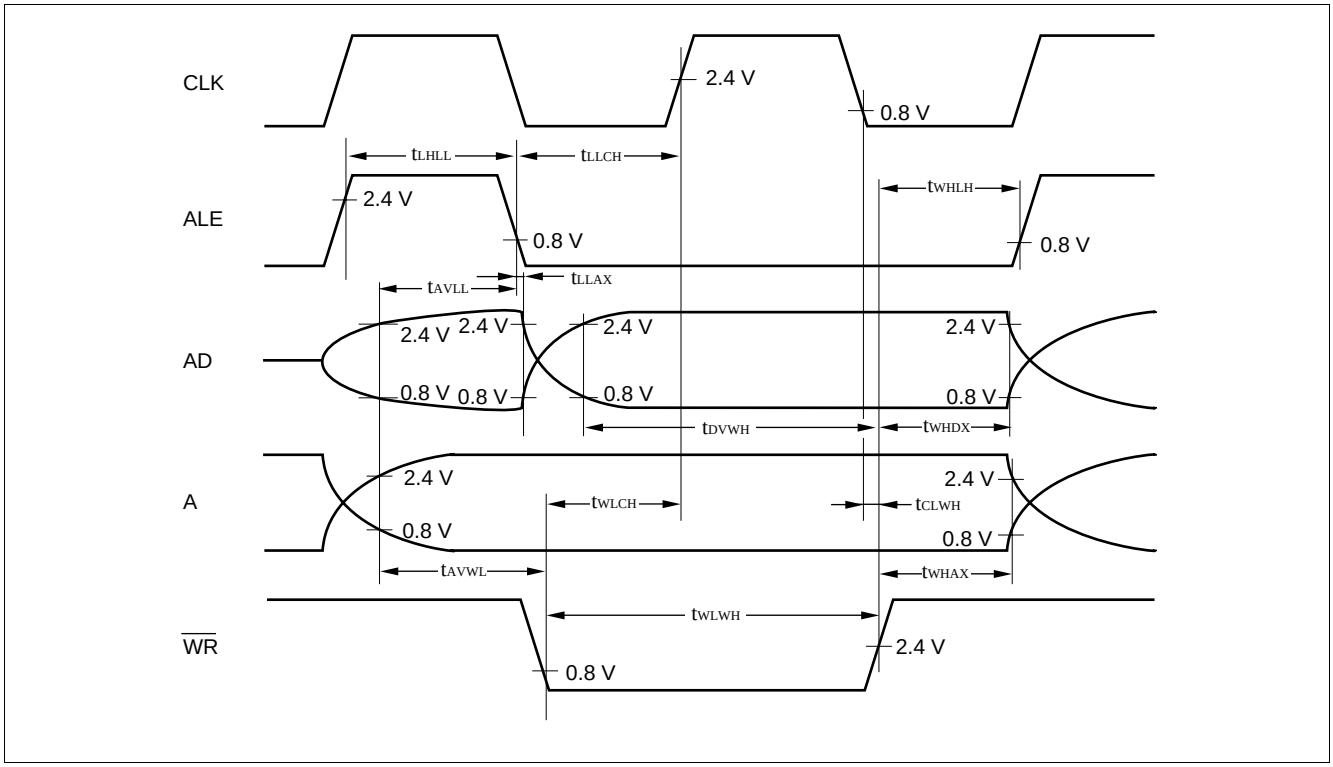
(7) Bus Write Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
Valid address → ALE ↓ time	t_{AVLL}	AD7 to AD0, ALE, A15 to A08	—	1/4 t_{inst}*2 – 0.064	—	µs	
ALE ↓ time → Address loss time	t_{LLAX}	AD7 to AD0, ALE, A15 to A08		5*1	—	ns	
Valid address → $\overline{WR}$ ↓ time	t_{AVWL}	$\overline{WR}$, ALE		1/4 t_{inst}*2 – 0.06	—	µs	
$\overline{WR}$ pulse width	t_{WLWH}	$\overline{WR}$		1/2 t_{inst}*2 – 0.02	—	µs	
Writing data → $\overline{WR}$ ↑ time	t_{DVWL}	AD7 to AD0, $\overline{WR}$		1/2 t_{inst}*2 – 0.06	—	µs	
$\overline{WR}$ ↑ → Address loss time	t_{WHAX}	$\overline{WR}$, A15 to A08		1/4 t_{inst}*2 – 0.04	—	µs	
$\overline{WR}$ ↑ → Data hold time	t_{WHDX}	AD7 to AD0, $\overline{WR}$		1/4 t_{inst}*2 – 0.04	—	µs	
$\overline{WR}$ ↑ → ALE ↑ time	t_{WHLH}	$\overline{WR}$, ALE		1/4 t_{inst}* – 0.04	—	µs	
$\overline{WR}$ ↓ → CLK ↑ time	t_{WLCH}	$\overline{WR}$, CLK		1/4 t_{inst}*2 – 0.04	—	µs	
CLK ↓ → $\overline{WR}$ ↑ time	t_{CLWH}	$\overline{WR}$, CLK		0	—	ns	
ALE pulse width	t_{LHLL}	ALE		1/4 t_{inst}*2 – 0.035	—	µs	
ALE ↓ → CLK ↑ time	t_{LLCH}	ALE, CLK		1/4 t_{inst}*2 – 0.03	—	µs	

*1: These characteristics are also applicable to the bus read timing.

*2: For information on t_{inst}, see “(4) Instruction Cycle.”

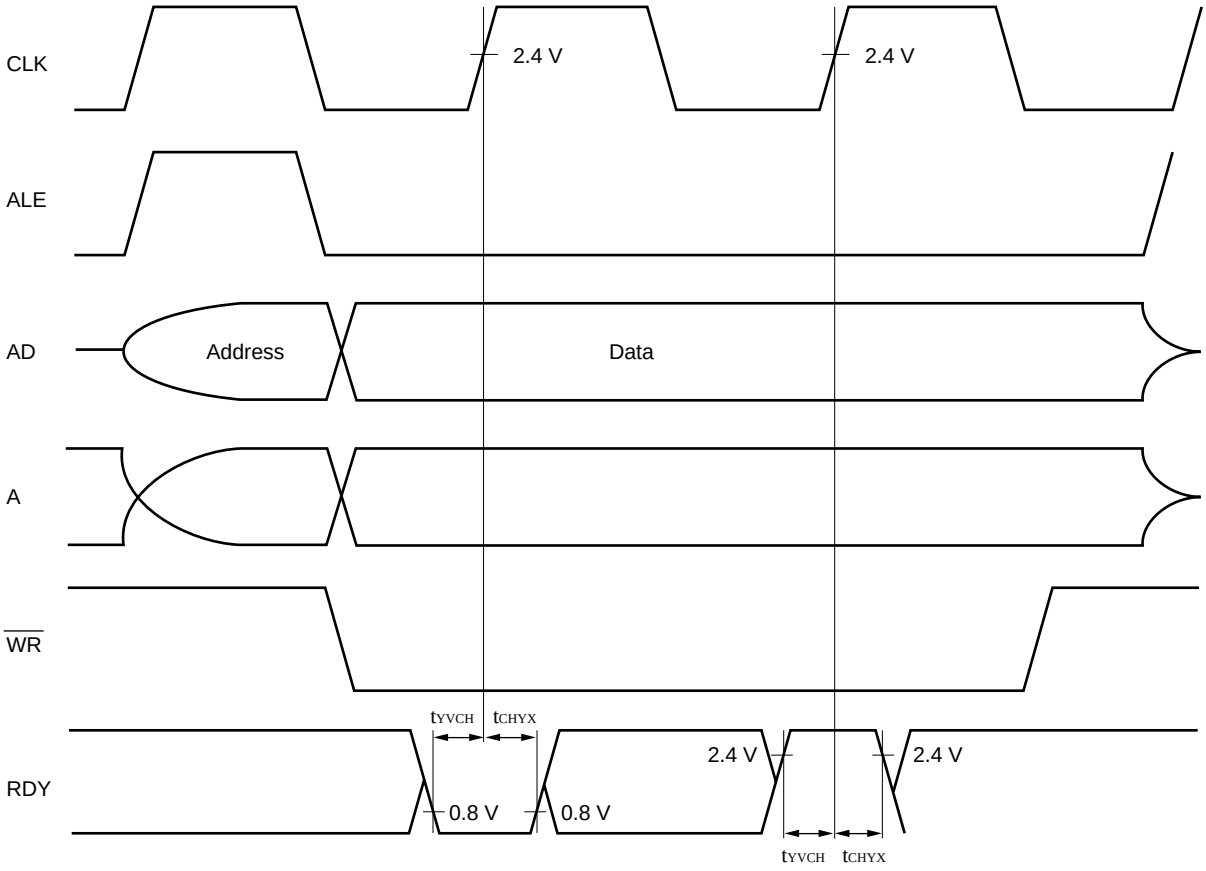


(8) Ready Input Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
RDY valid → CLK ↑ time	t_{YVCH}	RDY, CLK	—	60	—	ns	*
CLK ↑ → RDY loss time	t_{CHYX}	RDY, CLK		0	—	ns	*

* : These characteristics are also applicable to the read cycle.



Note: The bus cycle is also extended in the read cycle in the same manner.

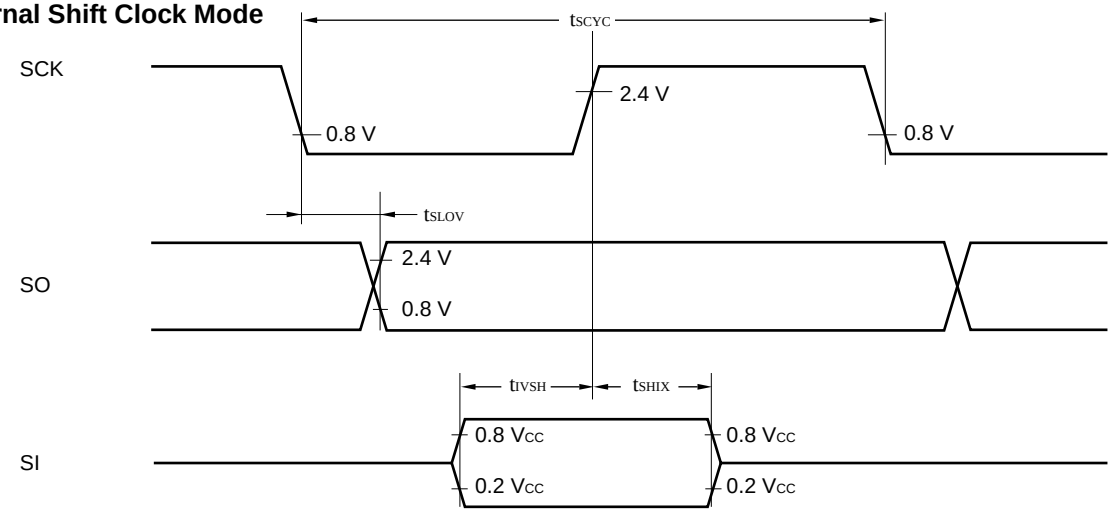
(9) Serial I/O Timing

(AV_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

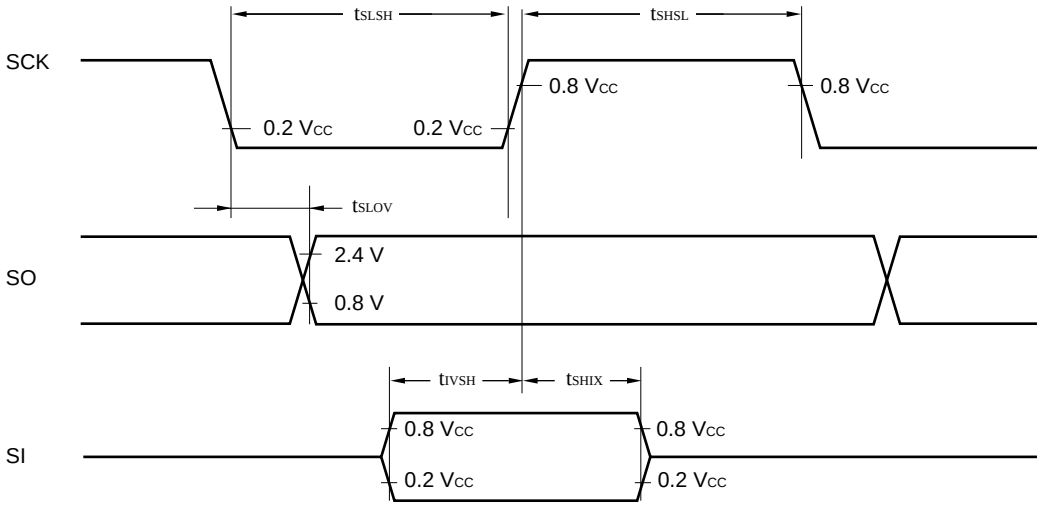
Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**

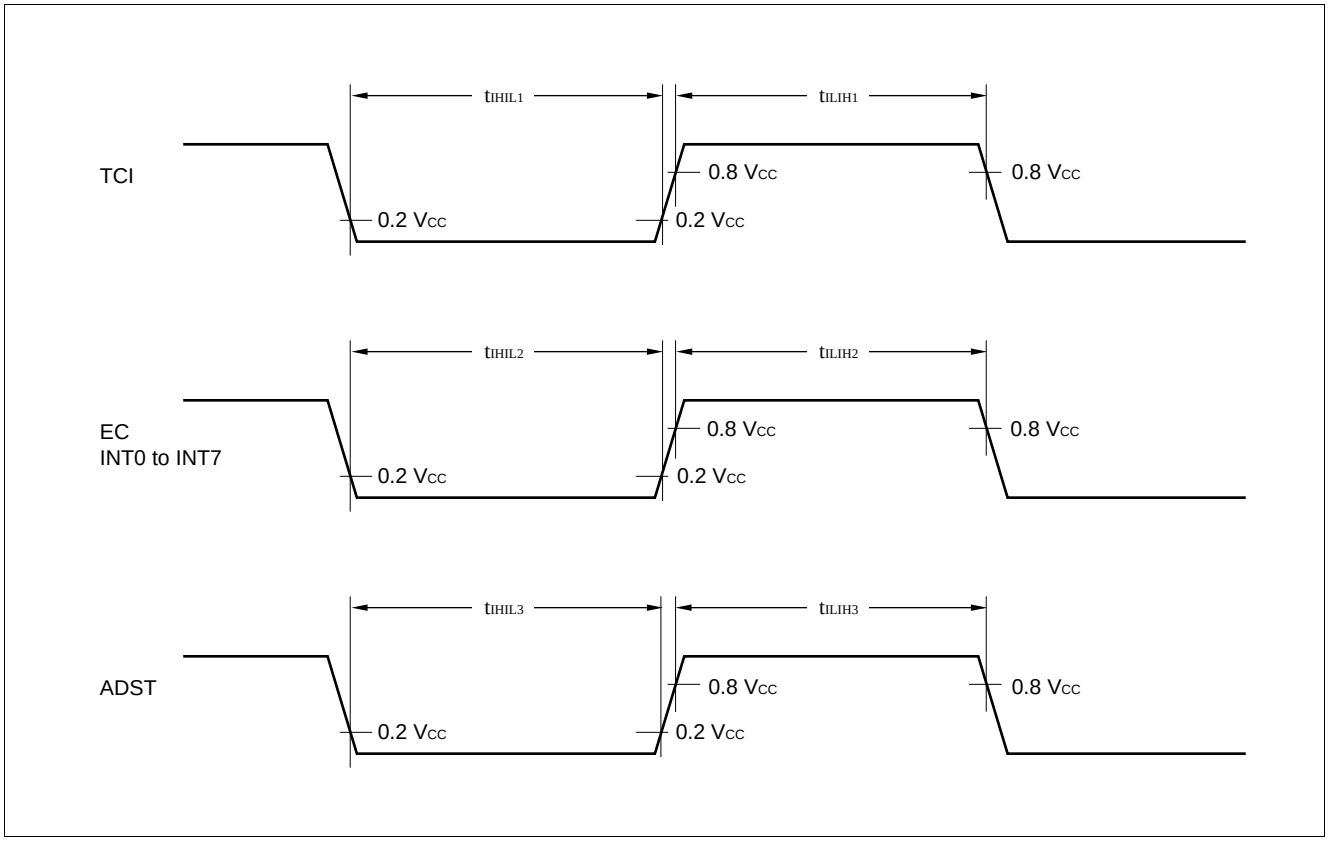


(10) Peripheral Input Timing

(AV_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	TCI	—	1 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}	TCI		1 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	EC, INT0 to INT7		2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}	EC, INT0 to INT7		2 t_{inst}*	—	µs	
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	A/D mode	64 t_{inst}*	—	µs	
Peripheral input “L” pulse width 3	t_{IHIL3}	ADST		64 t_{inst}*	—	µs	
Peripheral input “H” pulse width 3	t_{ILIH3}	ADST	Sense mode	64 t_{inst}*	—	µs	
Peripheral input “L” pulse width 3	t_{IHIL3}	ADST		64 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

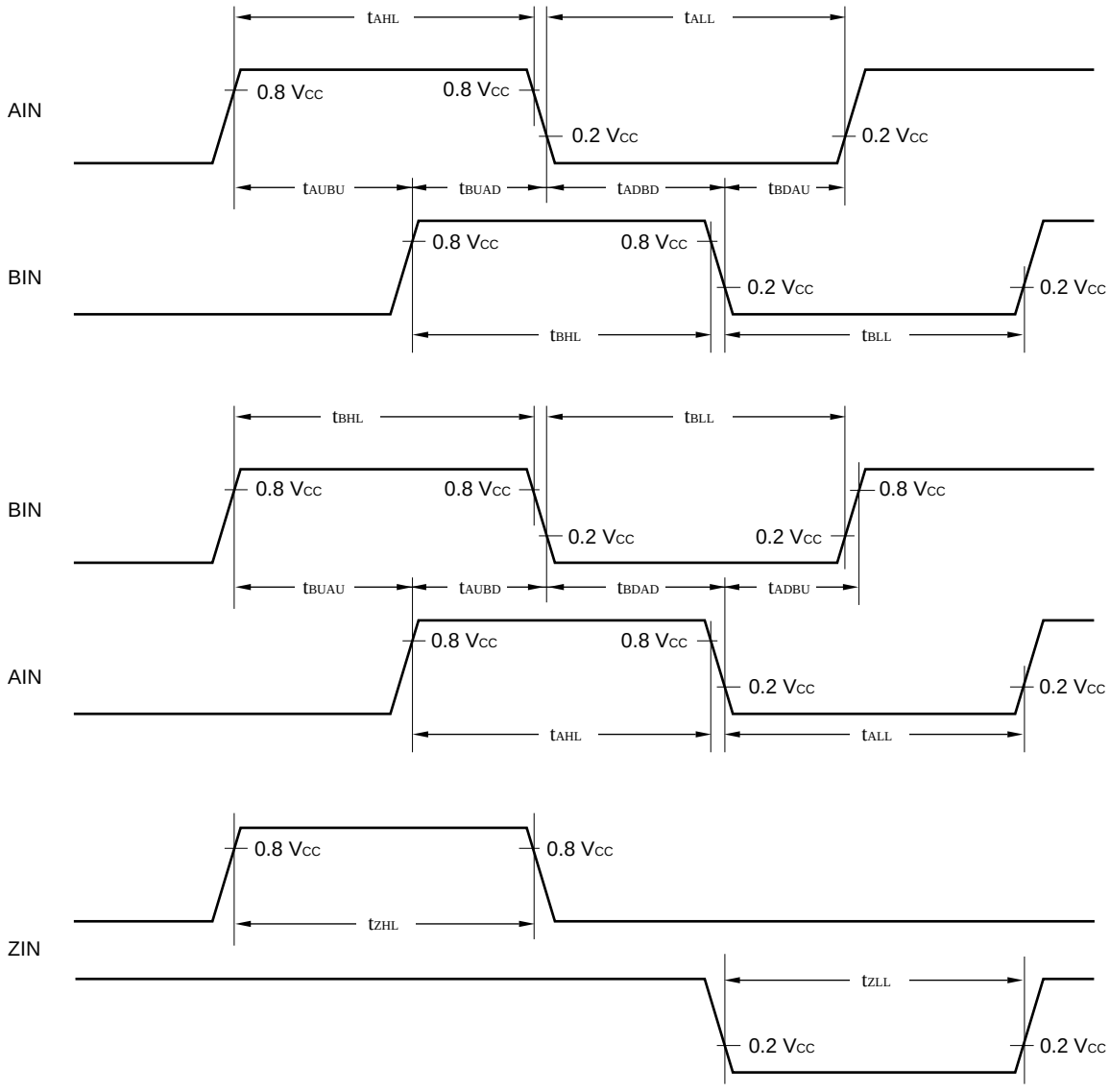


(11) Up/down Counter Input Timing

(AV_{CC} = V_{CC} = 5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Rated value		Unit	Remarks
				Min.	Max.		
AIN input “1” pulse width	t_{AHL}	P33, P34, P36, P37	—	2 t_{inst}*	—	µs	
AIN input “0” pulse width	t_{ALL}			2 t_{inst}*	—	µs	
BIN input “1” pulse width	t_{BHL}			2 t_{inst}*	—	µs	
BIN input “0” pulse width	t_{BLL}			2 t_{inst}*	—	µs	
AIN ↑ → BIN ↑ time	t_{AUBU}			1 t_{inst}*	—	µs	
BIN ↑ → AIN ↓ time	t_{BUAD}			1 t_{inst}*	—	µs	
AIN ↓ → BIN ↓ time	t_{ADBD}			1 t_{inst}*	—	µs	
BIN ↓ → AIN ↑ time	t_{BDAU}			1 t_{inst}*	—	µs	
BIN ↑ → AIN ↑ time	t_{BUAU}			1 t_{inst}*	—	µs	
AIN ↑ → BIN ↓ time	t_{AUBD}			1 t_{inst}*	—	µs	
BIN ↓ → AIN ↓ time	t_{BDAD}			1 t_{inst}*	—	µs	
AIN ↓ → BIN ↑ time	t_{ADBU}			1 t_{inst}*	—	µs	
ZIN input “1” pulse width	t_{ZHL}	P32, P35		1 t_{inst}*	—	µs	
ZIN input “0” pulse width	t_{ZLL}			1 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”


AIN
BIN
BIN
AIN
ZIN
tAHL
tALL
tAUBU
tBUAD
tADBD
tBDAU
tBHL
tBLL
tBUAU
tAUBD
tBDAD
tADBU
tZHL
tZLL
0.8 VCC
0.2 VCC

5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC}$ = 3.5 V to 6.0 V, F_C = 10 MHz, $AV_{SS} = V_{SS}$ = 0.0 V, T_A = –40°C to +85°C)

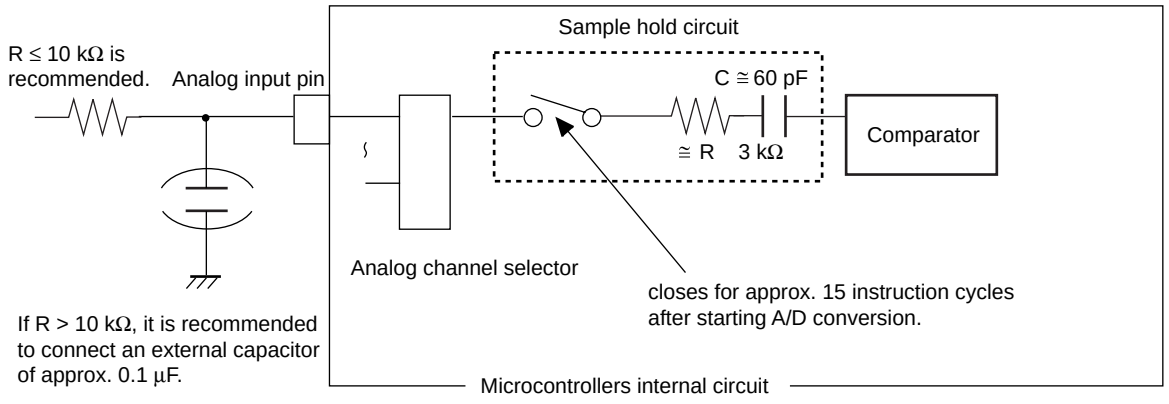
Parameter	Symbol	Pin name	Rated value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	
Linearity error			—	—	±2.0	LSB	AV_{CC} = AVR = V_{CC}
Differential linearity error			—	—	±1.5	LSB	
Total error			—	—	±3.0	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV	
Interchannel disparity	—	—	—	—	4	LSB	
A/D mode conversion time			—	—	13.2	µs	At 10 MHz oscillation
Sense mode conversion time			—	—	7.2	µs	At 10 MHz oscillation
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	—	AN0 to AN7	0	—	AVR	V	
Reference voltage		AVR	0	—	AV_{CC}	V	
Reference voltage supply current	I_R	AVR	—	200	—	µA	AVR = 5.0 V

6. Notes on Using A/D Converter

- The smaller | AVR – AV_{SS} |, the greater the error would become relatively.
- The output impedance of the external circuit for the analog input must satisfy the following conditions: Output impedance of the external circuit < Approx. 10 kΩ If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 6 µs at 10 MHz oscillation).

  An analog input equivalent circuit is shown below.

• Analog Input Equivalent Circuit



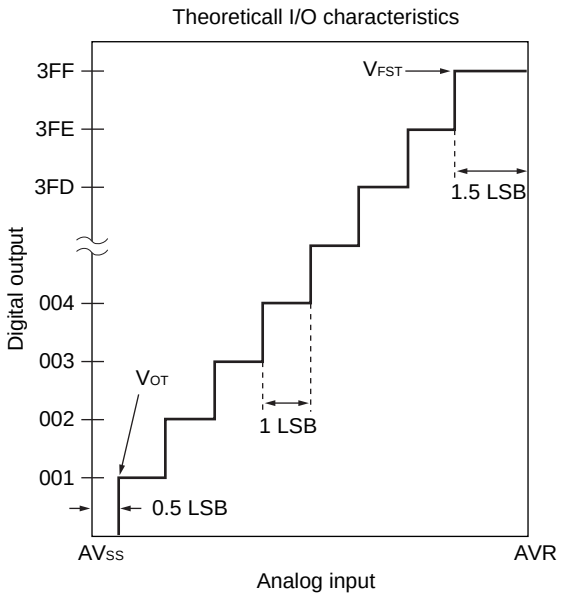
Since the A/D converter contains a sample hold circuit, the level of the analog input pin might not stabilize within the sampling period after starting A/D, resulting in inaccurate A/D conversion values, if the input impedance to the analog pin is too high. Be sure to maintain an appropriate input impedance to the analog pin.

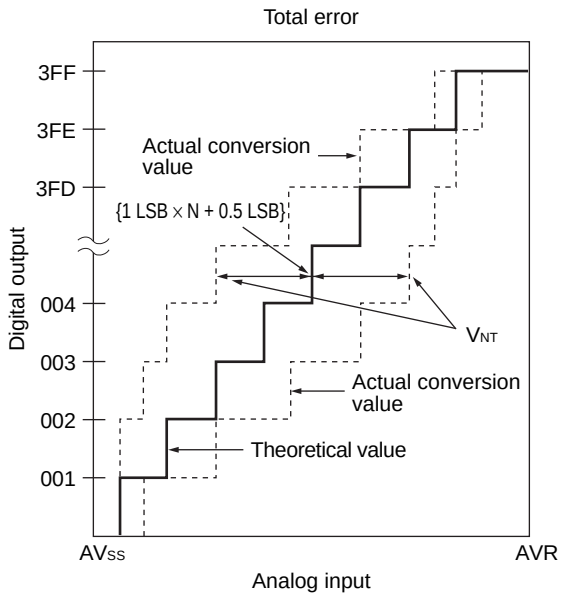
It is recommended to keep the input impedance to the analog pin from exceeding 10 kΩ. If it exceeds 10 kΩ, it is recommended to connect a capacitor of approx. 0.1 µF to the analog input pin.

Except for the sampling period after starting A/D, the input leakage current of the analog input pin is less than 10 µA.

7. A/D Converter Glossary

- Resolution
  Analog-change that are identifiable with the A/D converter.
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error
  The deviation of the input voltage needed to change the output code by 1 LSB from the theoretical voltage
- Total error
  The difference between theoretical and actual conversion values, caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise.





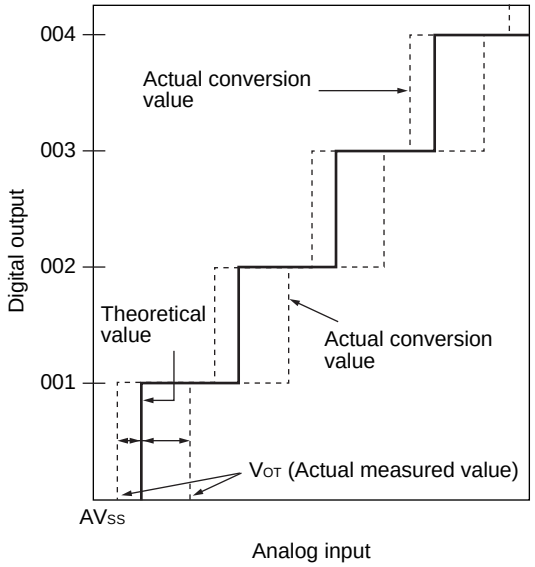
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times \text{N} + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

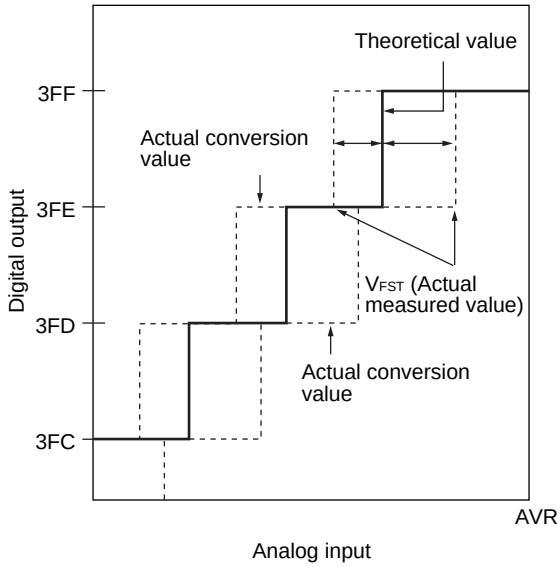
(Continued)

(Continued)

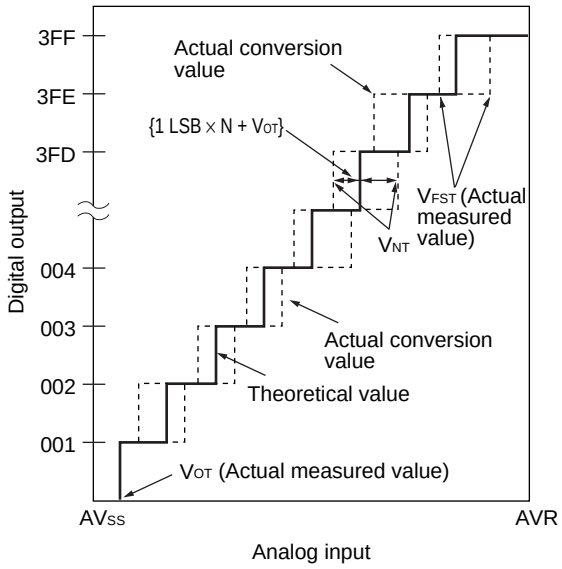
Zero transition error



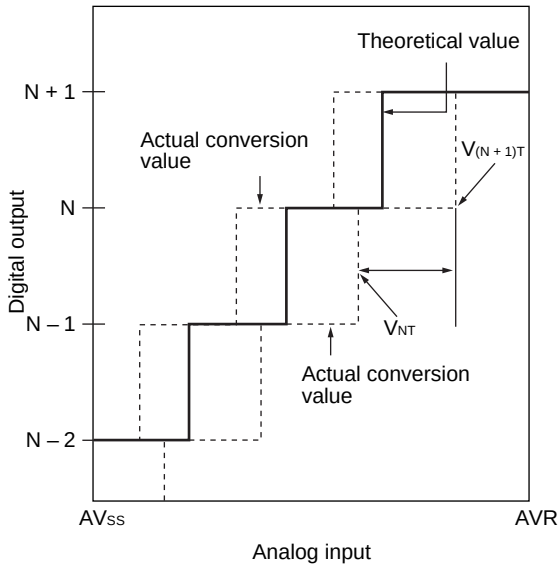
Full-scale transition error



Linearity error



Differential linearity error

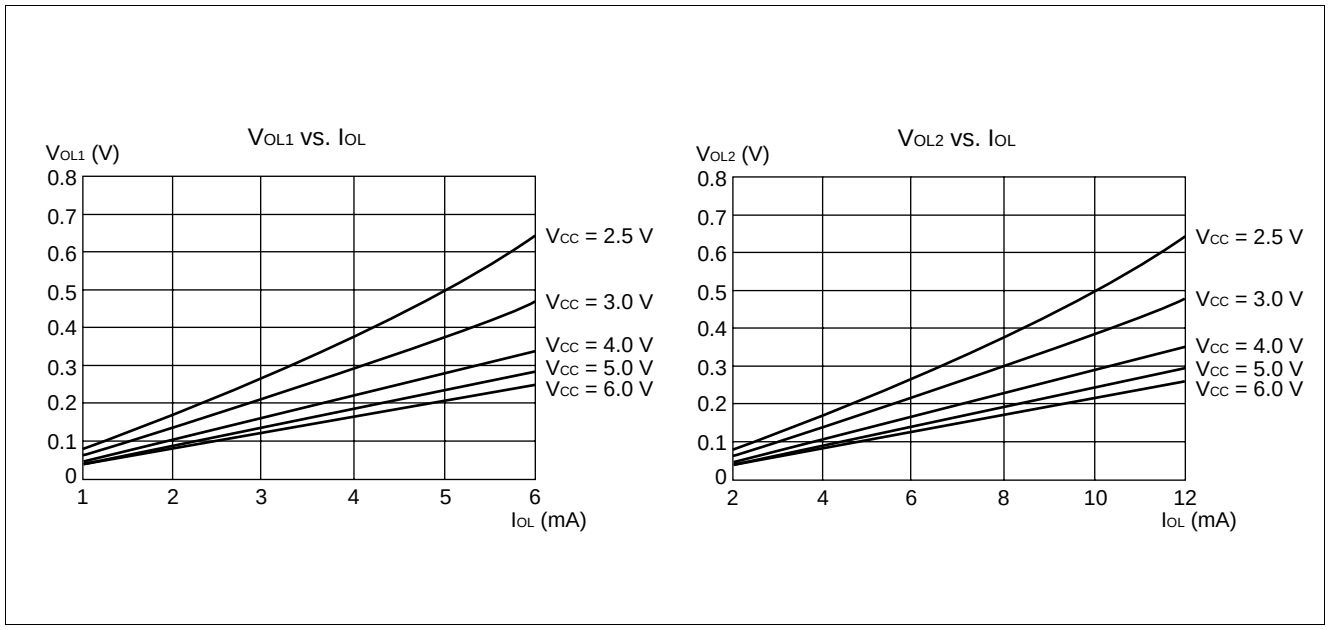


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

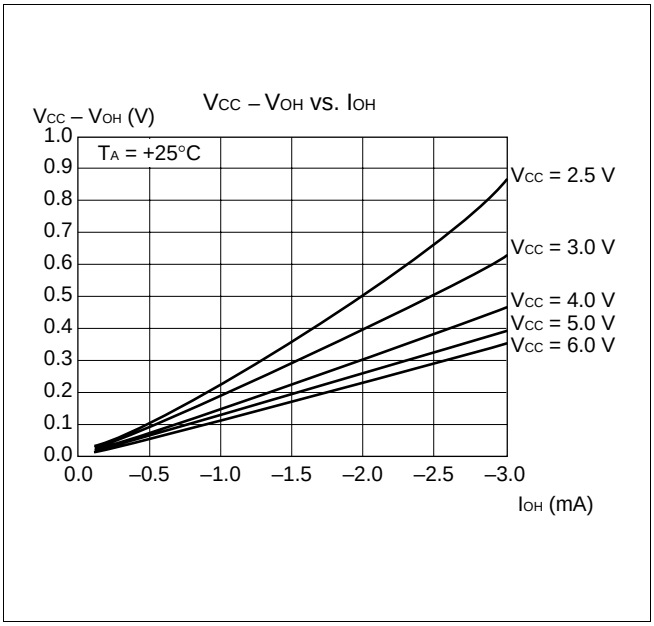
$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

■ EXAMPLE CHARACTERISTICS

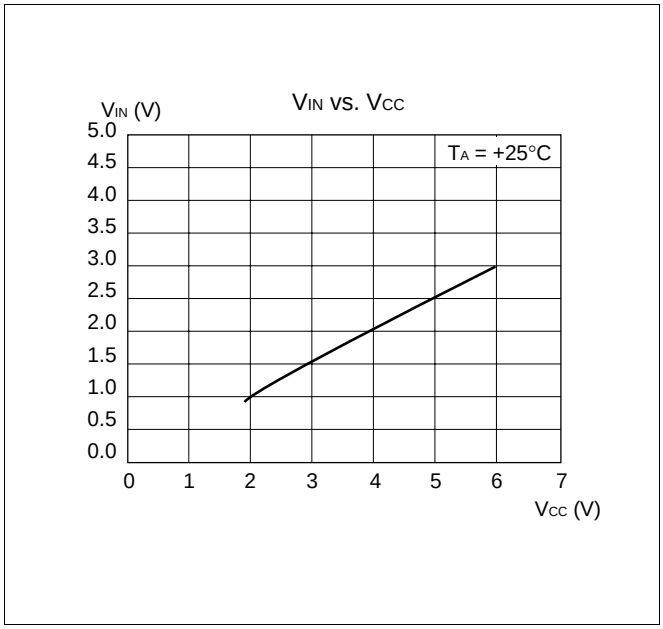
(1) “L” Level Output Voltage



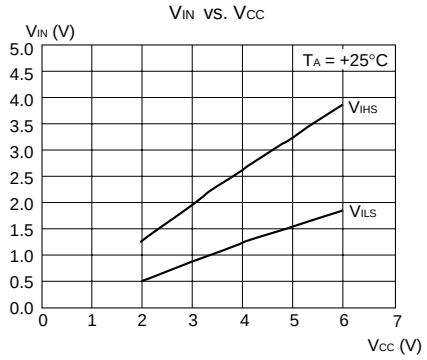
(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (CMOS Input)

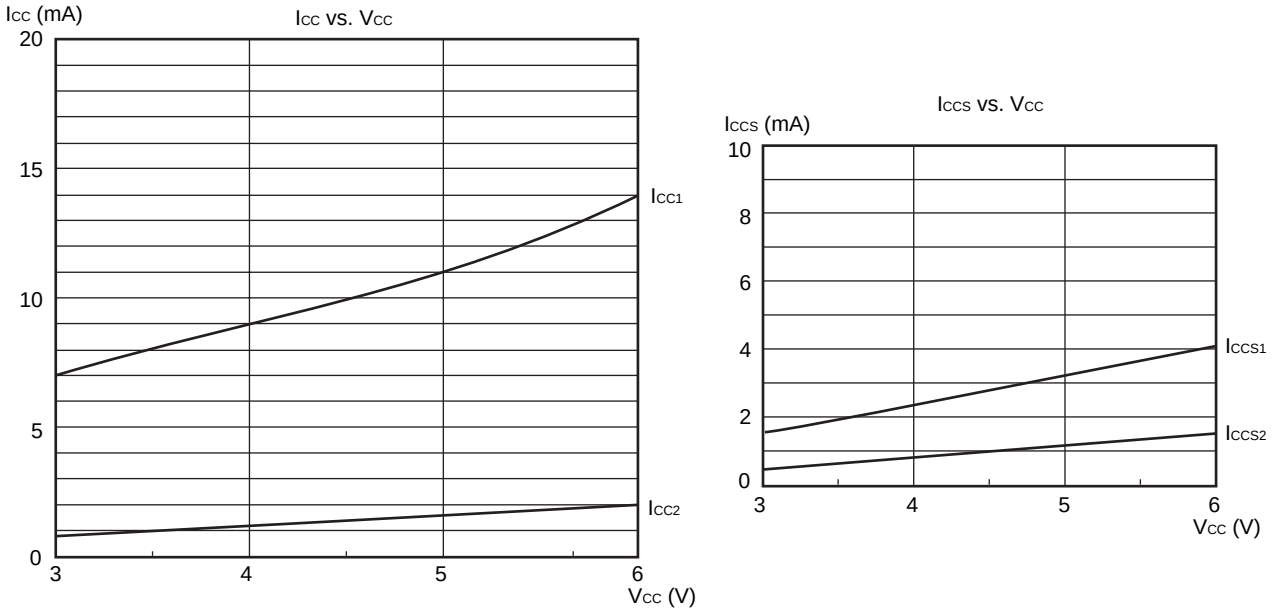


(4) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

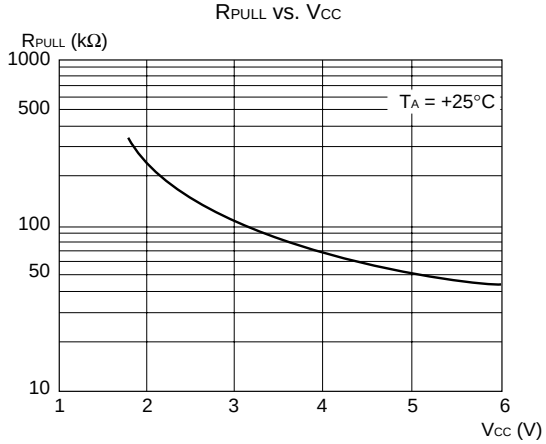


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(5) Power Supply Current (External Clock)



(6) Pull-up Resistance



■ INSTRUCTIONS (136 instructions)

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8/3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (e.g.: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	indicates that the contents at address '×' is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The contents addressed by the contents at address '×' is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions. An instruction cycle consists of 2 machine cycles.

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A changed contents of the TL, TH and AH when instruction is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the upper 8 bits of the data in the operation.
- AL and AH must become the contents of AL and AH each prior to the instruction executed.
- "00" becomes "00".

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

e.g.: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, the data transfered at “T ← A” is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A@,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

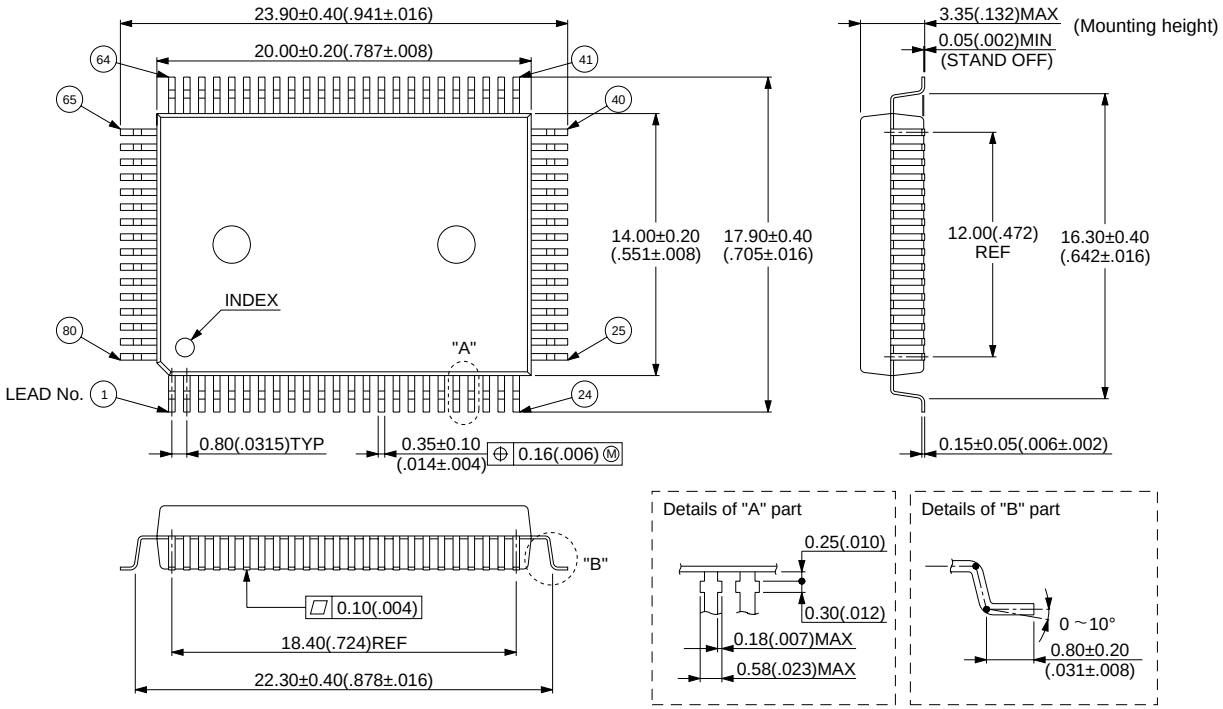
No.	Part number	MB89673R MB89673AR MB89675R MB89675AR MB89677AR	MB89P677A	MB89PV670A
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P10 to P17, P30 to P37, P40 to P47, P70 to P76	Selectable by pin	Selectable by pin	Fixed to “without pull-up resistor”
2	Pull-up resistors P00 to P03	Selectable by pin	Selectable in 4-pin unit	
3	Pull-up resistors P04 to P07	Selectable by pin	Selectable in 4-pin unit	
4	Power-on reset With power-on reset Without power-on reset	Selectable	Selectable	Fixed to “with power-on reset”
5	Oscillation stabilization time selection (at 10 MHz) Approx. $2^{18}/F_C$ (approx. 26.2 ms) Approx. $2^{17}/F_C$ (approx. 13.1 ms) Approx. $2^{14}/F_C$ (approx. 1.6 ms) Approx. $2^4/F_C$ (approx. 0 ms) F_C: Clock frequency	Selectable	Selectable	Fixed to Approx. $2^{18}/F_C$ (Approx. 26.2 ms)
6	Reset pin output With reset output Without reset output	Selectable	Selectable	Fixed to “with reset output”

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89673RPF MB89673ARPF MB89675RPF MB89675ARPF MB89677ARPF MB89P677APF	80-pin Plastic QFP (FPT-80P-M06)	
MB89673RPFM MB89673ARPFM MB89675RPFM MB89675ARPFM MB89677ARPFM MB89P677APFM	80-pin Plastic LQFP (FPT-80P-M11)	
MB89PV670ACF	80-pin Ceramic MQFP (MQP-80C-P01)	

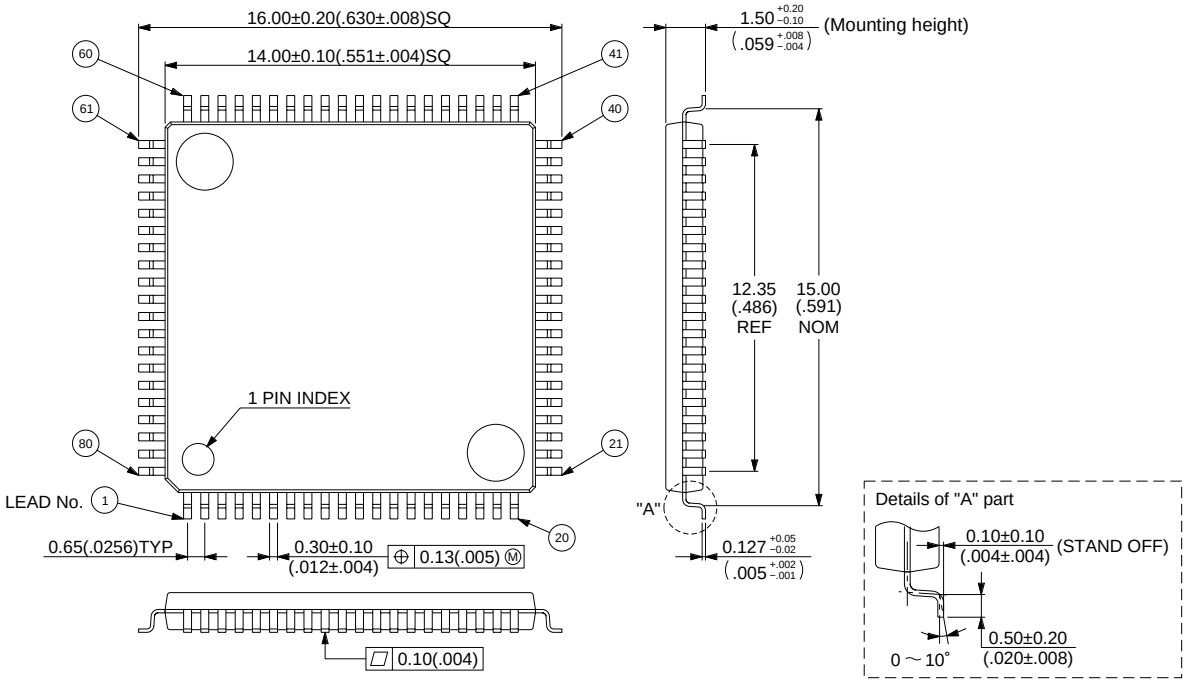
■ PACKAGE DIMENSIONS

80-pin Plastic QFP
(FPT-80P-M06)



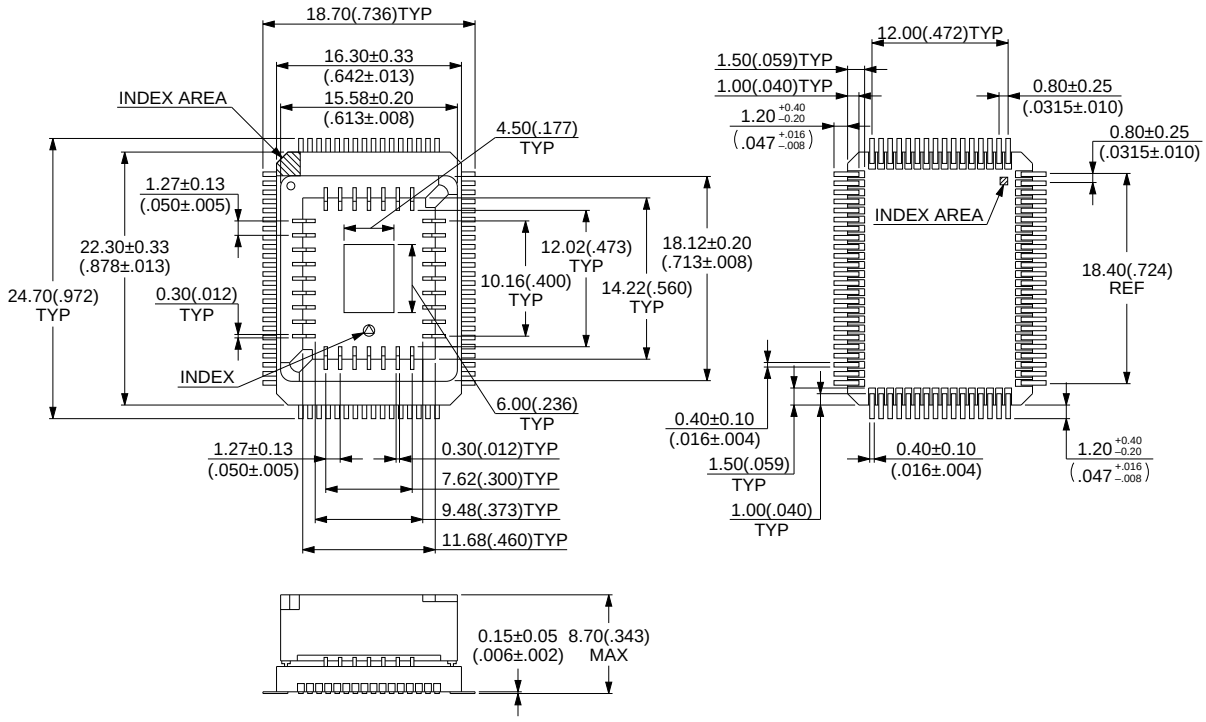
Dimensions in mm (inches)

80-pin Plastic LQFP
(FPT-80P-M11)



Dimensions in mm (inches)

80-pin Ceramic MQFP
(MQP-80C-P01)



Dimensions in mm (inches)

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