

8-bit Proprietary Microcontrollers

CMOS

F²MC-8L MB89890 Series

MB89898/899/P899/PV890

■ OUTLINE

The MB89890 series is a line of single-chip microcontrollers containing a great variety of peripheral functions such as dual clock control systems, 4-stage operating speed controller, DTMF signal generator, timer, PWM timer, serial interface, modem, A/D converter and external interrupt, as well as compact instruction set.

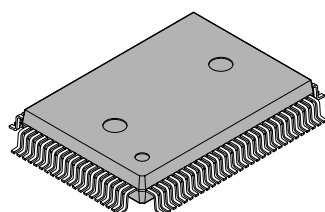
■ FEATURES

- F²MC-8L family CPU core
- Dual clock control system
- Maximum memory size: 64 Kbytes
- Minimum execution time: 0.5 μ s at 8 MHz
- Interrupt processing time: 4.5 μ s at 8 MHz
- I/O ports: Max 85 ports
- 21-bit time-base counter
- 8-bit PWM timer
- DTMF generator
- 8/16-bit timer
- 8-bit serial I/O
- Serial I/O with 1-byte buffer

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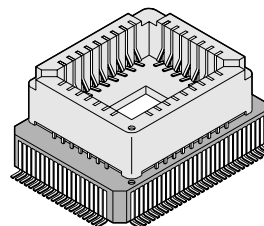
■ PACKAGES

100-pin Plastic QFP



(FPT-100P-M06)

100-pin Ceramic MQFP



(MQP-100C-P01)

MB89890 Series

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- A/D converter
- Modem timer (pulse-width counter)
- Modem signal output
- External interrupt: 16 channels
- Power-on reset function
- Low-power consumption modes (subclock mode, watch mode, sleep mode, stop mode)
- CMOS technology

■ PRODUCT LINEUP

Part number Item	MB89898	MB89899	MB89P899	MB89PV890
Classification	Mass-produced products (mask ROM products)		One-time product OTPROM product	Piggyback/ evaluation product (for development)
ROM size	48 K × 8 bits (internal mask ROM)	60 K × 8 bits (internal mask ROM)	60 K × 8 bits (internal OTPROM)	60 K × 8 bits (external ROM)
RAM size	1.5 K × 8 bits	2.0 K × 8 bits		
Instruction bit length	8 bits			
Instruction length	1 to 3 bytes			
Data bit length	1, 8, 16 bits			
The number of instructions	136			
Clock generator	Internal			
Minimum execution time	0.5 μs at 8 MHz to 8 μs at 8 MHz, 61 μs at 32.768 kHz			
Interrupt processing time	4.5 μs at 8 MHz to 72 μs at 8 MHz, 549.3 μs at 32.768 kHz			
Ports () indicate shared function ports.	General-purpose output ports (N-ch open-drain): 21 (8) General-purpose output ports (CMOS): 8 (0) General-purpose I/O ports (N-ch open-drain): 8 (6) General-purpose I/O ports (CMOS): 48 (29) Total: 85 (43)			
PWM timer	8 bits × 1 channel			
Timer/counter	8 bits × 2 channels or 16 bits × 1 channel			
Serial I/O	8-bit serial I/O (with 1-byte buffer) × 1			
A/D converter	8 bits × 8 channels			
DTMF generator	CCITT all-tone output capable (1 to 0 ₍₁₀₎ , *, #, A to D) Single-tone output capable			
Soft modem receiving timer	5-bit noise reduction circuit + pulse-width measurement timer			

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Part number Item	MB89898	MB89899	MB89P899	MB89PV890
Soft modem transmitting circuit	approximately 1208 bps, approximately 2415 bps modem output			
External interrupt	16			
Time-base timer	21 bits			
Watch prescaler	15 bits			
Standby mode	Watch mode, subclock mode, sleep mode, stop mode			
Process	CMOS			
Operating voltage*	2.2 V to 6.0 V		2.7 V to 6.0 V	
EPROM for use				MBM27C512-20TV

*: Varies with conditions such as operating frequencies.

■ PACKAGE AND CORRESPONDING MODELS

Package	MB89898 MB89899 MB89P899	MB89PV890
FPT-100P-M06	○	×
MQP-100C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see “■ PACKAGE DIMENSIONS”.

■ DIFFERENCES AMONG MODELS

1. Memory Size

Before evaluating using the piggyback model, verify its difference from the model that will actually be used.

2. Current Consumption

- In the case of the MB89PV890, added is the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed the product with an OTPROM (EPROM) will consume more current than the product with a mask ROM. However, the same is current consumption in sleep/stop mode.

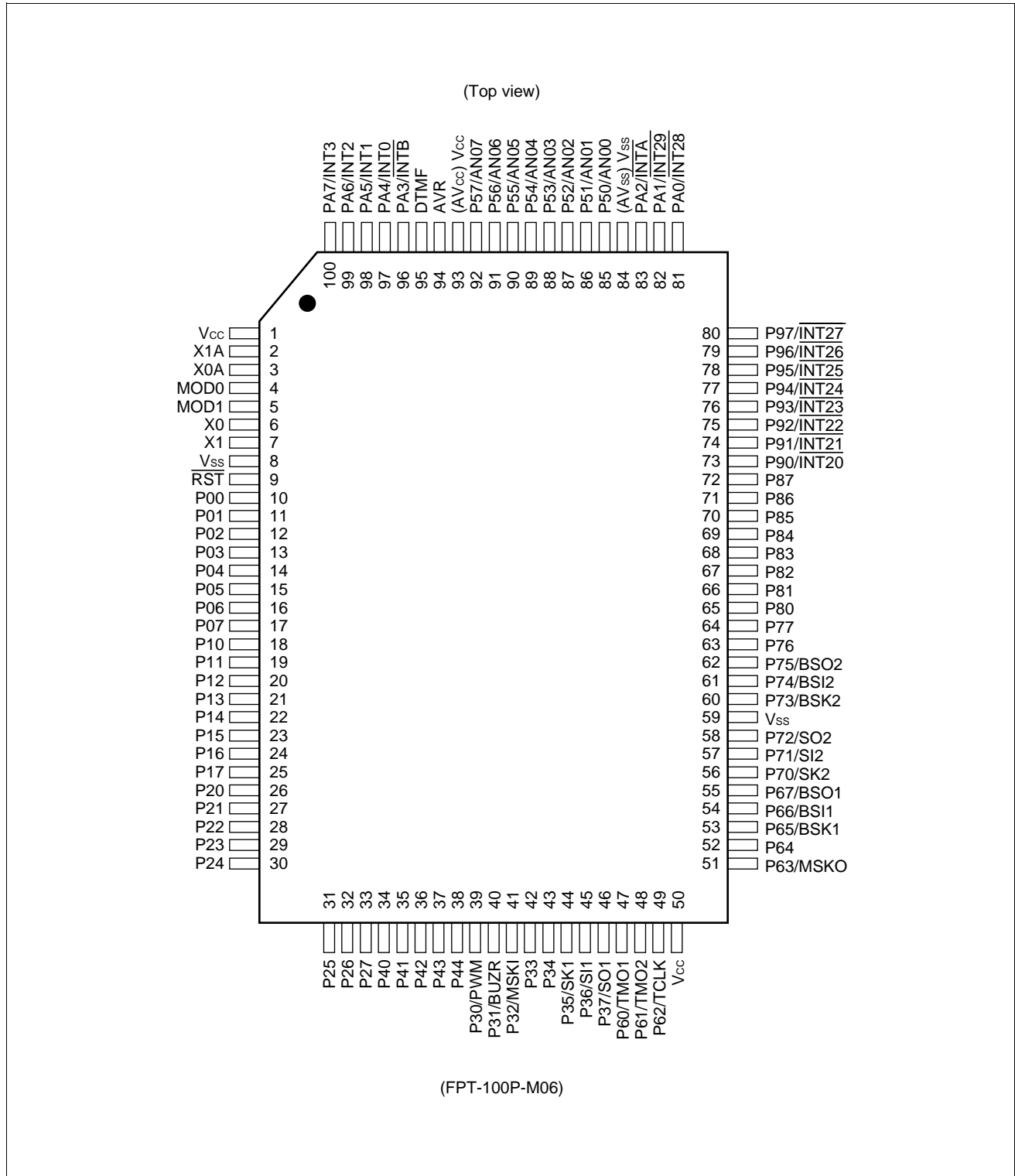
3. Mask Options

Functions that can be selected as options and how to designate these options vary with product. Before using options, check “■ MASK OPTIONS”. Take particular care on the following points:

- Options are fixed on the MB89PV890.
- Pull-up resistor options on the MB89P899 are in 2-bit units for P00 to P07, P10 to P17, P60 to P67, P90 to P97, and PA0 to PA7. Options are in 1-bit units for P40 to P44, P70 to P77, P80 to P87.

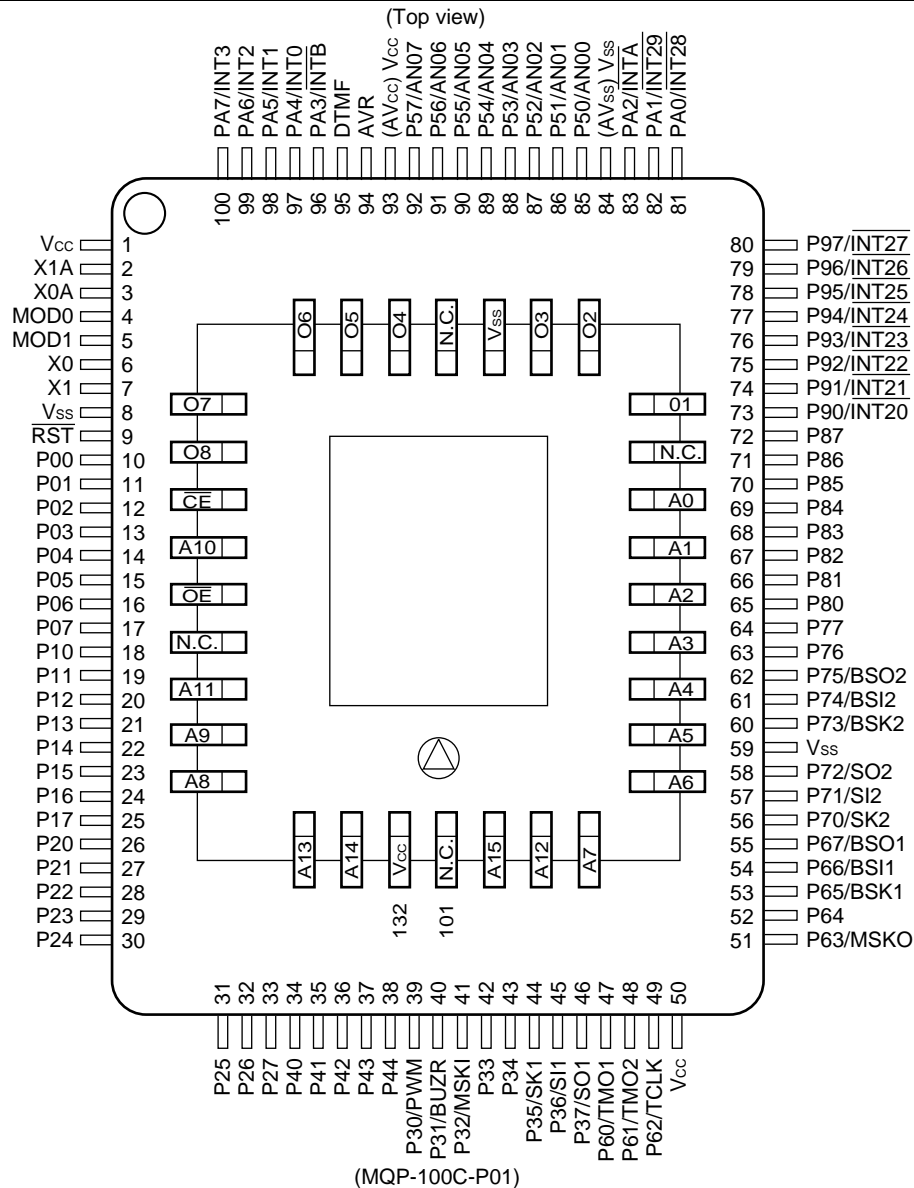
MB89890 Series

PIN ASSIGNMENTS



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• Pin assignment on package top (MB89PV890 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
101	N.C.	109	A2	117	N.C.	125	OE
102	A15	110	A1	118	O4	126	N.C.
103	A12	111	A0	119	O5	127	A11
104	A7	112	N.C.	120	O6	128	A9
105	A6	113	O1	121	O7	129	A8
106	A5	114	O2	122	O8	130	A13
107	A4	115	O3	123	CE	131	A14
108	A3	116	V _{ss}	124	A10	132	V _{cc}

N.C.: Internally connected. Do not use.

MB89890 Series

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
QFP*1, MQP*2			
6	X0	A	Crystal oscillator pins (8 MHz)
7	X1		
3	X0A	B	Crystal oscillator pins (32.768 kHz)
2	X1A		
4	MOD0	C	Operation mode select pins Connect to V _{SS} (GND) when using.
5	MOD1		
9	$\overline{\text{RST}}$	D	Reset input pin
10 to 17	P00 to P07	E	General-purpose I/O ports
18 to 25	P10 to P17	E	General-purpose I/O ports
26 to 33	P20 to P27	G	General-purpose I/O ports
39	P30/PWM	F	General-purpose I/O port Also serves as an 8-bit PWM.
40	P31/BUZR	F	General-purpose I/O port Also serves as a buzzer output.
41	P32/MSKI	F	General-purpose I/O port Also serves as a modem timer.
42, 43	P33, P34	F	General-purpose I/O ports
44, 45, 46	P35/SK1, P36/SI1, P37/SO1	F	General-purpose I/O ports Also serve as an 8-bit serial I/O output 1.
34 to 38	P40 to P44	J	General-purpose I/O ports
85 to 92	P50/AN00 to P57/AN07	H	General-purpose output ports Also serve as an analog input.
47, 48, 49	P60/TMO1, P61/TMO2, P62/TCLK	F	General-purpose I/O ports Also serve as an 8/16-bit timer.
51	P63/MSKO	F	General-purpose I/O port Also serves as a modem output.
52	P64	F	General-purpose I/O port
53, 54, 55	P65/BSK1, P66/BSI1, P67/BSO1	F	General-purpose I/O ports Also serve as a serial I/O output 1 with 1-byte buffer.
56, 57, 58	P70/SK2, P71/SI2, P72/SO2	I	General-purpose I/O ports Also serve as an 8-bit serial I/O output 2.

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*1: FPT-100P-M06

*2: MQP-100C-P01

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Pin no. QFP*1, MQP*2	Pin name	Circuit type	Function
60, 61, 62	P73/BSK2, P74/BSI2, P75/BSO2	I	General-purpose I/O ports Also serve as a serial I/O output 2 with 1-byte buffer.
63, 64	P76, P77	I	General-purpose I/O ports
65 to 72	P80 to P87	J	General-purpose output ports
73 to 80	P90/ $\overline{\text{INT20}}$ to P97/ $\overline{\text{INT27}}$	F	General-purpose I/O ports External interrupt input is hysteresis input.
81, 82, 83	PA0/ $\overline{\text{INT28}}$, PA1/ $\overline{\text{INT29}}$, PA2/ $\overline{\text{INTA}}$	F	General-purpose I/O ports External interrupt input is hysteresis input.
96, 97 to 100	PA3/ $\overline{\text{INTB}}$, PA4/INT0 to PA7/INT3	F	General-purpose I/O ports External interrupt input is hysteresis input.
95	DTMF	K	DTMF signal output pin
1, 50	V _{cc}	—	Power supply pin
8, 59	V _{ss}	—	Power supply (GND) pin
93	V _{cc} (AV _{cc})	—	Power supply pin
84	V _{ss} (AV _{ss})	—	Power supply GND pin
94	AVR	—	A/D converter reference input pin

*1: FPT-100P-M06

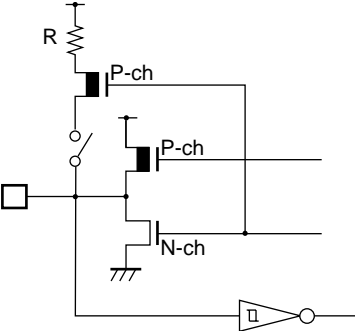
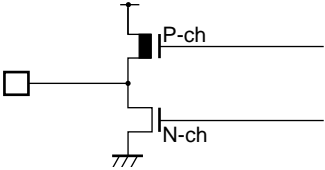
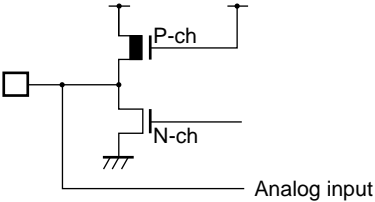
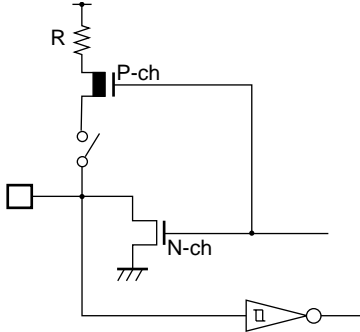
*2: MQP-100C-P01

MB89890 Series

I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	<p>Main clock control signal</p>	<p>Main clock</p> <ul style="list-style-type: none"> Oscillator feedback resistor: approximately 1 MΩ at 5 V
B	<p>Subclock control signal</p>	<p>Subclock</p> <ul style="list-style-type: none"> Oscillator feedback resistor: approximately 4.5 MΩ at 5 V
C		
D		<ul style="list-style-type: none"> Output pull-up resistor (P-ch) At approximately 50 kΩ/5 V Hysteresis input
E		<ul style="list-style-type: none"> CMOS output CMOS input Pull-up resistor optional

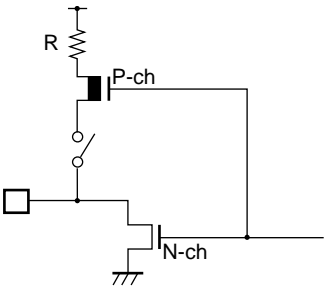
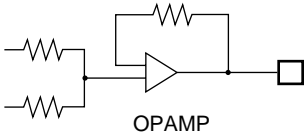
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Type	Circuit	Remarks
F		<ul style="list-style-type: none">• CMOS output• Hysteresis input• Pull-up resistor optional
G		<ul style="list-style-type: none">• CMOS output
H		<ul style="list-style-type: none">• N-ch open-drain output• Analog input
I		<ul style="list-style-type: none">• N-ch open-drain output• Hysteresis input• Pull-up resistor optional

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Type	Circuit	Remarks
J		<ul style="list-style-type: none">• N-ch open-drain output• Pull-up resistor optional
K		<ul style="list-style-type: none">• DTMF analog output

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be $AV_{CC} = DAVC = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although operation is assured within the rated range of V_{CC} power supply voltage, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required for even power-on reset (optional) and release from stop mode.

MB89890 Series

■ PROGRAMMING TO THE EPROM ON THE MB89P899

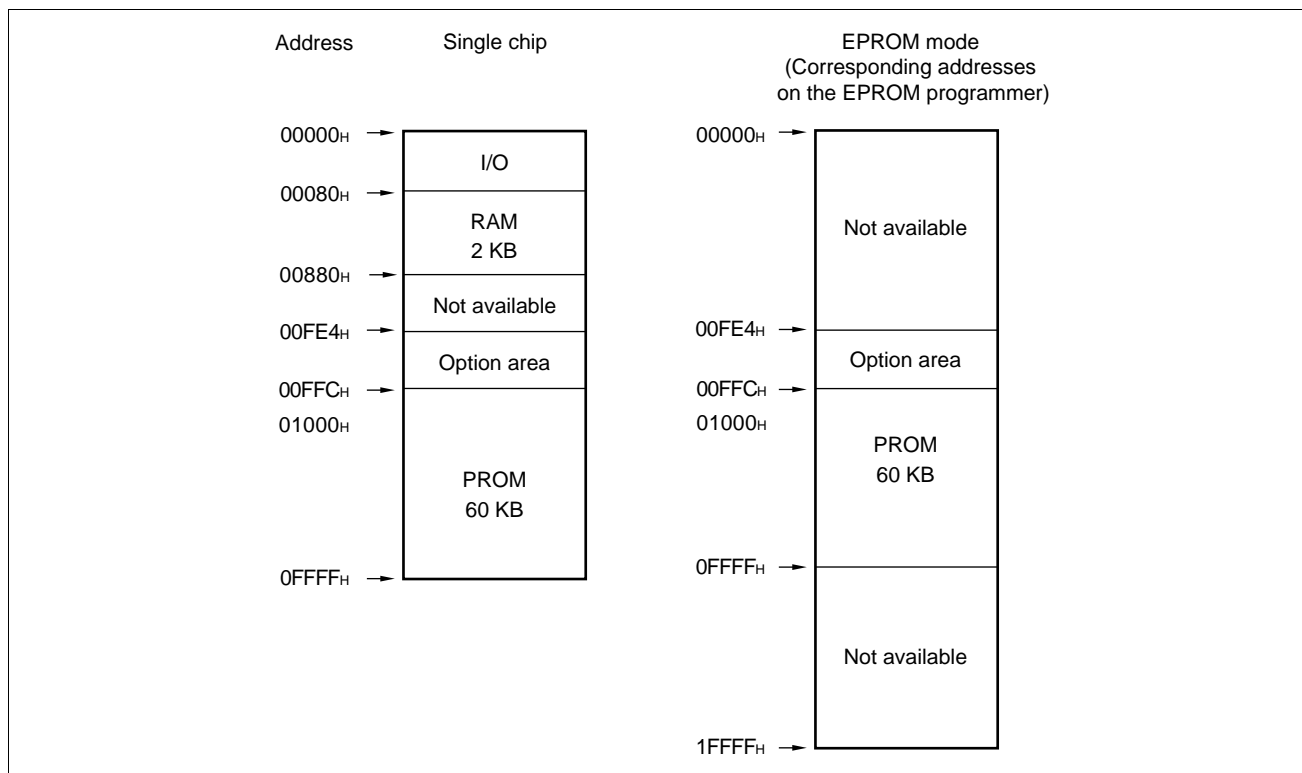
The MB89P899 is a one-time PROM version of the MB89890 series.

1. Features

- 60-Kbyte PROM on chip
- Option can be set using the EPROM programmer.
- Equivalency to the MBM27C1001, in EPROM mode (when programmed with the EPROM programmer), supports 4-byte programming mode.

2. Memory Space

Memory space in each mode such as 60-Kbyte PROM, option area is diagrammed below.



3. Programming to the EPROM

In EPROM mode the MB89P899 functions equivalent to the MBM27C1001. This allows the EPROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

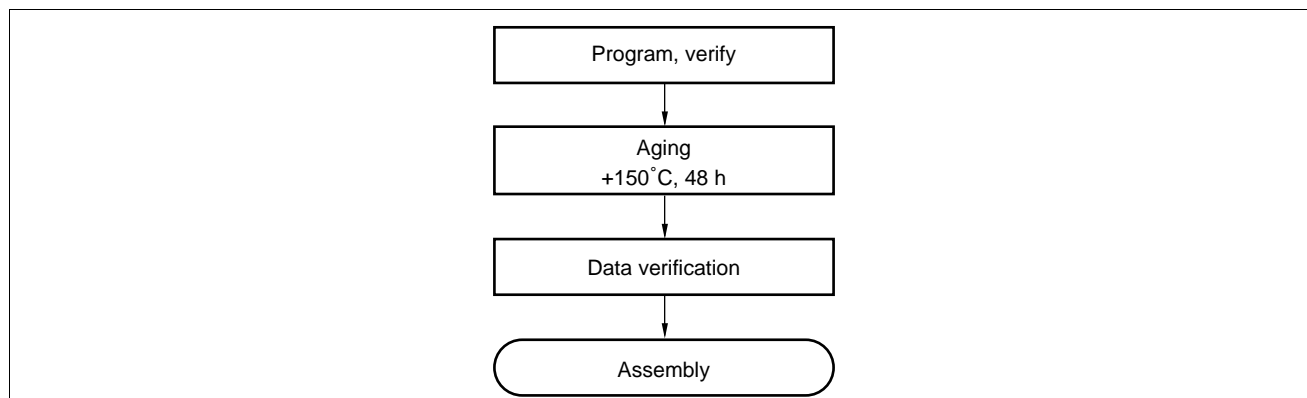
When the operating ROM area for a single chip is 60 Kbytes (01000H to 0FFFFH) the EPROM can be programmed as follows:

- Programming procedure

- (1) Set the EPROM programmer to MBM27C1001.
- (2) Load program data into the EPROM programmer at 01000H to 0FFFFH.
Load option data into addresses 00FE4H to 00FFCH. (For information about each corresponding options, see "7. Setting OTPROM Options.")
- (3) Program to 00FE4H to 00FFCH, and 01000H to 0FFFFH with the EPROM programmer.

4. Recommended Screening Conditions

High-Temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

Due to its nature, bit programming test can't be conducted as Fujitsu delivery test. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Part number	Package	Compatible socket adapter Sun Hayato Co., Ltd.
MB89P899	QFP-100	ROM-100QF-32DP-8LA

Inquiry: Sun Hayato Co., Ltd.:TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

MB89890 Series

7. Setting OTPROM Options

The programming procedure is the same as that for the program data. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map.

- PROM Option Bitmap

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00FE4 _H	Vacancy Readable and writ-able	Vacancy Readable and writ-able	Vacancy Readable and writ-able	Single/ double clock 1:2 clock systems 0:1 clock system	Reset output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Oscillation stabilization time 11 2 ¹⁸ /F _{CH} 10 2 ¹⁶ /F _{CH} 01 2 ¹² /F _{CH} 00 2 ³ /F _{CH}	
00FE8 _H	P17, P16 Pull-up 1: No 1: Yes	P15, P14 Pull-up 1: No 1: Yes	P13, P12 Pull-up 1: No 0: Yes	P11, P10 Pull-up 1: No 0: Yes	P07, P06 Pull-up 1: No 0: Yes	P05, P04 Pull-up 1: No 0: Yes	P03, P02 Pull-up 1: No 0: Yes	P01, P00 Pull-up 1: No 0: Yes
00FEC _H	P67, P66 Pull-up 1: No 0: Yes	P65, P64 Pull-up 1: No 0: Yes	P63, P62 Pull-up 1: No 0: Yes	P61, P60 Pull-up 1: No 0: Yes	P37, P36 Pull-up 1: No 0: Yes	P35, P34 Pull-up 1: No 0: Yes	P33, P32 Pull-up 1: No 0: Yes	P31, P30 Pull-up 1: No 0: Yes
00FF0 _H	PA7, PA6 Pull-up 1: No 0: Yes	PA5, PA4 Pull-up 1: No 0: Yes	PA3, PA2 Pull-up 1: No 0: Yes	PA1, PA0 Pull-up 1: No 0: Yes	P97, P96 Pull-up 1: No 0: Yes	P95, P94 Pull-up 1: No 0: Yes	P93, P92 Pull-up 1: No 0: Yes	P91, P90 Pull-up 1: No 0: Yes
00FF4 _H	Vacancy Readable and writ-able	Vacancy Readable and writ-able	Vacancy Readable and writ-able	P44 Pull-up 1: No 0: Yes	P43 Pull-up 1: No 0: Yes	P42 Pull-up 1: No 0: Yes	P41 Pull-up 1: No 0: Yes	P40 Pull-up 1: No 0: Yes
00FF8 _H	P77 Pull-up 1: No 0: Yes	P76 Pull-up 1: No 0: Yes	P75 Pull-up 1: No 0: Yes	P74 Pull-up 1: No 0: Yes	P73 Pull-up 1: No 0: Yes	P72 Pull-up 1: No 0: Yes	P71 Pull-up 1: No 0: Yes	P70 Pull-up 1: No 0: Yes
00FFC _H	P87 Pull-up 1: No 0: Yes	P86 Pull-up 1: No 0: Yes	P85 Pull-up 1: No 0: Yes	P84 Pull-up 1: No 0: Yes	P83 Pull-up 1: No 0: Yes	P82 Pull-up 1: No 0: Yes	P81 Pull-up 1: No 0: Yes	P80 Pull-up 1: No 0: Yes

Notes: • Note that option area address values are equivalent to every fourth address to accommodate 4-byte programming mode.

- Each bit is set to '1' as the initialized value, therefore the pull-up option is not selected.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

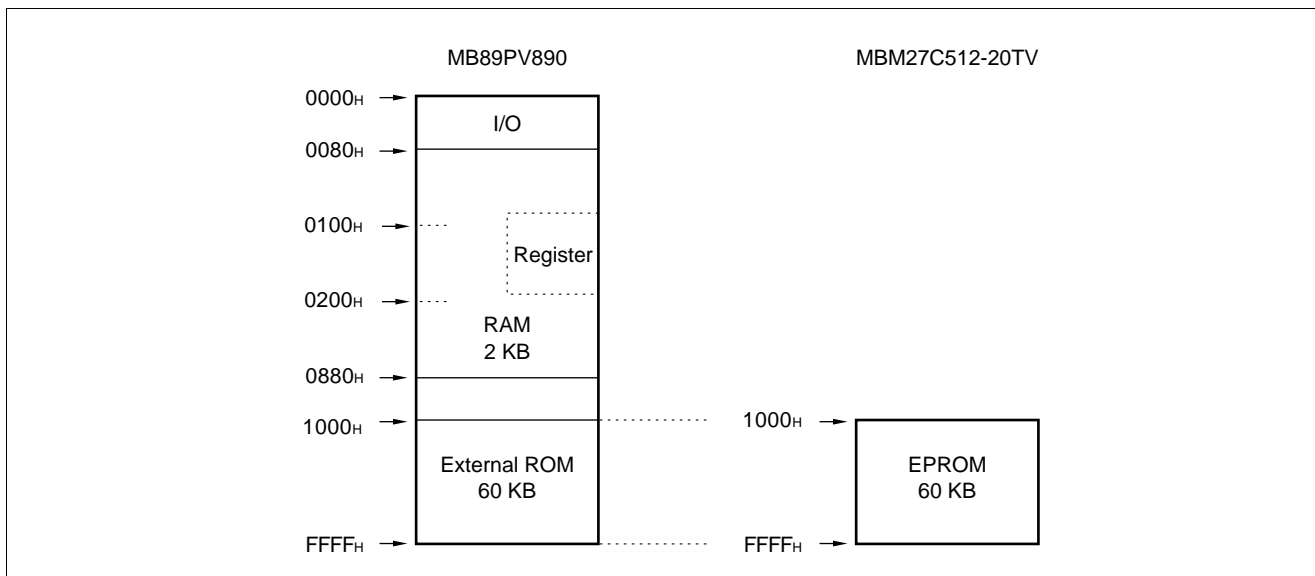
2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.:TEL (81)-3-3986-0403
FAX (81)-3-5396-9106

3. Memory Space

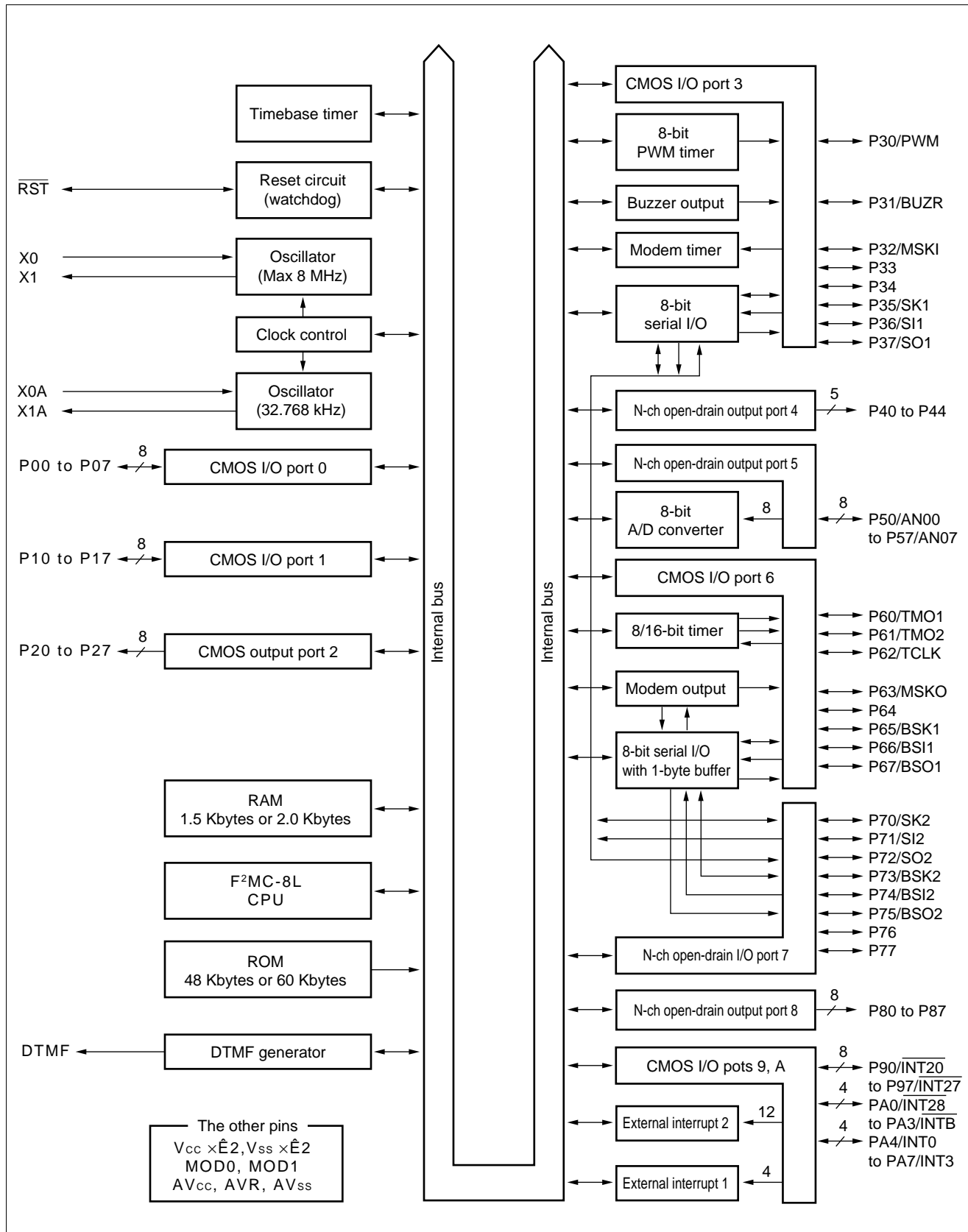


4. Programming Procedure

- (1) Set the EPROM programmer to MBM27C512-20TV.
- (2) Load program data into the EPROM programmer at 1000H to FFFFH.
- (3) Program to 1000H to FFFFH with the EPROM programmer.

MB89890 Series

■ BLOCK DIAGRAM

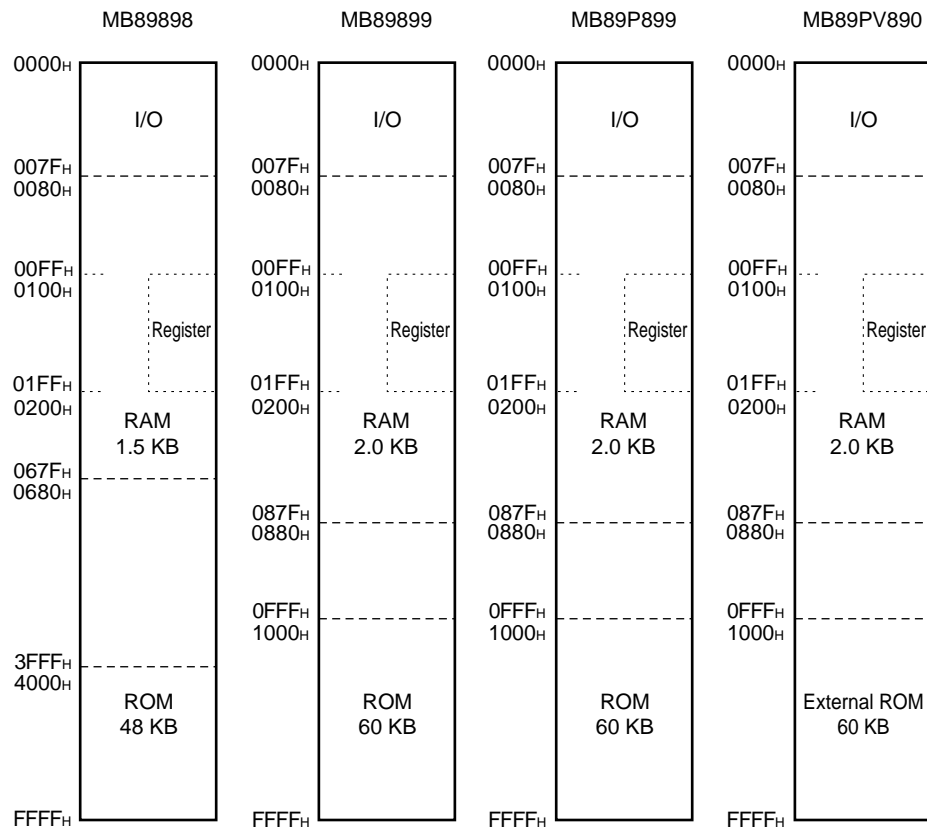


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89890 series offer 64 Kbytes of memory for storing all of I/O, data, and program areas. The I/O area is allocated from the lowest address. The data area is allocated immediately above the I/O area. The data area can be divided into register, stack, and direct areas, according to the application. The program area is allocated from exactly the opposite end, that is, near the highest address. The tables of interrupt reset vectors and vector call instructions are allocated from the highest address within the program area. The memory space of the MB89890 series is structured as illustrated below:

• Memory Space



MB89890 Series

2. Registers

The F²MC-8L family has two types of registers; dedicated hardware registers in the CPU and general-purpose memory registers. The following dedicated registers are provided:

Program counter (PC): A 16-bit-long register for indicating the instruction storage positions

Accumulator (A): A 16-bit-long temporary register for arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Temporary accumulator (T): A 16-bit-long register which is used for arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX): A 16-bit-long register for index modification

Extra pointer (EP) : A 16-bit-long pointer for indicating a memory address

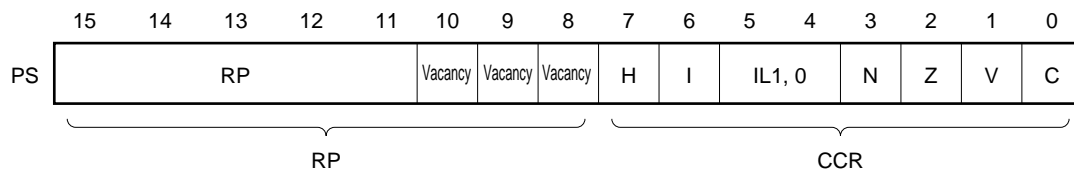
Stack pointer (SP) : A 16-bit-long pointer for indicating a stack area

Program status (PS) : A 16-bit-long register for storing a register pointer, a condition code

16 bits		Initial value	
PC	: Program counter	FFFD _H	
A	: Accumulator	indeterminate	
T	: Temporary accumulator	indeterminate	
IX	: Index register	indeterminate	
EP	: Extra pointer	indeterminate	
SP	: Stack pointer	indeterminate	
PS	: Program status	I-flag = 0, IL1, 0 = 11 The other bit values are indeterminate.	

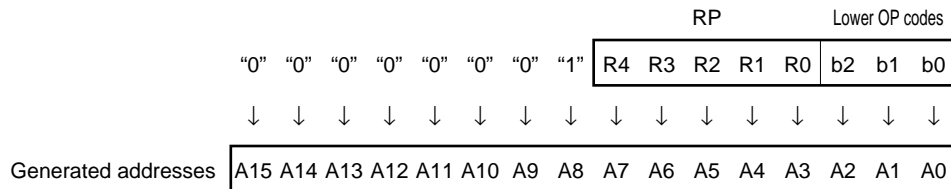
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) (see the diagram below).

• Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

• **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data, and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	0	<div>High</div> <div>↑</div> <div>↓</div> <div>Low</div>
0	1	1	
1	0	2	
1	1	3	

N-flag: Set to '1' if the highest bit becomes '1' as the result of an arithmetic operation. Cleared to '0' otherwise.

Z-flag: Set to '1' when an arithmetic operation results in '0'. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on '2' overflows as a result of an arithmetic operation. Cleared to '0' if the overflow does not occur.

C-flag: Set to '1' when a carry or borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

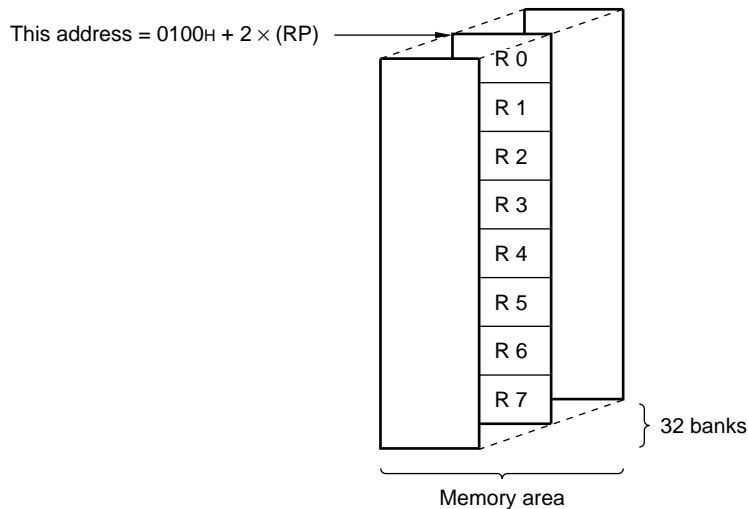
MB89890 Series

The following general-purpose registers are provided:

General-purpose registers: An 8-bit-long register for storing data

The general-purpose registers are of 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used. The bank currently in use is indicated by the register bank pointer (RP).

- Register Bank Configuration



■ I/O MAP

Address	Write/read	Register name	Register description
00 _H	(R/W)	PDR0	Port 0 data register
01 _H	(W)	DDR0	Port 0 data direction register
02 _H	(R/W)	PDR1	Port 1 data register
03 _H	(W)	DDR1	Port 1 data direction register
04 _H	(R/W)	PDR2	Port 2 data register
05 _H			Vacancy
06 _H			Vacancy
07 _H	(R/W)	SCC	System clock control register
08 _H	(R/W)	SMC	Standby control register
09 _H	(R/W)	WDTC	Watchdog control register
0A _H	(R/W)	TBTC	Time-base timer control register
0B _H	(R/W)	WPCR	Watch prescaler control register
0C _H	(R/W)	PDR3	Port 3 data register
0D _H	(R/W)	DDR3	Port 3 data direction register
0E _H	(R/W)	PDR4	Port 4 data register
0F _H	(R/W)	BZCR	Buzzer register
10 _H	(R/W)	PDR5	Port 5 data register
11 _H			Vacancy
12 _H	(R/W)	PDR6	Port 6 data register
13 _H	(R/W)	DDR6	Port 6 direction register
14 _H	(R/W)	PDR7	Port 7 data register
15 _H			Vacancy
16 _H	(R/W)	PDR8	Port 8 data register
17 _H			Vacancy
18 _H	(R/W)	PDR9	Port 9 data register
19 _H	(R/W)	DDR9	Port 9 data direction register
1A _H	(R/W)	PDRA	Port A data register
1B _H	(R/W)	DDRA	Port A data direction register
1C _H	(R/W)	SMR	Serial mode register
1D _H	(R/W)	SDR	Serial data register
1E _H	(R/W)	CNTR	PWM control register
1F _H	(W)	COMR	PWM compare register

(Continued)

MB89890 Series

Address	Write/read	Register name	Register description
20 _H	(R/W)	DTMC	DTMF control register
21 _H	(R/W)	DTMD	DTMF data register
22 _H	(R/W)	SBMR	Serial mode register with 1-byte buffer
23 _H	(R/W)	SBFR	Serial flag register with 1-byte buffer
24 _H	(W)	SBUF _W	Serial write register with 1-byte buffer
	(R)	SBUF _R	Serial read register with 1-byte buffer
25 _H	(R)	SBD _R	Serial data register with 1-byte buffer
26 _H	(R/W)	T2C _R	Timer 2 control register
27 _H	(R/W)	T1C _R	Timer 1 control register
28 _H	(R/W)	T2D _R	Timer 2 data register
29 _H	(R/W)	T1D _R	Timer 1 data register
2A _H	(R/W)	MODC	Modem output control register
2B _H	(R/W)	MODA	Modem output data register
2C _H	Vacancy		
2D _H	(R/W)	ADC1	A/D converter control register 1
2E _H	(R/W)	ADC2	A/D converter control register 2
2F _H	(R/W)	ADCD	A/D converter data register
30 _H	(R/W)	EIE1	External interrupt 1 enable register
31 _H	(R/W)	EIF1	External interrupt 1 flag register
32 _H	(R/W)	EIE2	External interrupt 2 enable register
33 _H	(R/W)	EIF2	External interrupt 2 flag register
34 _H	(R/W)	MDC1	Modem timer control 1 register
35 _H	(R/W)	MDC2	Modem timer control 2 register
36 _H	(R/W)	MLDH	Modem timer "H" level data register
37 _H	(R/W)	MLDL	Modem timer "L" level data register
38 _H	Vacancy		
39 _H	Vacancy		
3A _H	Vacancy		
3B _H	Vacancy		
3C _H	Vacancy		
3D _H	(R/W)	SSEL	Serial I/O port switching register
3E _H	Vacancy		
3F _H	Vacancy		

(Continued)

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Address	Write/read	Register name	Register description
40 _H to 7B _H			Vacancy
7C _H	(W)	ILR1	Interrupt level register 1
7D _H	(W)	ILR2	Interrupt level register 2
7E _H	(W)	ILR3	Interrupt level register 3
7F _H			Vacancy

Note: Do not use vacancies.

MB89890 Series

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	Set $V_{CC} = AV_{CC}^*$
	AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AVR must not exceed " $AV_{CC} + 0.3\text{ V}$ ".
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P40 to P44, P70 to P77, P80 to P87
		$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	P40 to P44, P70 to P77, P80 to P87
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
"L" level maximum output current	I_{OL}	—	20	mA	Peak value
"L" level average output current	I_{OLAV}	—	10	mA	Specified by the average value of 1 hour.
"L" level total maximum output current	ΣI_{OL}	—	120	mA	Peak value
"L" level total average output current	ΣI_{OLAV}	—	40	mA	Specified by the average value of 1 hour.
"H" level maximum output current	I_{OH}	—	-20	mA	Peak value
"H" level average output current	I_{OHAV}	—	-10	mA	Specified by the average value of 1 hour.
"H" level total maximum output current	ΣI_{OH}	—	-60	mA	Peak value
"H" level total average output current	ΣI_{OHAV}	—	-20	mA	Specified by the average value of 1 hour.
Power consumption	P_D	—	200	mW	
Operating temperature	T_A	-20	+85	°C	
Storage temperature	T_{stg}	-55	+150	°C	

*: Use AV_{CC} and V_{CC} set to the same voltage.

Take care so that AV_{CC} does not exceed V_{CC} , such as when power is turned on.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

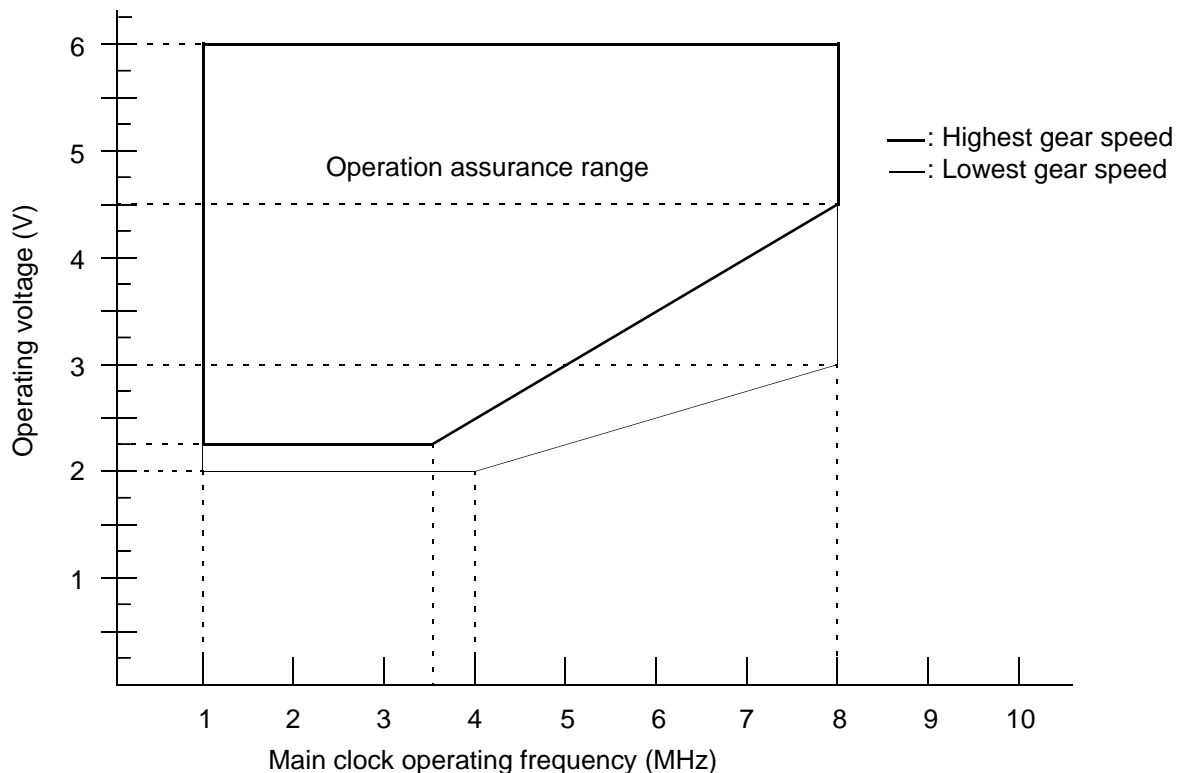
2. Recommended Operating Conditions

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	2.2*	6.0	V	See Figure 1.
	AV_{CC}	1.5	6.0	V	Retains the RAM state in the stop mode
	AVR	2.0	AV_{CC}	V	
Operating temperature	T_A	-20	+85	°C	

*: This value varies with the DTMF generator assurance range.

Figure 1 Operation Assurance Range



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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3. DC Characteristics

($AV_{CC} = V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Sym- bol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
“H” level input voltage	V_{IH}	P00 to P07, P10 to P17	—	$0.7 V_{CC}$	—	$V_{CC} + 0.3$	V	
	V_{IHS}	P30 to P37, P60 to P67, P90 to P97, PA0 to PA7, \overline{RST} , MOD0, MOD1, X0, X0A	—	$0.8 V_{CC}$	—	$V_{CC} + 0.3$	V	
“L” level input voltage	V_{IL}	P00 to P07, P10 to P17	—	$V_{SS} - 0.3$	—	$0.3 V_{CC}$	V	
	V_{ILS}	P30 to P37, P60 to P67, P90 to P97, PA0 to PA7, \overline{RST} , MOD0, MOD1, X0, X0A	—	$V_{SS} - 0.3$	—	$0.2 V_{CC}$	V	
Open-drain output pin applied voltage	V_D	P40 to P47, P70 to P77, P80 to P87	—	$V_{SS} - 0.3$	—	$V_{SS} + 7.0$	V	N-ch open-drain
		P50 to P57	—	$V_{SS} - 0.3$	—	$V_{CC} + 0.3$	V	N-ch open-drain
“H” level output voltage	V_{OH}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P60 to P67, P90 to P97, PA0 to PA7	$I_{OH} = -2.0\text{ mA}$	2.4	—	—	V	
“L” level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P60 to P67, P90 to P97, PA0 to PA7	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	V_{OL2}	\overline{RST}	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	
	V_{OL3}	P40 to P44, P70 to P77, P80 to P87	$I_{OL} = 8.0\text{ mA}$	—	—	0.6	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P44, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, MOD0, MOD1	$0.45\text{ V} < V_i < V_{CC}$	—	—	± 5	μA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P30 to P37, P40 to P44, P60 to P67, P70 to P77, P80 to P87, P90 to P97, PA0 to PA7, \overline{RST}	$V_i = 0.0\text{ V}$	25	50	100	k Ω	With pull-up resistor (Except \overline{RST})

(Continued)

MB89890 Series

($AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Sym- bol	Pin	Condition		Value			Unit	Remarks
					Min	Typ	Max		
Power supply current	I _{CC}	V _{CC}	When DTMF operation is stopped	F _{CH} = 4 MHz V _{CC} = 5.0 V in the main clock operation	—	6	9	mA	Highest gear speed
				F _{CH} = 4 MHz V _{CC} = 3.0 V in the main clock operation	—	1.2	1.8	mA	Lowest gear speed
				F _{CH} = 8 MHz V _{CC} = 5.0 V in the main clock operation	—	13	26	mA	Highest gear speed
				F _{CH} = 8 MHz V _{CC} = 3.0 V in the main clock operation	—	3	5	mA	Lowest gear speed
	I _{CCS1}			F _{CH} = 4 MHz V _{CC} = 5.0 V in the main sleep mode	—	2.5	4	mA	Highest gear speed
				F _{CH} = 8 MHz V _{CC} = 5.0 V in the main sleep mode	—	4	8	mA	Highest gear speed
	I _{CCS2}			F _{CL} = 32.768 kHz V _{CC} = 3.0 V in the subclock sleep mode	—	15	2.5	μA	
				I _{CCH1}	T _A = +25°C V _{CC} = 3.0 V in the subclock stop mode	—	—	1	μA
	I _{CCH2}				T _A = +85°C V _{CC} = 3.0 V in the subclock stop mode	—	1	10	μA
				I _{CSB}	F _{CL} = 32.768 kHz V _{CC} = 3.0 V in the sub-clock operation	—	50	75	μA
	I _{CCT}			F _{CL} = 32.768 kHz V _{CC} = 3.0 V in the watch mode	—	—	15	μA	

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($AV_{CC} = V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CCD}	V_{CC}	During DTMF operation $F_{CH} = 4 \text{ MHz}$ $V_{CC} = 5.0 \text{ V}$ in the main clock operation	—	8	12	mA	Highest gear speed
				—	2.3	3.4	mA	Lowest gear speed
				—	17	31	mA	Highest gear speed
				—	6	11	mA	Lowest gear speed
	I_A	AV_{CC}	$F_{CH} = 8 \text{ MHz}$	—	1.5	3.5	mA	When A/D conversion is operating
	I_{AH}			—	1	5	μA	When A/D conversion is not operating
Input capacitance	C_{IN}	Other than AV_{CC} , AV_{SS} , V_{CC} , and V_{SS}	—	—	10	—	pF	

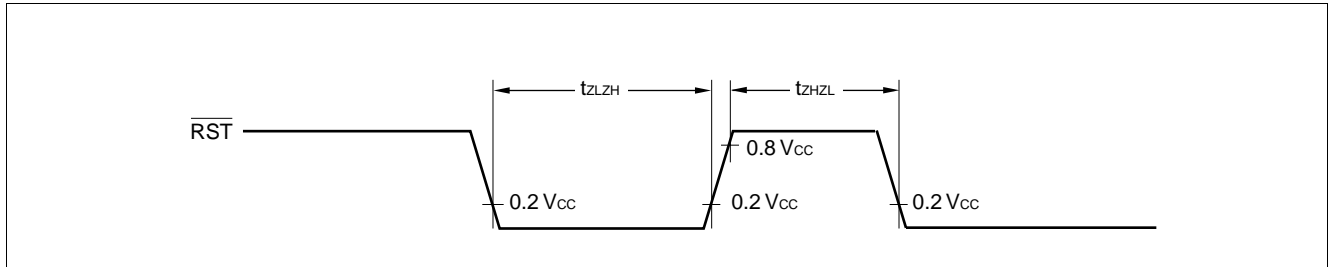
4. AC Characteristics

(1) Reset Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
$\overline{\text{RST}}$ "L" pulse width	t_{ZLZH}	—	48 t_{CYL}	—	ns	
$\overline{\text{RST}}$ "H" pulse width	t_{ZHHL}		24 t_{CYL}	—	ns	

Note: t_{CYL} is the oscillation cycle input to the X0.

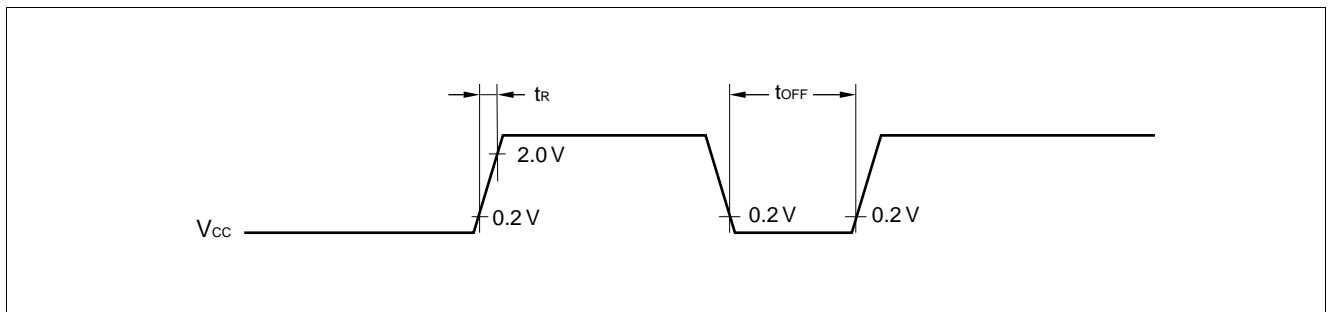


(2) Power-on Reset

($V_{SS} = 0.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_{R}	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time selected.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.



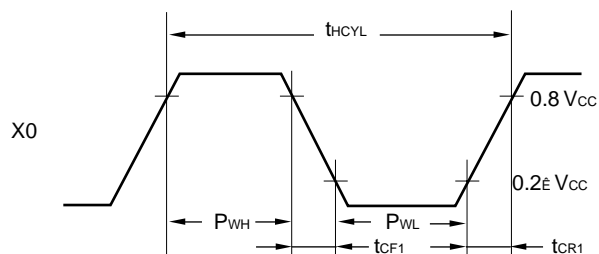
MB89890 Series

(3) Clock Timing

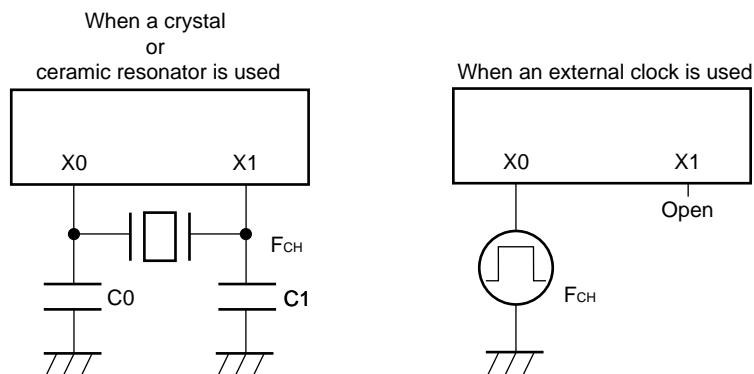
($V_{CC} = +5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F_{CH}	X0, X1	—	1	—	8	MHz	Main clock
	F_{CL}	X0A, X1A		—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1		125	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A		—	30.5	—	μs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	—	ns	External clock
	P_{WLH} P_{WLL}	X0A		—	15.2	—	μs	External clock
Input clock rising/falling time	t_{CR1} t_{CF1}	X0		—	—	24	ns	External clock
	t_{CR2} t_{CF2}	X0A		—	—	200	ns	

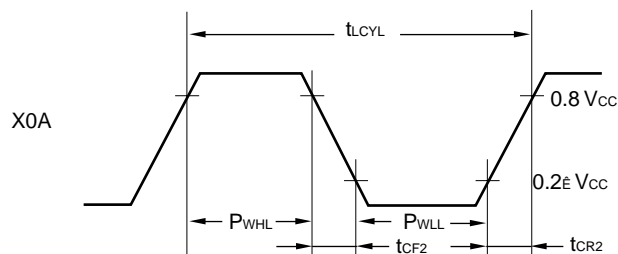
- X0 and X1 Timing and Conditions of Applied Voltage



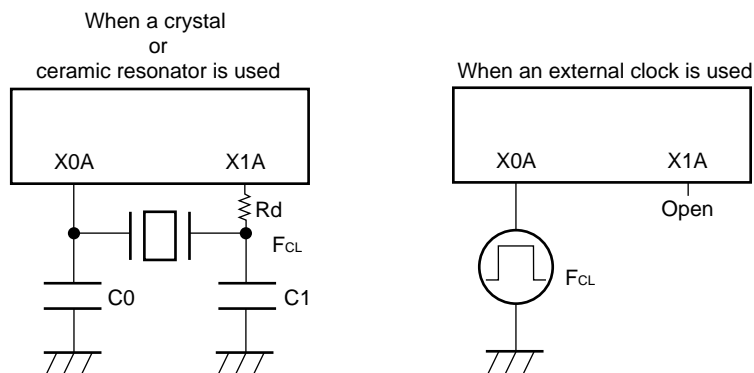
- Main Clock Conditions



- X0A and X1A Timing and Conditions of Applied Voltage



- Subclock Conditions



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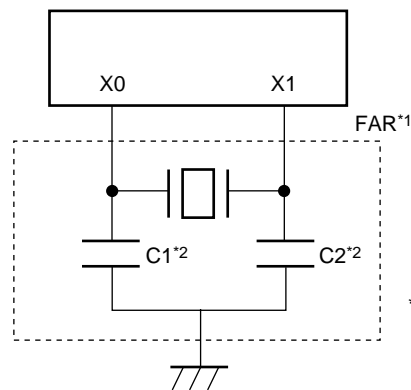
(4) Instruction Cycle

Parameter	Symbol	Value	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	μs	$(4/F_{CH}) t_{inst} = 0.5 \mu s$ when operating at $F_{CH} = 8 \text{ MHz}$
		$2/F_{CL}$	μs	$t_{inst} = 61.036 \mu s$ when operating at $F_{CL} = 32.768 \text{ kHz}$

Notes : • When operating at the main clock, t_{inst} varies with the execution time (gear) setting, within the following range: Min = $4/F_{CH}$, Max = $64/F_{CH}$.
 • When operating at the subclock, $t_{inst} = 2/F_{CL}$.

(5) Recommended Resonator Manufacturers

- Sample Application of Piezoelectric Resonator (FAR Series)

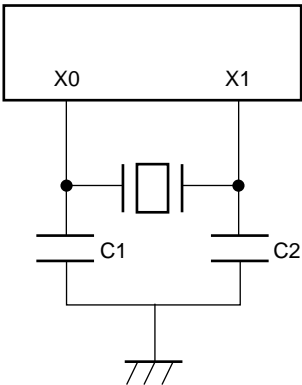


*1: Fujitsu Media Devices Acoustic Resonator

FAR part number (built-in capacitor type)	Frequency (MHz)	Initial deviation of FAR frequency ($T_A = +25^\circ\text{C}$)	Temperature characteristics of FAR frequency ($T_A = -20^\circ\text{C}$ to $+60^\circ\text{C}$)	Loading capacitors*2
FAR-C4□A-03580-□01	3.58	$\pm 0.5\%$	$\pm 0.5\%$	Built-in
FAR-C4□G-10000-□05	10.00	$\pm 0.5\%$	$\pm 0.5\%$	

Inquiry: FUJITSU MEDIA DEVICES LIMITED

- Sample Application of Ceramic Resonator



- Mask ROM products

Resonator manufacturer	Resonator	Frequency (MHz)	C1 (pF)	C2 (pF)	R
Murata Mfg. Co., Ltd.	CSA8.00MTZ	8.00	30	30	Not required
	CST8.00MTW		Built-in	Built-in	Not required

Inquiry: Murata Mfg. Co., Ltd

- Murata Electronics North America. Inc.: TEL 1-404-436-1300
- Murata Europe Management GmbH: TEL 49-911-66870
- Murata Electronics Singapore (Pte.) Ltd.: TEL 65-758-4233

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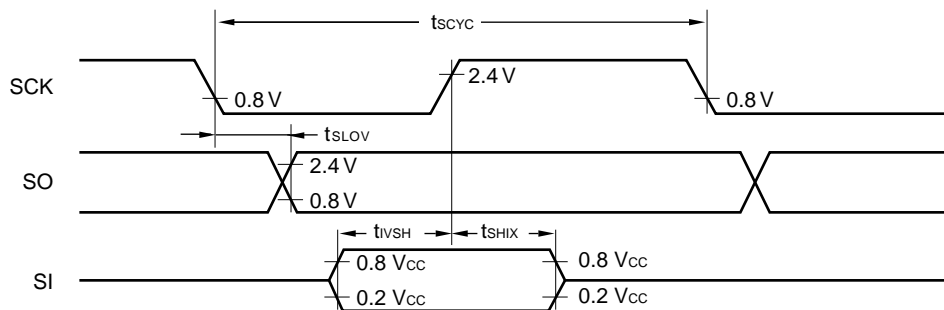
(6) Serial I/O Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

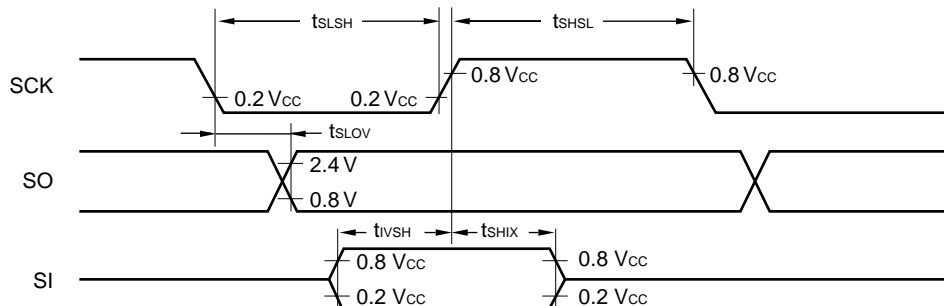
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	$2 t_{inst}^*$	—	μs	
SCK $\downarrow \rightarrow$ SO time	t_{SLOV}	SCK, SO		−200	200	ns	
Valid SI \rightarrow SCK \uparrow	t_{IVSH}	SI, SCK		200	—	ns	
SCK $\uparrow \rightarrow$ valid SI hold time	t_{SHIX}	SCK, SI		200	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	$1 t_{inst}^*$	—	μs	
Serial clock “L” pulse width	t_{SLSH}			$1 t_{inst}^*$	—	μs	
SCK $\downarrow \rightarrow$ SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI \rightarrow SCK \uparrow	t_{IVSH}	SI, SCK		200	—	ns	$2 \times t_{CYL}$
SCK $\uparrow \rightarrow$ valid SI hold time	t_{SHIX}	SCK, SI		200	—	ns	$2 \times t_{CYL}$

*: For information on t_{inst} , see “(4) Instruction Cycle.”

• Internal Shift Clock Mode



• External Shift Clock Mode

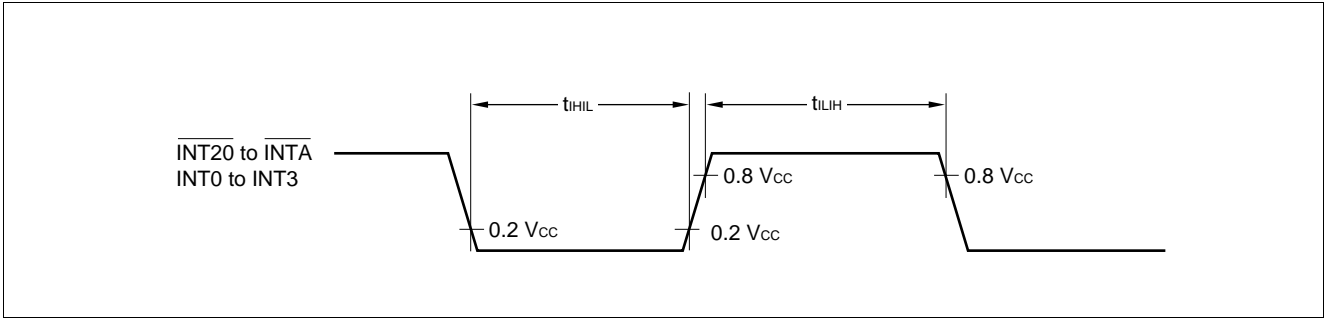


(7) Peripheral Input Timing

($V_{CC} = +5.0\text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min	Max		
Peripheral input “H” level pulse width	t_{ILIH}	$\overline{\text{INT20}}$ to $\overline{\text{INTA}}$ INT0 to INT3	$2\ t_{inst}^*$	—	μs	
Peripheral input “L” level pulse width	t_{IHIL}	$\overline{\text{INT20}}$ to $\overline{\text{INTA}}$ INT0 to INT3	$2\ t_{inst}^*$	—	μs	

*: For information on t_{inst} , see “(4) Instruction Cycle.”



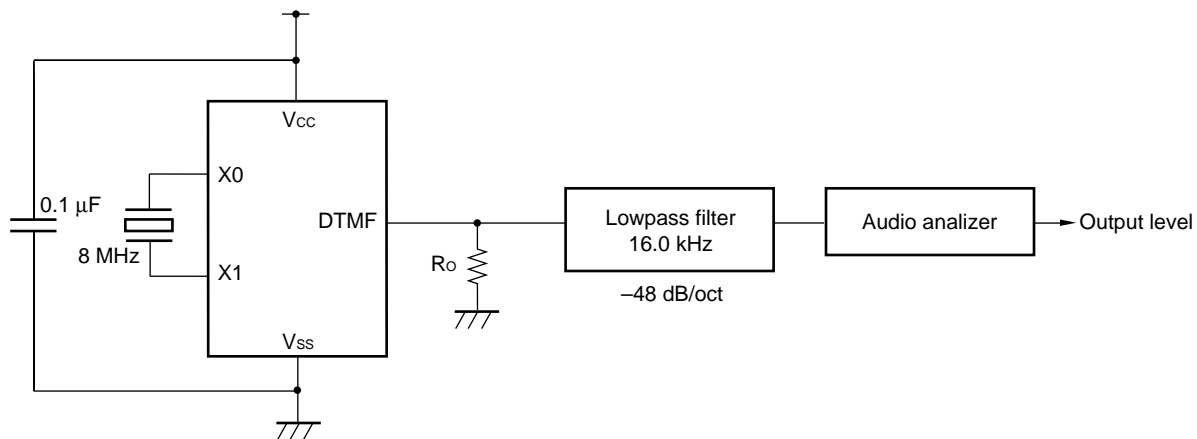
MB89890 Series

(8) Electrical Characteristics of DTMF Generator

($A_{V_{SS}} = V_{SS} = 0.0 \text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Operating voltage range	—	—	2.5	5.0	6.0	V	
Output load requirements	R_o	$V_{CC} = 2.5 \text{ V to } 6.0 \text{ V}$	20	—	—	$k\Omega$	Defined when the DTMF pin is connected to a pull-down resistor.
DTMF output offset voltage (at signal output)	V_{MOF}	$V_{CC} = 5.0 \text{ V}$	—	0.4	—	V	When the DTMF pin is open. $R_o = 200 \text{ k}\Omega$
DTMF output amplitude (ROW single tone)	V_{MFOR}	$V_{CC} = 5.0 \text{ V}$	-16.3	-14.0	-12.5	dBm	
Difference between COLUMN and ROW levels	R_{MF}	—	1.6	2.0	2.4	dB	
Distortion ratio	—	—	—	—	7	%	

• Output Level Measurement Circuit



5. A/D Converter Electrical Characteristics

($AV_{CC} = V_{CC} = +5.0 \text{ V} \pm 10\%$, $AV_{SS} = V_{SS} = 0.0 \text{ V}$, $T_A = -20^\circ\text{C}$ to $+85^\circ\text{C}$)

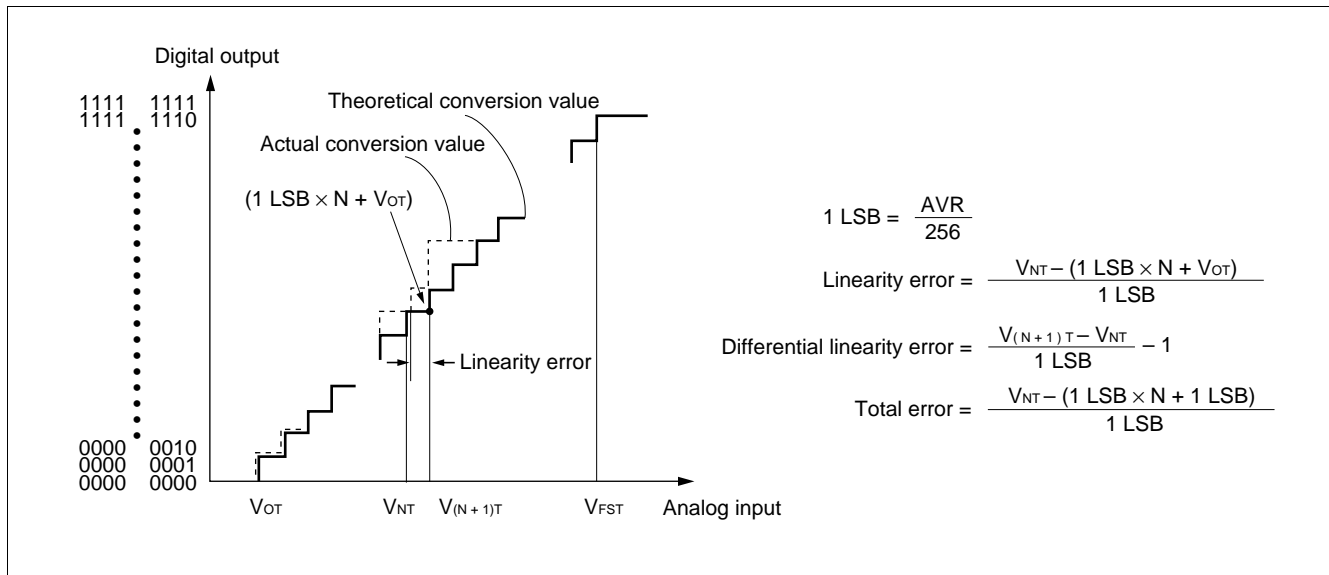
Parameter	Sym- bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Resolution	—	—	AVR = AV _{CC} = 5.0 V	—	—	8	bit	
Total error				—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V _{0T}			AV _{SS} – 1.5 LSB	AV _{SS} + 0.5 LSB	AV _{SS} + 1.5 LSB	mV	1 LSB = AVR/256
Full-scale transition voltage	V _{FST}			AVR – 1.5 LSB	AVR – 1.5 LSB	AVR + 1.5 LSB	mV	
Interchannel disparity	—		—	—	—	0.5	LSB	
A/D mode conversion time				—	44 t _{inst} *	—	μs	
Sense mode conversion time				—	12 t _{inst} *	—	μs	
Analog port input current				I _{AIN}	—	—	10	
Analog input voltage	—	AN0 to AN7	—	0.0	—	AVR	V	
Reference voltage	—			0.0	—	AV _{CC}	V	
Reference voltage supply current	I _R	AVR	AVR = AV _{CC} = 5.0 V	—	100	300	μA	When starting A/D conversion
	I _{RH}			—	—	1	μA	When starting A/D conversion

*: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Converter Glossary

- Resolution
Analog changes that are identifiable by the A/D converter
When the number of bits is 8, analog voltage can be divided into $2^8 = 256$.
- Linearity error (unit: LSB)
The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
The difference between theoretical and actual conversion values

MB89890 Series



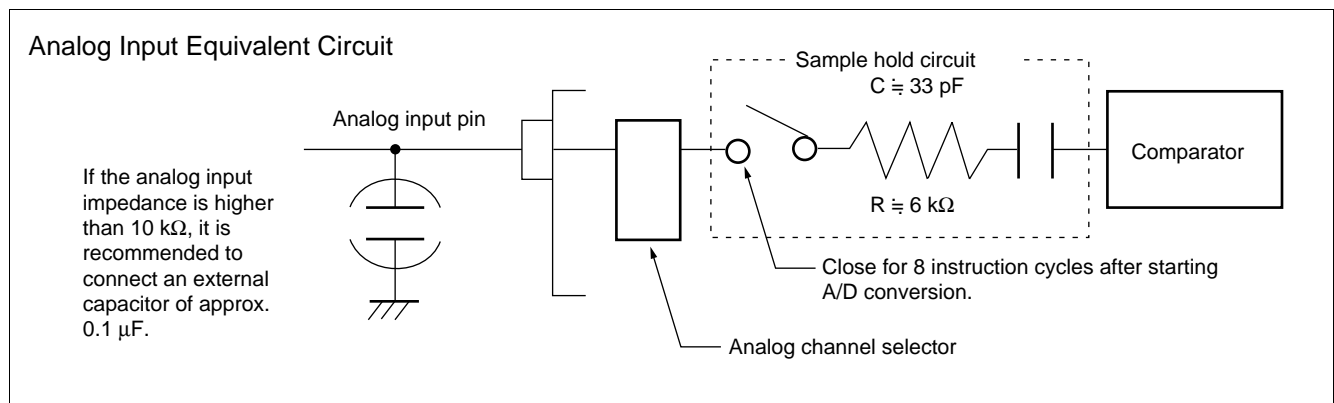
7. Notes on Using A/D Converter

- Input impedance of the analog input pins

The A/D converter used for the MB89890 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after starting A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of approx. 0.1 μF for the analog input pin.



- Error

The smaller the $|AVR - AV_{SS}|$, the greater the error would become relatively.

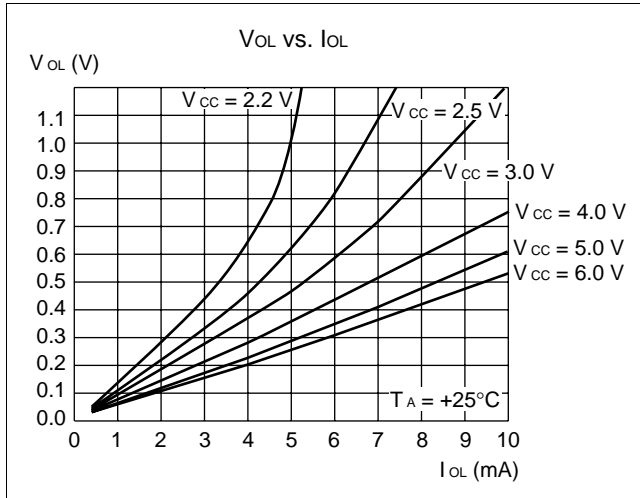
- Order of turning on A/D converter and analog input

Make sure to turn on the digital power supply (V_{CC}) before or at the same time with turning on the A/D converter power supply (AV_{CC} , AV_{SS}) and application of AN00 to AN07.

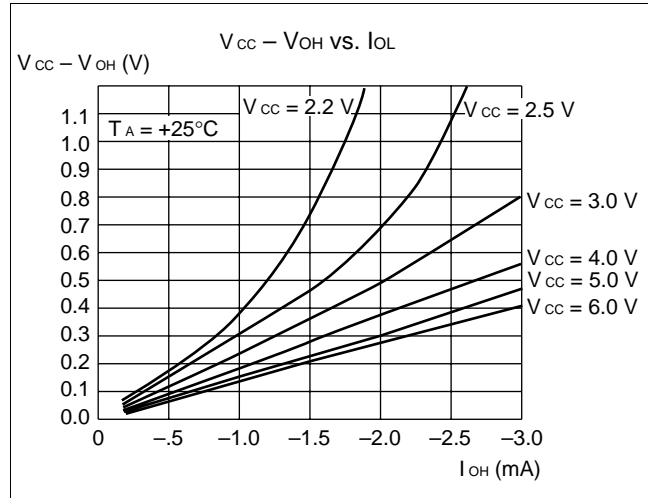
To turn off the power, turn off the A/D converter power supply (AV_{CC} , AV_{SS}) and stop the analog input (AN00 to AN07) before or at the same time with turning off the digital power supply (V_{CC}).

EXAMPLE CHARACTERISTICS

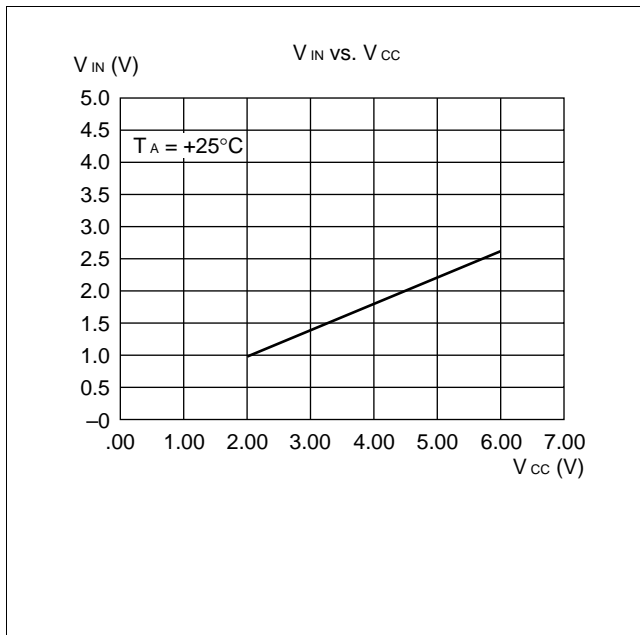
(1) "L" Level Output Voltage



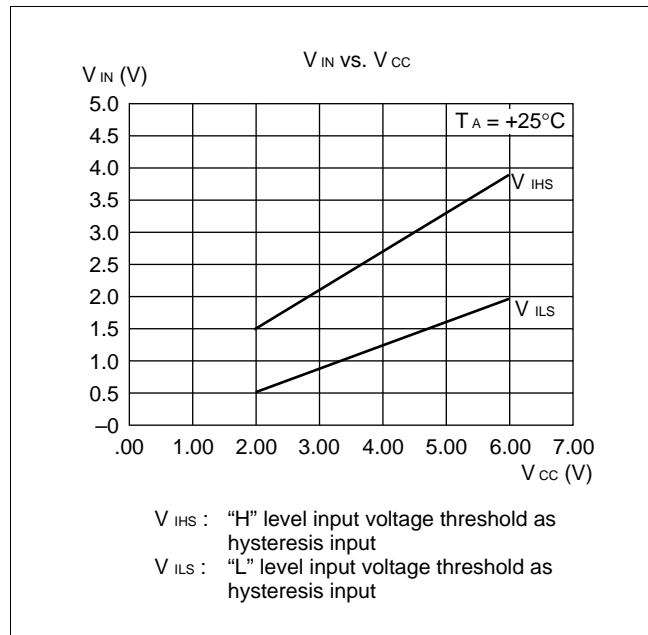
(2) "H" Level Output Voltage



(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



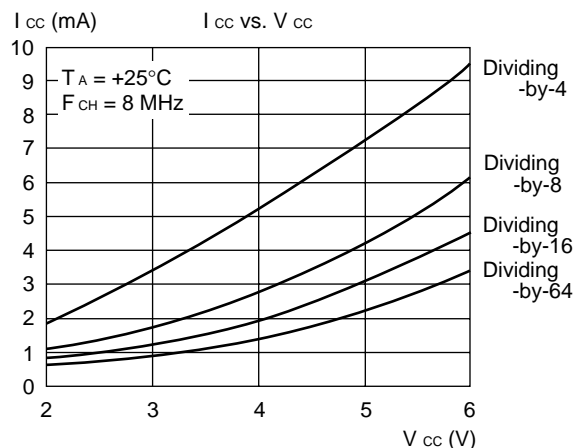
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



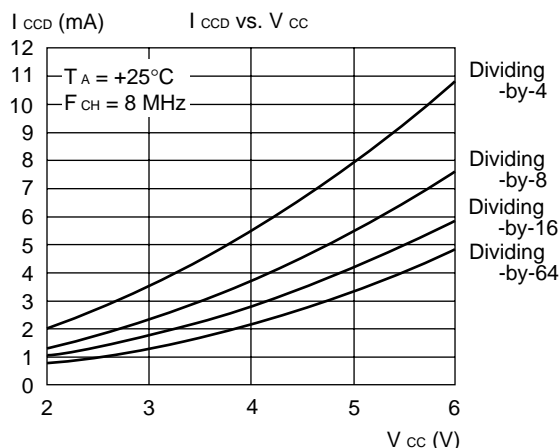
MB89890 Series

(5) Power Supply Current (External Clock)

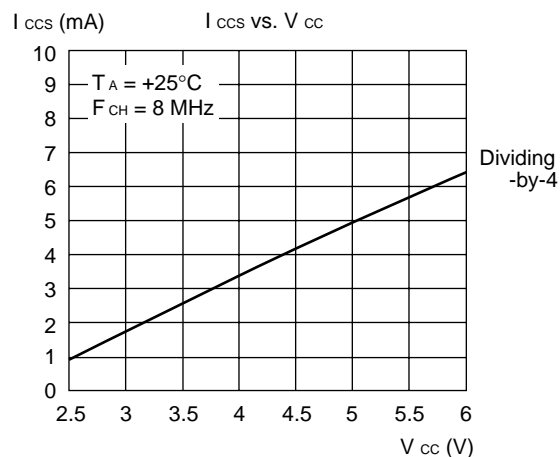
Characteristics of Current Consumption in the Main Clock Operation



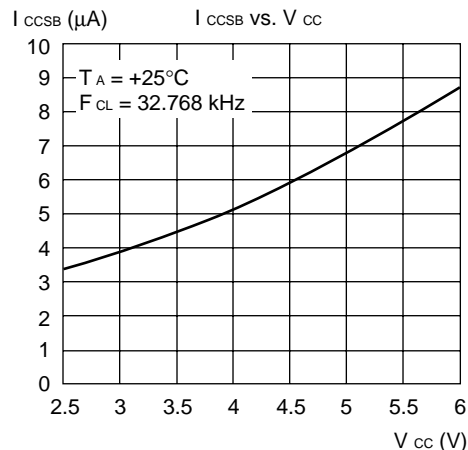
Characteristics of Current Consumption in the DTMF and Main Clock Operation



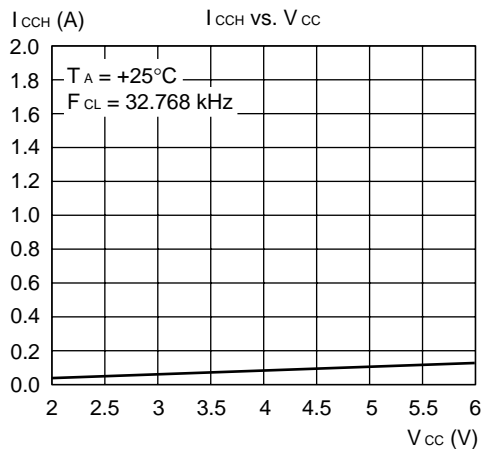
Characteristics of Current Consumption in the Main Sleep Mode



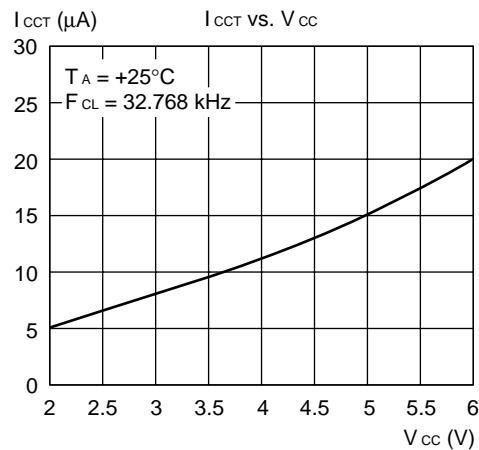
Characteristics of Current Consumption in the Subclock Operation



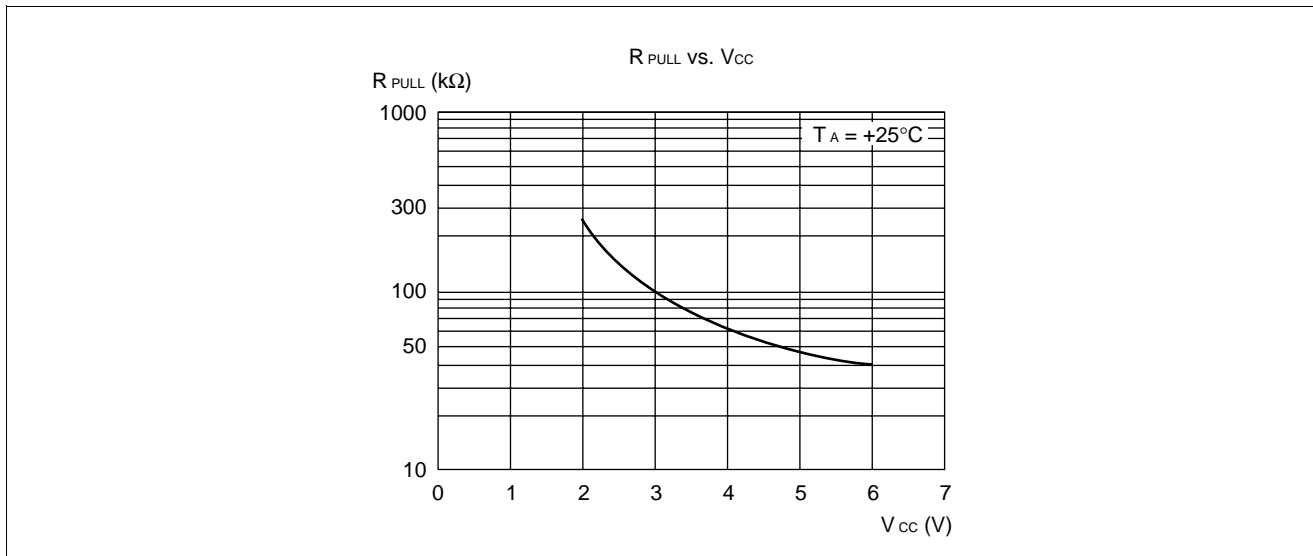
Characteristics of Current Consumption in the Subclock Stop



Characteristics of Current Consumption in the Watch Mode



(6) Pull-up Resistance



MB89890 Series

■ MASK OPTIONS

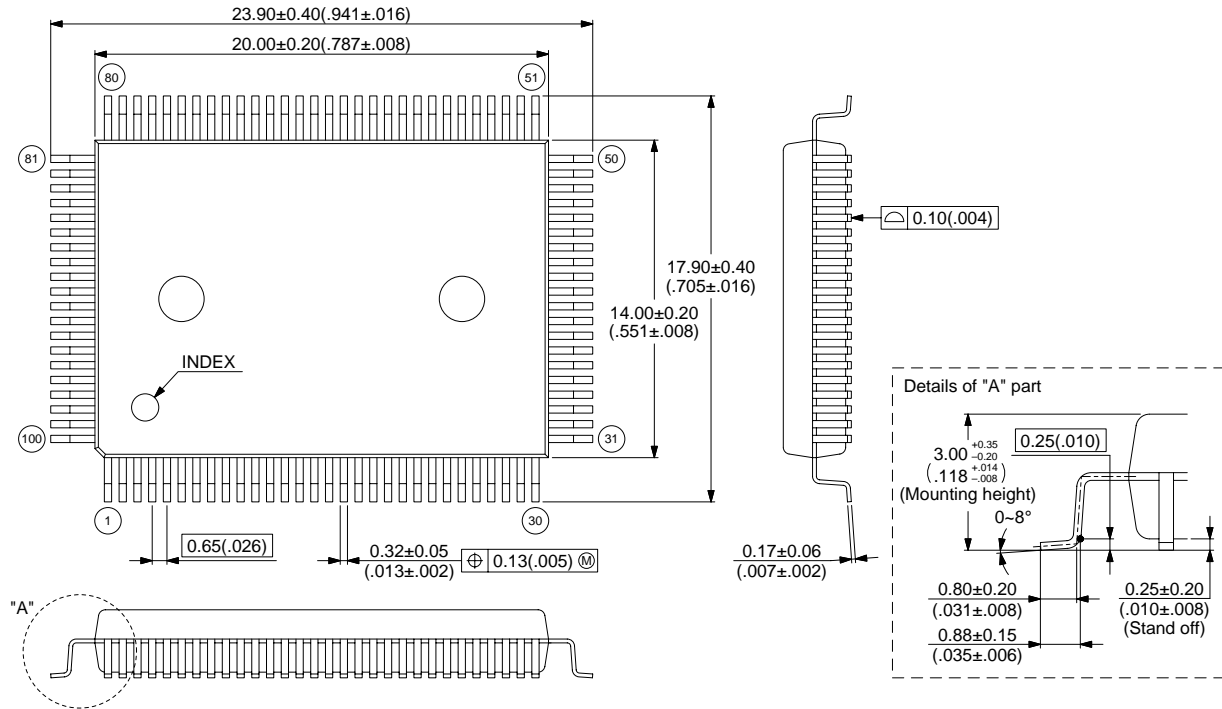
No.	Part number	MB89898/9	MB89P899	MB89PV890
	Specifying procedure	Specify when ordering masking	Specify with EPROM programmer	Specifying not possible
1	Pull-up resistors <input checked="" type="checkbox"/> P00 to P07 <input checked="" type="checkbox"/> P10 to P17 <input checked="" type="checkbox"/> P30 to P37 <input checked="" type="checkbox"/> P40 to P44 <input checked="" type="checkbox"/> P60 to P67 <input checked="" type="checkbox"/> P70 to P77 <input checked="" type="checkbox"/> P80 to P87 <input checked="" type="checkbox"/> P90 to P97 <input checked="" type="checkbox"/> PA0 to PA7	Select by single pin <input checked="" type="checkbox"/> P00 to P07 <input checked="" type="checkbox"/> P10 to P17 <input checked="" type="checkbox"/> P30 to P37 <input checked="" type="checkbox"/> P40 to P44 <input checked="" type="checkbox"/> P60 to P67 <input checked="" type="checkbox"/> P70 to P77 <input checked="" type="checkbox"/> P80 to P87 <input checked="" type="checkbox"/> P90 to P97 <input checked="" type="checkbox"/> PA0 to PA7 Set in the above combinations	Select by 2-pin pair <input checked="" type="checkbox"/> P00 to P07 <input checked="" type="checkbox"/> P10 to P17 <input checked="" type="checkbox"/> P30 to P37 <input checked="" type="checkbox"/> P60 to P67 <input checked="" type="checkbox"/> P90 to P97 <input checked="" type="checkbox"/> PA0 to PA7 Select by single pin <input checked="" type="checkbox"/> P40 to P44 <input checked="" type="checkbox"/> P70 to P77 <input checked="" type="checkbox"/> P80 to P87 Set in the above combinations	Fixed to no pull-up resistor
2	Power-on reset (POR) <input checked="" type="checkbox"/> Power-on reset provided <input checked="" type="checkbox"/> No power-on reset	Selectable	Selectable	Fixed to power-on reset optional
3	Selection of the oscillation stabilization time (OSC) The oscillation stabilization time initial value can be set with WTM1 bit and WTM0 bit.	Selectable WTM1 WTM0 0 0: $2^3/F_{CH}$ 0 1: $2^{12}/F_{CH}$ 1 0: $2^{16}/F_{CH}$ 1 1: $2^{18}/F_{CH}$	Selectable WTM1 WTM0 0 0: $2^3/F_{CH}$ 0 1: $2^{12}/F_{CH}$ 1 0: $2^{16}/F_{CH}$ 1 1: $2^{18}/F_{CH}$	Fixed to oscillator stabilization $2^{18}/F_{CH}$
4	Reset pin output (RST) <input checked="" type="checkbox"/> Reset output provided <input checked="" type="checkbox"/> No reset output	Selectable	Selectable	Fixed to reset output optional
5	Selection of clock mode (CLK) <input checked="" type="checkbox"/> Double clock mode <input checked="" type="checkbox"/> Single clock mode	Selectable	Selectable	Fixed to double clock mode

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89898PF MB89899PF MB89P899PF	100-pin Plastic QFP (FPT-100P-M06)	
MB89PV890CF	100-pin Ceramic MQFP (MQP-100C-P01)	

■ PACKAGE DIMENSIONS

100-pin Plastic QFP
(FPT-100P-M06)



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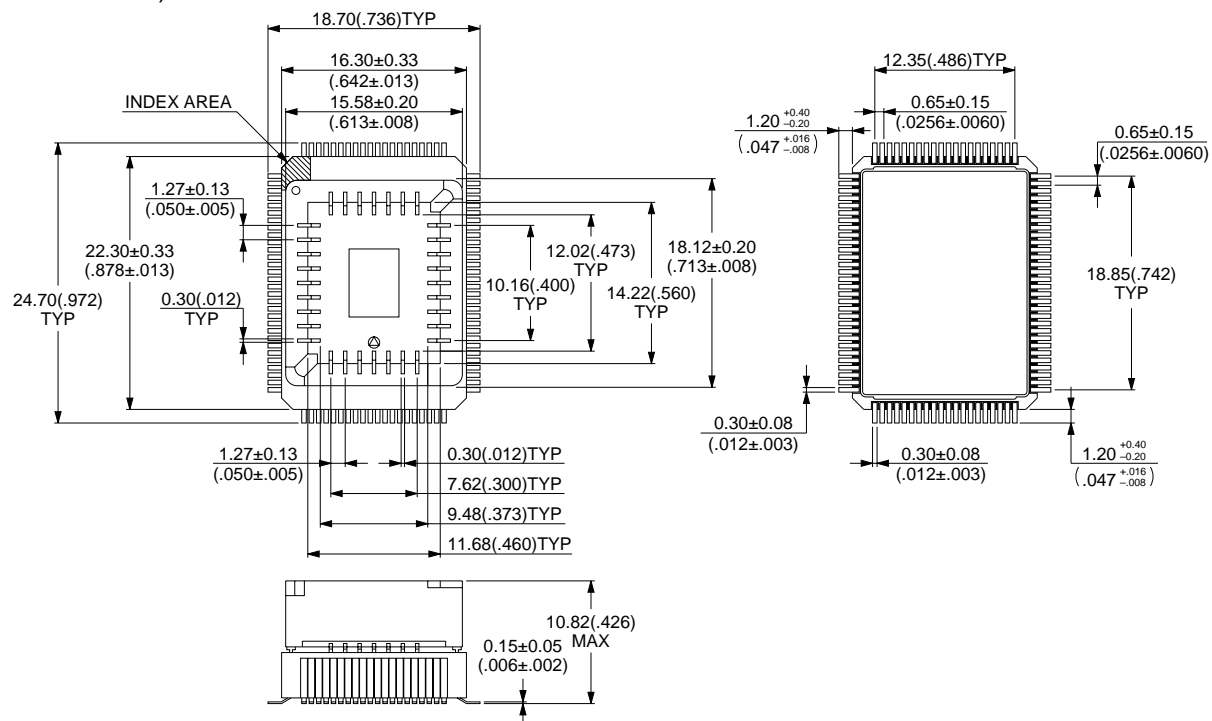
Dimensions in mm (inches)

(Continued)

MB89890 Series

(Continued)

100-pin Ceramic MQFP
(MQP-100C-P01)



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Dimensions in mm (inches)

MB89890 Series

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