

32-bit RISC Microcontroller

CMOS

FR30 Series

MB91107/108

■ DESCRIPTION

The MB91107 is a standard single-chip microcontroller constructed around the 32-bit RISC CPU (FR* family) core with abundant I/O resources and bus control functions optimized for high-performance/high-speed CPU processing for embedded controller applications. To support the vast memory space accessed by the 32-bit CPU, the MB91107 normally operates in the external bus access mode and executes instructions on the internal 1 Kbyte cache memory and RAM (MB91107: 128 Kbytes, MB91108: 160 Kbytes) for enhanced performance.

The MB91107 is optimized for applications requiring high-performance CPU processing such as navigation systems, high-performance FAXs and printer controllers.

*: FR Family stands for FUJITSU RISC controller.

■ FEATURES

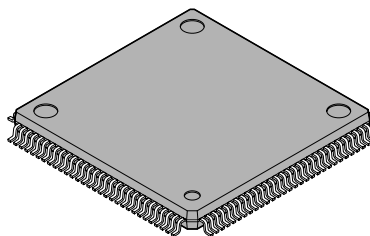
FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- Operating clock frequency: Internal 50 MHz/external 25 MHz (PLL used at source oscillation 12.5 MHz)
- General purpose registers: 32 bits × 16
- 16-bit fixed length instructions (basic instructions), 1 instruction/1 cycle
- Memory to memory transfer, bit processing, barrel shifter processing: Optimized for embedded applications

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■ PACKAGE

120-pin Plastic LQFP



(FPT-120P-M21)

- Function entrance/exit instructions, multiple load/store instructions of register contents, instruction systems supporting high level languages
- Register interlock functions, efficient assembly language coding
- Branch instructions with delay slots: Reduced overhead time in branch executions
- Internal multiplier/supported at instruction level
 - Signed 32-bit multiplication: 5 cycles
 - Signed 16-bit multiplication: 3 cycles
- Interrupt (push PC and PS): 6 cycles, 16 priority levels

Bus interface

- Clock doubler: Internal 50 MHz, external bus 25 MHz operation
- 25-bit address bus (32 Mbytes memory space)
- 8/16-bit data bus
- Basic external bus cycle: 2 clock cycles
- Chip select outputs for setting down to a minimum memory block size of 64 Kbytes: 8
- Interface supported for various memory technologies
 - DRAM interface (area 4 and 5)
- Automatic wait cycle insertion: Flexible setting, from 0 to 7 for each area
- Unused data/address pins can be configured as input/output ports
- Little endian mode supported (Select 1 area from area 1 to 5)

DRAM interface

- 2 banks independent control (area 4 and 5)
- Double CAS DRAM (normal DRAM I/F) / Single CAS DRAM / Hyper DRAM
- Basic bus cycle: Normally 5 cycles, 2-cycle access possible in high-speed page mode
- Programmable waveform: Automatic 1-cycle wait insertion to RAS and CAS cycles
- DRAM refresh
 - CBR refresh (interval time configurable by 6-bit timer)
 - Self-refresh mode
- Supports 8/9/10/12-bit column address width
- 2CAS/1WE, 2WE/1CAS selective

Cache memory

- 1-Kbyte instruction cache memory
- 2 way set associative
- 32 block/way, 4 entry(4 word)/block
- Lock function: For specific program code to be resident in cache memory

DMAC (DMA controller)

- 8 channels
- Transfer incident/external pins/internal resource interrupt requests
- Transfer sequence: Step transfer/block transfer/burst transfer/continuous transfer
- Transfer data length: 8 bits/16 bits/32 bits selective
- NMI/interrupt request enables temporary stop operation

UART

- 3 independent channels
- Full-duplex double buffer
- Data length: 7 bits to 9 bits (non-parity), 6 bits to 8 bits (parity)
- Asynchronous (start-stop system), CLK-synchronized communication selective
- Multi-processor mode
- Internal 16-bit timer (U-TIMER) operating as a proprietary baud rate generator: Generates any given baud rate
- Use external clock can be used as a transfer clock
- Error detection: Parity, frame, overrun

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10-bit A/D converter (successive approximation conversion type)

- 10-bit resolution, 4 channels
- Successive approximation type: Conversion time of 5.6 μ s at 25 MHz
- Internal sample and hold circuit
- Conversion mode: Single conversion/scanning conversion/repeated conversion selective
- Start: Software/external trigger/internal timer selective

16-bit reload timer

- 16-bit timer: 3 channels
- Internal clock: 2 clock cycle resolution, divide by 2/8/32 selective

Other interval timers

- 16-bit timer: 3 channels (U-TIMER)
- PWM timer: 4 channels
- Watchdog timer: 1 channel

Bit search module

First bit transition “1” or “0” from MSB can be detected in 1 cycle

Interrupt controller

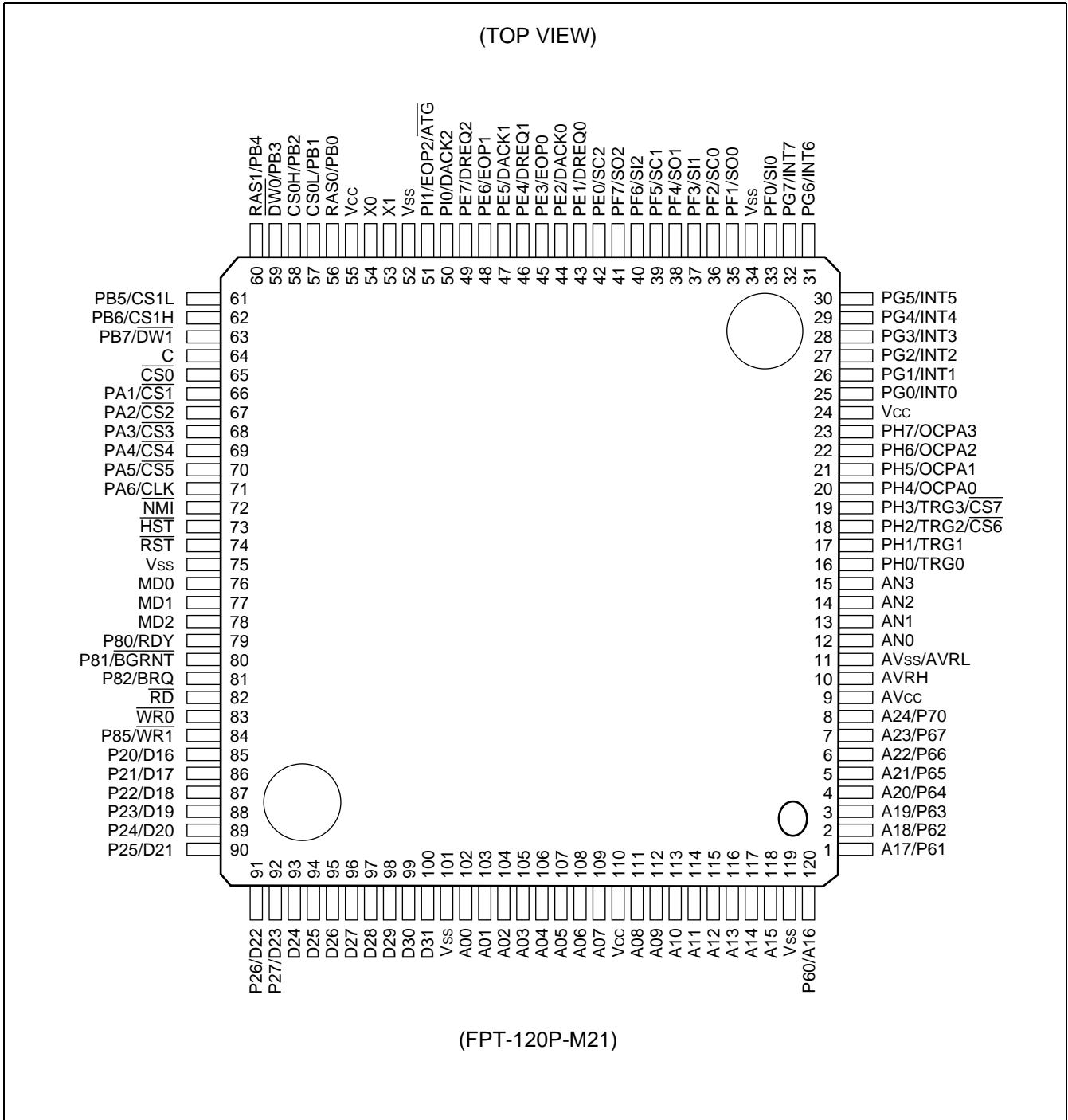
- External interrupt input: Non-maskable interrupt ($\overline{\text{NMI}}$), normal interrupt 8 (INT0 to INT7)
- Internal interrupt incident: UART, DMA controller (DMAC), A/D converter, U-TIMER and delayed interrupt module
- Priority levels of interrupts are programmable except for non-maskable interrupt (in 16 levels)

Others

- Reset cause: Power-on reset/hardware standby/watchdog timer/software reset/external reset
- Low-power consumption mode: Sleep mode/stop mode
- Clock control
 - Gear function: Operating clocks for CPU and peripherals are independently selective
 - Gear clock can be selected from 1/1, 1/2, 1/4 and 1/8 (or 1/2, 1/4, 1/8 and 1/16)
 - However, operating frequency for peripherals is less than 25 MHz.
- Packages: LQFP-120
- CMOS technology (0.35 μ m): MB91V108 (0.25 μ m) Development model
 - MB91107 (0.25 μ m) Production model
 - MB91108 (0.25 μ m) Production model
- Power supply voltage: 3.3 V \pm 0.3 V (internal regulator)

MB91107/108

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
85 86 87 88 89 90 91 92	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	C	Bit 16 to bit 23 of external data bus. Can be configured as ports (P20 to P27) when external data bus width is set to 8-bit.
93 94 95 96 97 98 99 100	D24 D25 D26 D27 D28 D29 D30 D31	C	Bit 24 to bit 31 of external data bus.
102 103 104 105 106 107 108 109 111 112 113 114 115 116 117 118	A00 A01 A02 A03 A04 A05 A06 A07 A08 A09 A10 A11 A12 A13 A14 A15	F	Bit 00 to bit 15 of external address bus.
120 1 2 3 4 5 6 7	A16/P60 A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66 A23/P67	F	Bit 16 to bit 23 of external address bus. Can be configured as ports(P60 to P67) when not used as address bus.
8	A24/P70	F	Bit 24 of external address bus. Can be configured as a port(P70) when not used as address bus.
79	RDY/P80	C	External ready input. Inputs "0" when bus cycle is being executed and not completed. Can be configured as a port when this pin is not used.

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Pin no.	Pin name	Circuit type	Function									
80	$\overline{\text{BGRNT}}/\text{P81}$	F	External bus release acknowledge output. Outputs "L" level when external bus is released. Can be configured as a port when this pin is not used.									
81	BRQ/P82	P	External bus release request input. Inputs "1" when release of external bus is required. Can be configured as a port when this pin is not used.									
82	$\overline{\text{RD}}$	M	Read strobe output pin for external bus.									
83	$\overline{\text{WR0}}$	M	Write strobe output pin for external bus. Relation between control signals and effective byte locations is as follows:									
84	$\overline{\text{WR1}}/\text{P85}$	F										
			<table border="1"> <thead> <tr> <th></th> <th>16-bit bus width</th> <th>8-bit bus width</th> </tr> </thead> <tbody> <tr> <td>D31 to D24</td> <td>$\overline{\text{WR0}}$</td> <td>$\overline{\text{WR0}}$</td> </tr> <tr> <td>D23 to D16</td> <td>$\overline{\text{WR1}}$</td> <td>(I/O port enabled)</td> </tr> </tbody> </table>		16-bit bus width	8-bit bus width	D31 to D24	$\overline{\text{WR0}}$	$\overline{\text{WR0}}$	D23 to D16	$\overline{\text{WR1}}$	(I/O port enabled)
	16-bit bus width	8-bit bus width										
D31 to D24	$\overline{\text{WR0}}$	$\overline{\text{WR0}}$										
D23 to D16	$\overline{\text{WR1}}$	(I/O port enabled)										
			Note: $\overline{\text{WR1}}$ is Hi-Z during resetting. Attach an external pull-up resistor when using at 16-bit bus width.									
65	$\overline{\text{CS0}}$	M	Chip select 0 output ("L" active).									
66	$\overline{\text{CS1}}/\text{PA1}$	F	Chip select 1 output ("L" active).									
67	$\overline{\text{CS2}}/\text{PA2}$		Chip select 2 output ("L" active).									
68	$\overline{\text{CS3}}/\text{PA3}$		Chip select 3 output ("L" active).									
69	$\overline{\text{CS4}}/\text{PA4}$		Chip select 4 output ("L" active).									
70	$\overline{\text{CS5}}/\text{PA5}$		Chip select 5 output ("L" active).									
			Can be configured as ports when PA1 to PA5 are not used.									
71	CLK/PA6	F	System clock output. Outputs clock signal of external bus operating frequency. Can be configured as a port when PA6 is not used.									
56	RAS0/PB0	F	RAS output for DRAM bank 0.									
57	CS0L/PB1		CASL output for DRAM bank 0.									
58	CS0H/PB2		CASH output for DRAM bank 0.									
59	$\overline{\text{DW0}}/\text{PB3}$		$\overline{\text{WE}}$ output for DRAM bank 0 ("L" active).									
60	RAS1/PB4		RAS output for DRAM bank 1.									
61	CS1L/PB5		CASL output for DRAM bank 1.									
62	CS1H/PB6		CASH output for DRAM bank 1.									
63	$\overline{\text{DW1}}/\text{PB7}$		$\overline{\text{WE}}$ output for DRAM bank 1 ("L" active)									
			Refer to the DRAM interface for details.									
			Can be configured as a port when PB0 to PB7 are not used.									
76	MD0	G	Mode pins 0 to 2.									
77	MD1		MCU basic operation mode is set by these pins.									
78	MD2		Directly connect these pins with V_{CC} or V_{SS} for use.									
53	X1	A	Clock (oscillator) output.									
54	X0		Clock (oscillator) input.									
74	$\overline{\text{RST}}$	B	External reset input.									
73	$\overline{\text{HST}}$	H	Hardware standby input ("L" active).									

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Pin no.	Pin name	Circuit type	Function
72	$\overline{\text{NMI}}$	H	NMI (non-maskable interrupt pin) input ("L" active).
42	SC2/PE0	F	(SC2) Clock I/O pin for UART2. Clock output is available when clock output of UART2 is enabled.
			(PE0) General purpose I/O port. This function is available when UART2 clock output is disabled.
43	DREQ0/PE1	F	(DREQ0) External transfer request input pins for DMA. This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
			(PE1) General purpose I/O port.
44	DACK0/PE2	F	(DACK0) External transfer request acknowledge output pin for DMAC (ch. 0). This function is available when transfer request output for DMAC is enabled.
			(PE2) General purpose I/O port. This function is available when transfer request acknowledge output for DMAC or DACK0 output is disabled.
45	EOP0/PE3	F	(EOP0) Can be configured as DMAC EOP OUTPUT (ch.0) when DMAC EOP output is enable.
			(PE3) General purpose I/O port.
46	DREQ1/PE4	F	(DREQ1) External transfer request input pins for DMA. This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
			(PE4) General purpose I/O port.
47	DACK1/PE5	F	(DACK1) External transfer request acknowledge output pin for DMAC (ch. 1). This function is available when transfer request output for DMAC is enabled.
			(PE5) General purpose I/O port. This function is available when transfer request acknowledge output for DMAC or DACK1 output is disabled.
48	EOP1/PE6	F	(EOP1) Can be configured as DMAC EOP OUTPUT (ch.1) when DMAC EOP output is enable.
			(PE6) General purpose I/O port.
49	DREQ2/PE7	F	(DREQ2) External transfer request input pins for DMA. This pin is used for input when external trigger is selected to cause DMAC operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
			(PE7) General purpose I/O port.

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Pin no.	Pin name	Circuit type	Function
33	SI0/PF0	F	(SI0) UART0 data input pin. This pin is used for input during UART0 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
			(PF0) General purpose I/O port.
35	SO0/PF1	F	(SO0) UART0 data output pin. This function is available when UART0 data output is enabled.
			(PF1) General purpose I/O port. This function is available when UART0 data output is disabled.
36	SC0/PF2	F	(SC0) UART0 clock I/O pin. Clock output is available when UART0 clock output is enabled.
			(PF2) General purpose I/O port. This function is available when UART0 clock output is disabled.
37	SI1/PF3	F	(SI1) UART1 data input pin. This pin is used for input during UART1 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
			(PF3) General purpose I/O port.
38	SO1/PF4	F	(SO1) UART1 data output pin. This function is available when UART1 data output is enabled.
			(PF4) General purpose I/O port. This function is available when UART1 data output is disabled.
39	SC1/PF5	F	(SC1) Clock I/O pin for UART1. Clock output is available when clock output of UART1 is enabled.
			(PF5) General purpose I/O port. This function is available when UART1 clock output is disabled.
40	SI2/PF6	F	(SI2) UART2 data input pin. This pin is used for input during UART2 is in input operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
			(PF6) General purpose I/O port.
41	SO2/PF7	F	(SO2) UART2 data output pin. This function is available when UART2 data output is enabled.
			(PF7) General purpose I/O port. This function is available when UART2 data output is disabled.

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Pin no.	Pin name	Circuit type	Function
25 26 27 28 29 30 31 32	INT0/PG0 INT1/PG1 INT2/PG2 INT3/PG3 INT4/PG4 INT5/PG5 INT6/PG6 INT7/PG7	I	(INT0 to INT7) External interrupt request input pin. This pin is used for input during corresponding interrupt is enabled, and it is necessary to disable output for other functions from this pin unless such output is made intentionally. (PG0 and PG7) General purpose I/O port.
16 17	TRG0/PH0 TRG1/PH1	F	(TRG0 and TRG1) PWM timer external trigger input pin. This function is available when PH0 and PH1 data outputs are disabled. (PH0 and PH1) General purpose I/O port.
18 19	TRG2/PH2/ $\overline{CS6}$ TRG3/PH3/ $\overline{CS7}$	F	(TRG2 and TRG3) PWM timer external trigger input pin. This function is available when PH2 and PH3 data outputs are disabled. (PH2 and PH3) Can be configured as a I/O port when TRG2, TRG3, $\overline{CS6}$ and $\overline{CS7}$ are not used. Chip select 6 output ("L" active). Chip select 7 output ("L" active).
20 21 22 23	OCPA0/PH4 OCPA1/PH5 OCPA2/PH6 OCPA3/PH7	F	(OCPA0 to OCPA3) PWM timer output pin. This function is available when PWM timer output is enabled. (PH4 to PH7) General purpose I/O port.
50	DACK2/PI0	F	(DACK2) External transfer request acknowledge output pin for DMAC (ch. 2). This function is available when transfer request output for DMAC is enabled. (PI0) General purpose I/O port. This function is available when transfer request acknowledge output for DMAC or DACK2 output is disabled.
51	EOP2/PI1/ \overline{ATG}	F	(EOP2) EOP output pin for DMAC (ch.1). This function is available when EOP output for DMAC is enabled. (PI1) General purpose I/O port. This function is available when transfer complete acknowledge output for DMAC output is disabled. (\overline{ATG}) External trigger input pin for A/D converter. This pin is used for input when external trigger is selected to cause A/D converter operation, and it is necessary to disable output for other functions from this pin unless such output is made intentionally.
12 to 15	AN0 to AN3	N	(AN0 to AN3) Analog input pins of A/D converter. This function is available when AIC register is set to specify analog input mode.
9	AV _{CC}	—	Power supply pin (V _{CC}) for A/D converter.
10	AVRH	—	Reference voltage input (high) for A/D converter. Make sure to turn on and off this pin with potential of AVRH or more applied to V _{CC} .

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Pin no.	Pin name	Circuit type	Function
11	AV _{ss} / AVRL	—	Power supply pin (V _{ss}) for A/D converter and reference voltage input pin (low).
24, 55, 110	V _{cc}	—	Power supply pin (V _{cc}) for digital circuit. Always three pins must be connected to the power supply
64	C	—	Bypass capacitor pin for internal capacitor. Refer to the HANDLING DEVICES.
34, 52, 75, 101, 119	V _{ss}	—	Earth level (V _{ss}) for digital circuit.

Note : In most of the above pins, I/O port and resource I/O are multiplexed e.g. xxx/Pxxx. In case of conflict between output of I/O port and resource I/O, priority is always given to the output of resource I/O.

■ DRAM CONTROL REGISTER

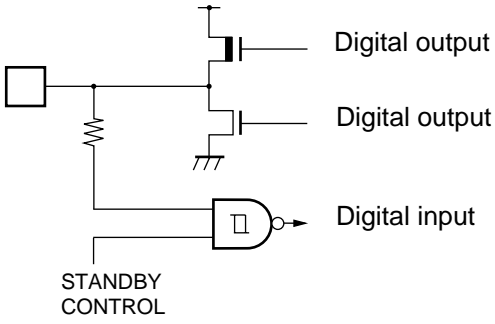
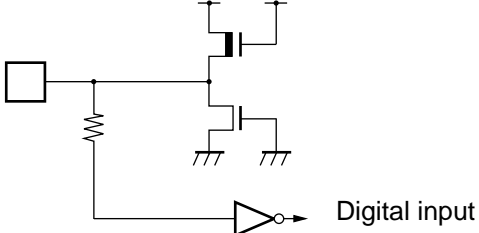
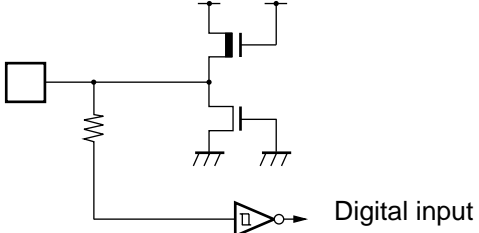
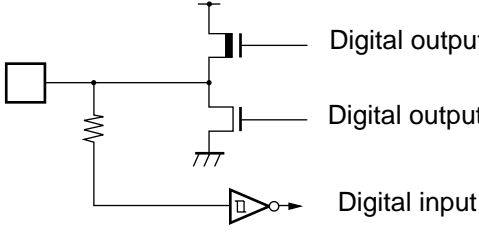
Pin name	Data bus 16-bit mode		Data bus 8-bit mode	Remarks
	2CAS/1WR mode	1CAS/2WR mode		
RAS0	Area 4 RAS	Area 4 RAS	Area 4 RAS	Correspondence of "L" "H" to lower address 1 bit (A0) in data bus 16-bit mode. "L": "0" "H": "1"
RAS1	Area 5 RAS	Area 5 RAS	Area 5 RAS	
CS0L	Area 4 CASL	Area 4 CAS	Area 4 CAS	CASL : CAS which A0 corresponds to "0" area CASH : CAS which A0 corresponds to "1" area
CS0H	Area 4 CASH	Area 4 \overline{WEL}	Area 4 CAS	
CS1L	Area 5 CASL	Area 5 CAS	Area 5 CAS	\overline{WEL} : \overline{WE} which A0 corresponds to "0" area \overline{WEH} : \overline{WE} which A0 corresponds to "1"
CS1H	Area 5 CASH	Area 5 \overline{WEL}	Area 5 CAS	
DW0	Area 4 WE	Area 4 WEL	Area 4 WE	
DW1	Area 5 WE	Area 5 WEL	Area 5 WE	

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		<ul style="list-style-type: none"> • Oscillation feedback resistance: 1 MΩ approx.
B		<ul style="list-style-type: none"> • CMOS level Hysteresis input Without standby control • With pull-up resistance
C		<ul style="list-style-type: none"> • CMOS level I/O With standby control
N		<ul style="list-style-type: none"> • Analog input

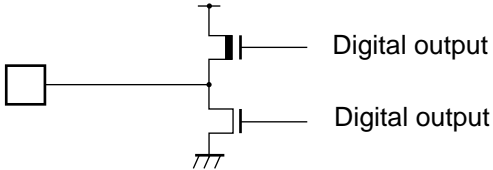
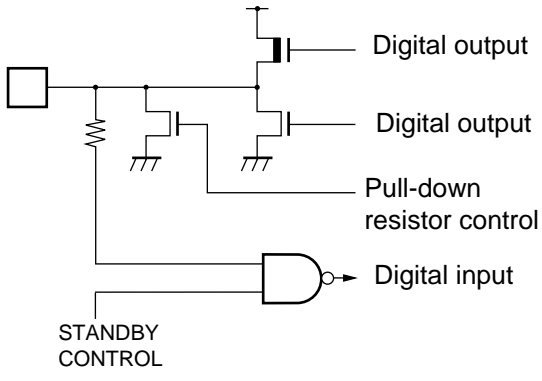
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Type	Circuit	Remarks
F		<ul style="list-style-type: none"> • CMOS level output • CMOS level Hysteresis input With standby control
G		<ul style="list-style-type: none"> • CMOS level input Without standby control
H		<ul style="list-style-type: none"> • CMOS level Hysteresis input Without standby control
I		<ul style="list-style-type: none"> • CMOS level output • CMOS level Hysteresis input Without standby control

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Type	Circuit	Remarks
M		<ul style="list-style-type: none"> • CMOS level output
P		<ul style="list-style-type: none"> • CMOS level output • CMOS level input With standby control • With pull-down resistance

■ HANDLING DEVICES

1. Preventing Latchup

In CMOS ICs, applying voltage higher than V_{CC} or lower than V_{SS} to input/output pin or applying voltage over rating across V_{CC} and V_{SS} may cause latchup.

This phenomenon rapidly increases the power supply current, which may result in thermal breakdown of the device. Make sure to prevent the voltage from exceeding the maximum rating.

2. Treatment of Pins

•Treatment of unused pins

Unused pins left open may cause malfunctions. Make sure to connect them to pull-up or pull-down resistors.

•Handling the output pins

Connecting an output pin to the power supply, to another output pin, or to a large-capacitance load may cause a large current to flow. Since letting it flow for an extended period of time degrades the device, be careful in using the device not to exceed the maximum rating.

•Power supply pins

When there are several V_{CC} and V_{SS} pins, each of them is equipotentially connected to its counterpart inside of the device, minimizing the risk of malfunctions such as latch up. To further reduce the risk of malfunctions, to prevent EMI radiation, to prevent strobe signal malfunction resulting from creeping-up of ground level and to observe the total output current standard, connect all V_{CC} and V_{SS} pins to the power supply or GND.

It is preferred to connect V_{CC} and V_{SS} of MB91107 to power supply with minimal impedance possible.

It is also recommended to connect a ceramic capacitor as a bypass capacitor of about 0.1 μF between V_{CC} and V_{SS} at a position as close as possible to MB91107.

•Mode setting pins (MD0 to MD2)

Connect mode setting pins (MD0 to MD2) directly to V_{CC} or V_{SS} .

Arrange each mode setting pin and V_{CC} or V_{SS} patterns on the printed circuit board as close as possible and make the impedance between them minimal to prevent mistaken entrance to the test mode caused by noises.

•Crystal oscillator circuit

Noises around X0 and X1 pins may cause malfunctions of MB91101. In designing the PC board, layout X0, X1 and crystal oscillator (or ceramic oscillator) and bypass capacitor for grounding as close as possible.

It is strongly recommended to design PC board so that X1 and X0 pins are surrounded by grounding area for stable operation.

3. Notes on Use

•External reset input

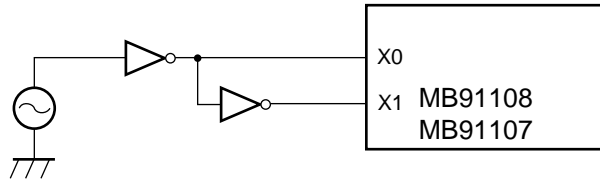
The $\overline{\text{RST}}$ pin requires "L" level input for at least five machine cycles before the the internal circuitry can be completely reset.

•External clock

To use an external clock, in principle, supply the X0 and X1 pins with a clock signal opposite in phase to the X0. To use the STOP mode (oscillation stop mode) along with the external clock, in which the X1 pin stops with "H" output, you should insert an external resistor of about 1 kilohm to prevent a collision between outputs.

Given the next page is an example of using an external clock.

- Using an external clock (for normal use)

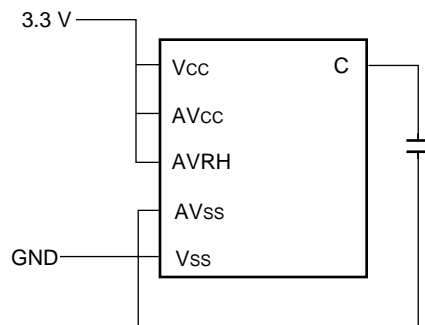


Note: To use the STOP mode (oscillation stop mode), insert a resistor to the X1 pin.

4. Notes on Internal DC-DC Regulator

- Since this product contains a regulator, be sure to supply current at 3.3 V to the VCC pin and insert a bypass capacitor of about 0.1 μ F to the C pin for the regulator.
- The A/D converter requires a 3.3-V power supply separately.

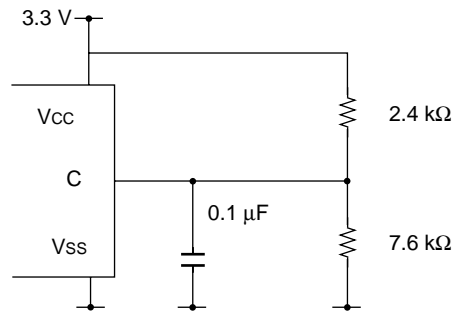
- Connecting to power supply



• Notes on using the STOP mode

The regulator built in this product stops in the STOP mode. If the regulator stops due to a malfunction caused by noise or a fault in the power supply during normal operation, the internal 2.5-V power supply may go below the lower limit of the guaranteed operating voltage range. When using the STOP mode with the internal regulator, therefore, be sure to supply an auxiliary external power to prevent the 3.3-V power supply from coming down. Even in that case, the internal regulator can be restarted by input of a reset signal (To restart the regulator, keep the reset pin at the L level for at least the oscillation settling time).

•Using STOP mode with 3.3 V power supply



5. Turning on the Power Supply

• $\overline{\text{RST}}$ pin

When turning on the power supply, never fail to start from setting the $\overline{\text{RST}}$ pin to “L” level. And after the power supply voltage goes to V_{CC} level, at least after ensuring the time for 5 machine cycles, then set to “H” level.

•Pin Condition at Turning on the Power Supply

The pin condition at turning on the power supply is unstable. The circuit starts being initialized after turning on the power supply and then starting oscillation and then the operation of the internal regulator becomes stable. So it takes about 42 ms for the pin to be initialized from the oscillation starting at the source oscillation 12.5 MHz. Take care that the pin condition may be output condition at initial unstable condition.

(With the MB91107, however, initialization can be achieved in less than about 42 ms after turning on the internal power supply by maintaining the $\overline{\text{RST}}$ pin at “L” level.)

•Source Oscillation Input at Turning on the Power Supply

At turning on the power supply, never fail to input the clock before cancellation of the oscillation stabilizing waiting.

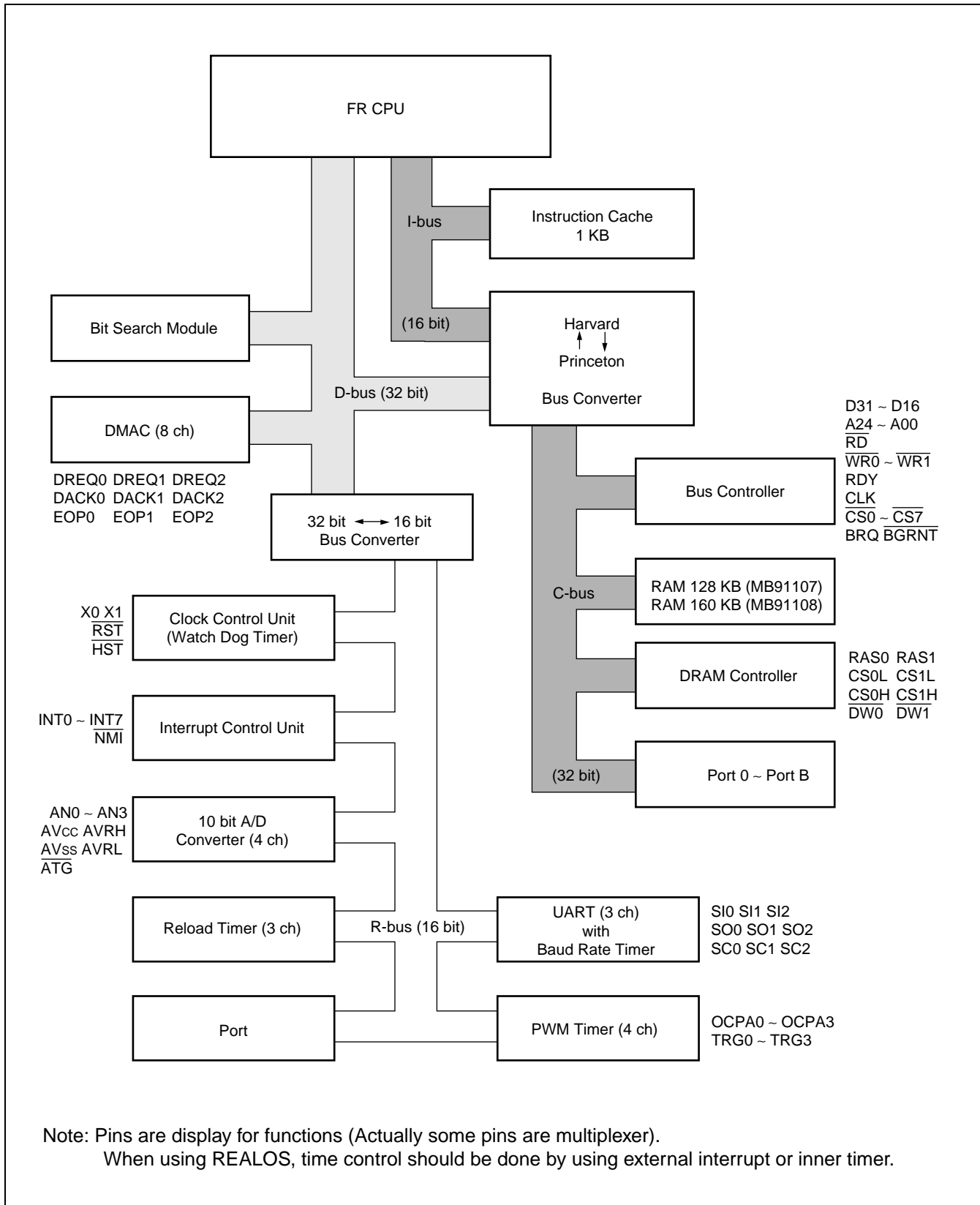
•Hardware Stand-by at Turning on the Power Supply

When turning on the power supply with the $\overline{\text{HST}}$ pin being set to “L” level, the hardware doesn’t stand by. However the $\overline{\text{HST}}$ pin becomes available after the reset cancellation, the $\overline{\text{HST}}$ pin must once be back to “H” level.

•Power on Reset

Make sure to make power on reset at turning on the power supply or returning on the power supply when the power supply voltage is below the warranty range for normal operation.

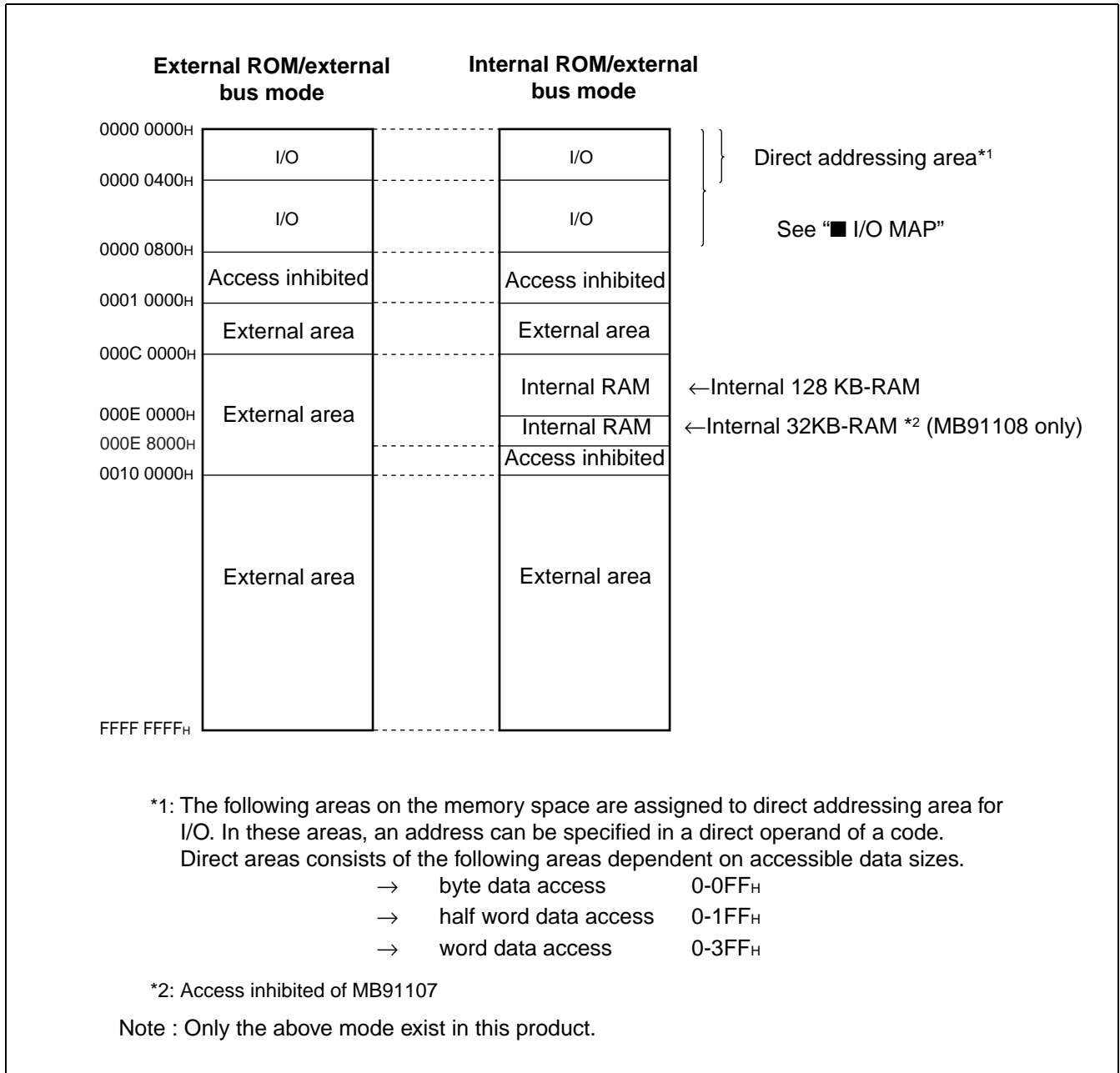
■ BLOCK DIAGRAM



■ CPU CORE

1. Memory Space

The FR family has a logical address space of 4 Gbytes (2^{32} bytes) and the CPU linearly accesses the memory space.



2. Registers

The FR family has two types of registers; dedicated registers embedded on the CPU and general-purpose registers on memory.

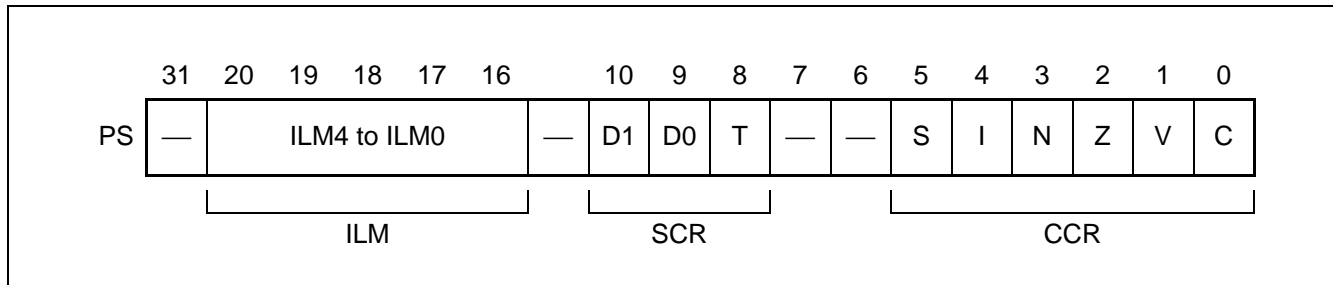
•Dedicated registers

- Program counter (PC) : 32-bit length, indicates the location of the instruction to be executed.
- Program status (PS) : 32-bit length, register for storing register pointer or condition codes.
- Table base register (TBR) : Holds top address of vector table used in EIT (Exceptional/Interrupt/Trap processing).
- Return pointer (RP) : Holds address to resume operation after returning from a subroutine.
- System stack pointer (SSP) : Indicates system stack space.
- User's stack pointer (USP) : Indicates user's stack space.
- Multiplication/division result register (MDH/MDL) : 32-bit length, register for multiplication/division.

	32 bit	← 32 bit →	
Program counter	PC	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	Initial value XXXX XXXX Indeterminate
Program status	PS	<div style="border: 1px solid black; width: 100%; height: 15px; display: flex; justify-content: space-between;"> — ILM — SCR CCR </div>	
Table base register	TBR	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	000F FC00
Return pointer	RP	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	XXXX XXXX Indeterminate
System stack pointer	SSP	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	0000 0000
User's stack pointer	USP	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	XXXX XXXX Indeterminate
Multiplication/division result register	MDH	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	XXXX XXXX Indeterminate
	MDL	<div style="border: 1px solid black; width: 100%; height: 15px;"></div>	XXXX XXXX Indeterminate

•Program status (PS)

The PS register is for holding program status and consists of a condition code register (CCR), a system condition code register (SCR) and a interrupt level mask register (ILM).



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•Condition code register (CCR)

- S-flag : Specifies a stack pointer used as R15.
- I-flag : Controls user interrupt request enable/disable.
- N-flag : Indicates sign bit when division result is assumed to be in the 2's complement format.
- Z-flag : Indicates whether or not the result of division was "0".
- V-flag : Assumes the operand used in calculation in the 2's complement format and indicates whether or not overflow has occurred.
- C-flag : Indicates if a carry or borrow from the MSB has occurred.

•System condition code register (SCR)

- T-flag : Specifies whether or not to enable step trace trap.

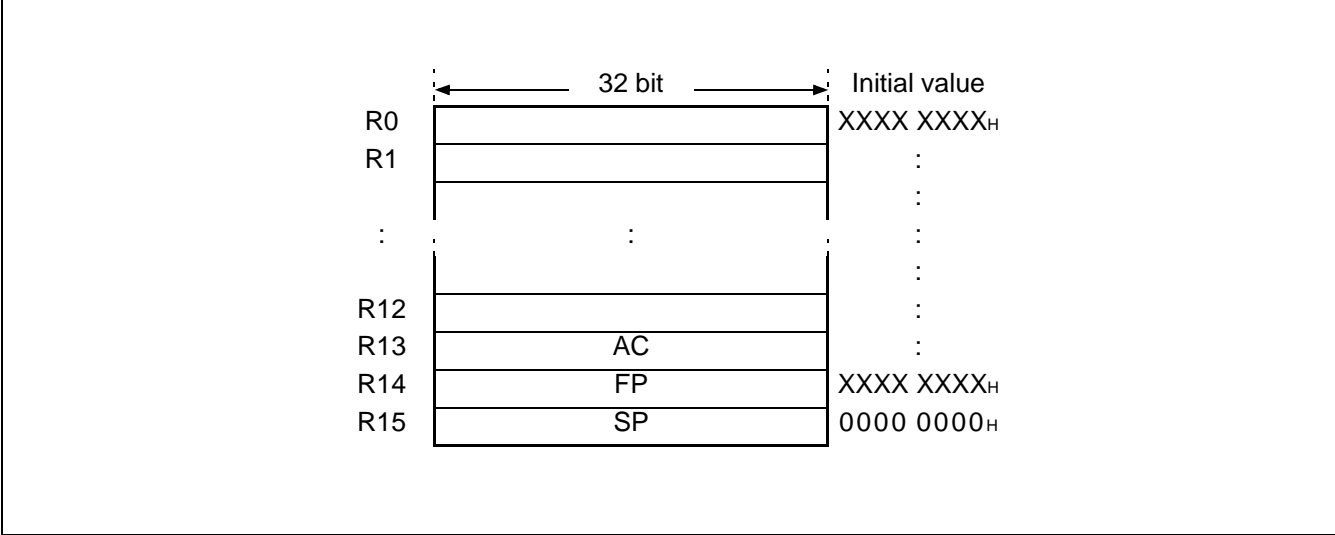
•Interrupt level mask register (ILM)

ILM4 to ILM0 : Register for holding interrupt level mask value. The value held by this register is used as a level mask. When an interrupt request issued to the CPU is higher than the level held by ILM, the interrupt request is accepted.

ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt level	High-low
0	0	0	0	0	0	High
						↑ ↓
0	1	1	1	1	15	
1	1	1	1	1	31	Low

■ GENERAL-PURPOSE REGISTERS

R0 to R15 are general-purpose registers embedded on the CPU. These registers functions as an accumulator and a memory access pointer.



Of the above 16 registers, following registers have special functions. To support the special functions, part of the instruction set has been sophisticated to have enhanced functions.

- R13: Virtual accumulator (AC)
- R14: Frame pointer (FP)
- R15: Stack pointer (SP)

Upon reset, values in R0 to R14 are not fixed. Value in R15 is initialized to be 0000 0000_H (SSP value).

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■ SETTING MODE

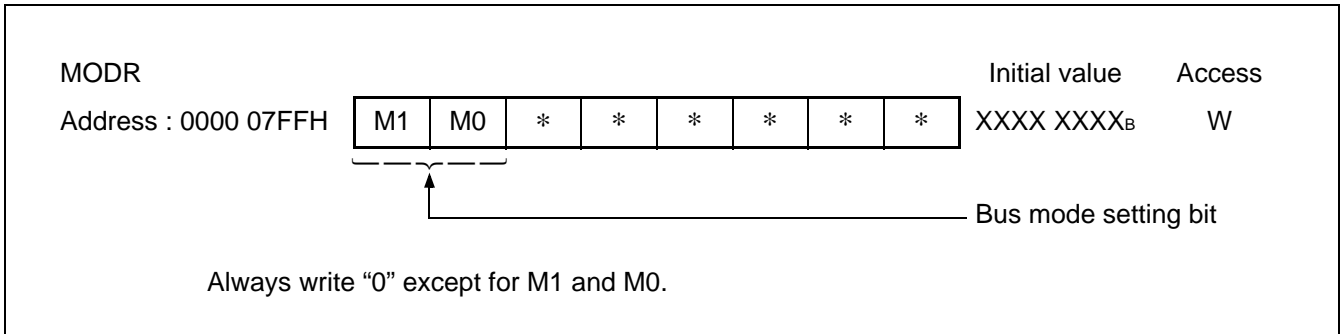
1. Pin

•Mode setting pins and modes

Mode setting pins			Mode name	Reset vector access area	External data bus width	Bus mode
MD2	MD1	MD0				
0	0	0	External vector mode 0	External	8 bits	External ROM/external bus mode
0	0	1	External vector mode 1	External	16 bits	
0	1	0	—	—	—	Inhibited
0	1	1	Internal vector mode	Internal	(Mode register)	Inhibited
1	—	—	—	—	—	Inhibited

2. Registers

•Mode data



•Bus mode setting bits and functions

M1	M0	Functions	Note
0	0	Single-chip mode	
0	1	Internal ROM/external bus mode	Inhibited
1	0	External ROM/external bus mode	
1	1	—	Inhibited

Note : MB91107 places 128-KB internal RAM in the internal ROM area.
To use the 128-KB internal RAM, be sure to set '01'.

■ I/O MAP

The remainder of this section contains a list of the registers for peripheral resources in memory space.

Address	Register name	Register name	Access	Resource name	Initial value
000001 _H	PDR2	Port 2 data registe	R/W	Port Data Register	XXXXXXXX _B
000004 _H	PDR7	Port 7 data registe	R/W		-----X _B
000005 _H	PDR6	Port 6 data registe	R/W		XXXXXXXX _B
000008 _H	PDRB	Port B data registe	R/W		XXXXXXXX _B
000009 _H	PDRA	Port A data registe	R/W		-XXXXXX- _B
00000B _H	PDR8	Port 8 data registe	R/W		--X--XXX _B
000012 _H	PDRE	Port E data registe	R/W		XXXXXXXX _B
000013 _H	PDRF	Port F data registe	R/W		XXXXXXXX _B
000014 _H	PDRG	Port G data registe	R/W		XXXXXXXX _B
000015 _H	PDRH	Port H data registe	R/W		XXXXXXXX0 _B
000016 _H	PDR I	Port I data registe	R/W		-----XX _B
00001C _H	SSR0	Serial status register 0	R/W		UART0
00001D _H	SIDR0/ SODR0	Serial input data register 0/ Serial output data register	R/W	XXXXXXXX _B	
00001E _H	SCR0	Serial control register 0	R/W	0 0 0 0 0 1 0 0 _B	
00001F _H	SMR0	Serial mode register 0	R/W	0 0 -- 0 - 0 0 _B	
000020 _H	SSR1	Serial status register 1	R/W	UART1	0 0 0 0 1 - 0 0 _B
000021 _H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register	R/W		XXXXXXXX _B
000022 _H	SCR1	Serial control register 1	R/W		0 0 0 0 0 1 0 0 _B
000023 _H	SMR1	Serial mode register 1	R/W		0 0 -- 0 - 0 0 _B
000024 _H	SSR2	Serial status register 2	R/W	UART2	0 0 0 0 1 - 0 0 _B
000025 _H	SIDR2/ SODR2	Serial input data register 2/ Serial output data register	R/W		XXXXXXXX _B
000026 _H	SCR2	Serial control register 2	R/W		0 0 0 0 0 1 0 0 _B
000027 _H	SMR2	Serial mode register 2	R/W		0 0 -- 0 - 0 0 _B
000028 _H	TMRLR0	16-bit reload register 0	W	Reload Timer 0	XXXXXXXX _B
000029 _H					XXXXXXXX _B
00002A _H	TMR0	16-bit timer register 0	R		XXXXXXXX _B
00002B _H					XXXXXXXX _B
00002E _H	TMCSR0	16-bit reload timer control status register 0	R/W		---- 0 0 0 0 _B
00002F _H					0 0 0 0 0 0 0 0 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

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Address	Register name	Register name	Access	Resource name	Initial value	
000030 _H	TMRLR1	16-bit reload register 1	W	Reload Timer 1	XXXXXXXX _B	
000031 _H					XXXXXXXX _B	
000032 _H	TMR1	16-bit timer register 1	R		XXXXXXXX _B	
000033 _H					XXXXXXXX _B	
000036 _H	TMCSR1	16-bit reload timer control status register 1	R/W		----0000 _B	
000037 _H					00000000 _B	
000038 _H	ADCR	A/D converter data register	R		A/D Converter (Successive approximation type)	-----XX _B
000039 _H						XXXXXXXX _B
00003A _H	ADCS	A/D converte control status register	R/W	00000000 _B		
00003B _H				00000000 _B		
00003C _H	TMRLR2	16-bit reload register 2	W	XXXXXXXX _B		
00003D _H				XXXXXXXX _B		
00003E _H	TMR2	16-bit timer register 2	R	XXXXXXXX _B		
00003F _H				XXXXXXXX _B		
000042 _H	TMCSR2	16-bit reload timer control status register 2	R/W	----0000 _B		
000043 _H				00000000 _B		
000050 _H	ASR6	Area select register 6	W	External Bus Interface	11111111 _B	
000051 _H					11111111 _B	
000052 _H	AMR6	Area mask register 6	W		00000000 _B	
000053 _H					00000000 _B	
000054 _H	ASR7	Area select register 7	W		11111111 _B	
000055 _H					11111111 _B	
000056 _H	AMR7	Area mask register 7	W		00000000 _B	
000057 _H					00000000 _B	
000059 _H	CS67	Output enable	R/W		----0011 _B	
000078 _H	UTIM0/	U-TIMER register ch.0	R/W		U-TIMER 0	00000000 _B
000079 _H	UTIMR0	U-TIMER reload register ch.0				00000000 _B
00007B _H	UTIMC0	U-TIMER control register ch.0				0--00001 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

Address	Register name	Register name	Access	Resource name	Initial value
00007C _H	UTIM1/ UTIMR1	U-TIMER register ch.1	R/W	U-TIMER 1	0 0 0 0 0 0 0 0 _B
00007D _H		U-TIMER reload register ch.1			0 0 0 0 0 0 0 0 _B
00007F _H	UTIMC1	U-TIMER control register ch.1	R/W		0 -- 0 0 0 0 1 _B
000080 _H	UTIM2/ UTIMR2	U-TIMER register ch.2	R/W	U-TIMER 2	0 0 0 0 0 0 0 0 _B
000081 _H		U-TIMER reload register ch.2			0 0 0 0 0 0 0 0 _B
000083 _H	UTIMC2	U-TIMER control register ch.2	R/W		0 -- 0 0 0 0 1 _B
000094 _H	EIRR	External interrupt request register	R/W	External Interrupt/NMI	0 0 0 0 0 0 0 0 _B
000095 _H	ENIR	Interrupt enable register	R/W		0 0 0 0 0 0 0 0 _B
000098 _H	ELVR	External interrupt request level setup register	R/W		0 0 0 0 0 0 0 0 _B
000099 _H					0 0 0 0 0 0 0 0 _B
0000D2 _H	DDRE	Port E data direction register	W	Port E-I Data Direction Register	0 0 0 0 0 0 0 0 _B
0000D3 _H	DDRF	Port F data direction register	W		0 0 0 0 0 0 0 0 _B
0000D4 _H	DDRG	Port G data direction register	W		0 0 0 0 0 0 0 0 _B
0000D5 _H	DDRH	Port H data direction register	W		0 0 0 0 0 0 0 1 _B
0000D6 _H	DDRI	Port I data direction register	W		-- -- -- -- 0 0 _B
0000DC _H	GCN1	General control register 1	R/W	PWM	0 0 1 1 0 0 1 0 _B
0000DD _H					0 0 0 1 0 0 0 0 _B
0000DF _H	GCN2	General control register 2	R/W		0 0 0 0 0 0 0 0 _B
0000E0 _H	PTMR0	PWM timer register 0	R		1 1 1 1 1 1 1 1 _B
0000E1 _H					1 1 1 1 1 1 1 1 _B
0000E2 _H	PCSR0	PWM cycle setting register 0	W		XXXXXXXX _B
0000E3 _H					XXXXXXXX _B
0000E4 _H	PDUT0	PWM duty setting register 0	W		XXXXXXXX _B
0000E5 _H					XXXXXXXX _B
0000E6 _H	PCNH0	Control status register H 0	R/W		0 0 0 0 0 0 0 - _B
0000E7 _H	PCNL0	Control status register L 0	R/W		0 0 0 0 0 0 0 0 _B
0000E8 _H	PTMR1	PWM timer register 1	R		1 1 1 1 1 1 1 1 _B
0000E9 _H					1 1 1 1 1 1 1 1 _B
0000EA _H	PCSR	PWM cycle setting register 1	W		XXXXXXXX _B
0000EB _H					XXXXXXXX _B
0000EC _H	PDUT	PWM duty setting register 1	W		XXXXXXXX _B
0000ED _H					XXXXXXXX _B
0000EE _H	PCNH	Control status register H 1	R/W		0 0 0 0 0 0 0 - _B
0000EF _H	PCNL	Control status register L 1	R/W		0 0 0 0 0 0 0 0 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

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Address	Register name	Register name	Access	Resource name	Initial value	
0000F0 _H	PTMR2	PWM timer register 2	R	PWM	1 1 1 1 1 1 1 1 _B	
0000F1 _H					1 1 1 1 1 1 1 1 _B	
0000F2 _H	PCSR2	PWM cycle setting register 2	W		XXXXXXXX _B	
0000F3 _H					XXXXXXXX _B	
0000F4 _H	PDUT2	PWM duty setting register 2	W		XXXXXXXX _B	
0000F5 _H					XXXXXXXX _B	
0000F6 _H	PCNH2	Control status register H 2	R/W		0 0 0 0 0 0 0 - _B	
0000F7 _H	PCNL2	Control status register L 2	R/W		0 0 0 0 0 0 0 0 _B	
0000F8 _H	PTMR3	PWM timer register 3	R		1 1 1 1 1 1 1 1 _B	
0000F9 _H					1 1 1 1 1 1 1 1 _B	
0000FA _H	PCSR3	PWM cycle setting register 3	W		XXXXXXXX _B	
0000FB _H					XXXXXXXX _B	
0000FC _H	PDUT3	PWM duty setting register 3	W		XXXXXXXX _B	
0000FD _H					XXXXXXXX _B	
0000FE _H	PCNH3	Control status register H 3	R/W		0 0 0 0 0 0 0 - _B	
0000FF _H	PCNL3	Control status register L 3	R/W		0 0 0 0 0 0 0 0 _B	
000200 _H	DPDP	DMAC parameter descriptor point	R/W	DMAC	XXXXXXXX _B	
000201 _H					XXXXXXXX _B	
000202 _H					XXXXXXXX _B	
000203 _H					X 0 0 0 0 0 0 0 0 _B	
000204 _H	DACSR	DMAC control status register	R/W		0 0 0 0 0 0 0 0 _B	
000205 _H					0 0 0 0 0 0 0 0 _B	
000206 _H					0 0 0 0 0 0 0 0 _B	
000207 _H					0 0 0 0 0 0 0 0 _B	
000208 _H	DATCR	DMAC pin control register	R/W		XXXXXXXX _B	
000209 _H					XX 0 0 0 0 0 0 0 _B	
00020A _H					XX 0 0 0 0 0 0 0 _B	
00020B _H					XX 0 0 0 0 0 0 0 _B	
0003E4 _H	ICHCR	Instruction cache	R/W		Instruction Cache	- - - - - _B
0003E5 _H						- - - - - _B
0003E6 _H						- - - - - _B
0003E7 _H						- - 0 0 0 0 0 0 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

Address	Register name	Register name	Access	Resource name	Initial value
0003F0 _H	BSD0	Bit search module zero-detection data register	W	Bit Search Module	XXXXXXXX _B
0003F1 _H					XXXXXXXX _B
0003F2 _H					XXXXXXXX _B
0003F3 _H					XXXXXXXX _B
0003F4 _H	BSD1	Bit search module single-detection data register	R/W		XXXXXXXX _B
0003F5 _H					XXXXXXXX _B
0003F6 _H					XXXXXXXX _B
0003F7 _H					XXXXXXXX _B
0003F8 _H	BSDC	Bit search module transition-detection data register	W		XXXXXXXX _B
0003F9 _H					XXXXXXXX _B
0003FA _H					XXXXXXXX _B
0003FB _H					XXXXXXXX _B
0003FC _H	BSRR	Bit search module result register	R		XXXXXXXX _B
0003FD _H					XXXXXXXX _B
0003FE _H					XXXXXXXX _B
0003FF _H					XXXXXXXX _B
000400 _H	ICR00	Interrupt control register 0	R/W	Interrupt Controller	--- 1 1 1 1 1 _B
000401 _H	ICR01	Interrupt control register 1			--- 1 1 1 1 1 _B
000402 _H	ICR02	Interrupt control register 2			--- 1 1 1 1 1 _B
000403 _H	ICR03	Interrupt control register 3			--- 1 1 1 1 1 _B
000404 _H	ICR04	Interrupt control register 4			--- 1 1 1 1 1 _B
000405 _H	ICR05	Interrupt control register 5			--- 1 1 1 1 1 _B
000406 _H	ICR06	Interrupt control register 6			--- 1 1 1 1 1 _B
000407 _H	ICR07	Interrupt control register 7			--- 1 1 1 1 1 _B
000408 _H	ICR08	Interrupt control register 8			--- 1 1 1 1 1 _B
000409 _H	ICR09	Interrupt control register 9			--- 1 1 1 1 1 _B
00040A _H	ICR10	Interrupt control register 10			--- 1 1 1 1 1 _B
00040B _H	ICR11	Interrupt control register 11			--- 1 1 1 1 1 _B
00040C _H	ICR12	Interrupt control register 12			--- 1 1 1 1 1 _B
00040D _H	ICR13	Interrupt control register 13			--- 1 1 1 1 1 _B
00040E _H	ICR14	Interrupt control register 14			--- 1 1 1 1 1 _B
00040F _H	ICR15	Interrupt control register 15			--- 1 1 1 1 1 _B
000410 _H	ICR16	Interrupt control register 16			--- 1 1 1 1 1 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

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Address	Register name	Register name	Access	Resource name	Initial value
000411 _H	ICR17	Interrupt control register17	R/W	Interrupt Controller	--- 1 1 1 1 1 _B
000412 _H	ICR18	Interrupt control register 18			--- 1 1 1 1 1 _B
000413 _H	ICR19	Interrupt control register 19			--- 1 1 1 1 1 _B
000414 _H	ICR20	Interrupt control register 20			--- 1 1 1 1 1 _B
000415 _H	ICR21	Interrupt control register 21			--- 1 1 1 1 1 _B
000416 _H	ICR22	Interrupt control register 22			--- 1 1 1 1 1 _B
000417 _H	ICR23	Interrupt control register 23			--- 1 1 1 1 1 _B
000418 _H	ICR24	Interrupt control register 24			--- 1 1 1 1 1 _B
000419 _H	ICR25	Interrupt control register 25			--- 1 1 1 1 1 _B
00041A _H	ICR26	Interrupt control register 26			--- 1 1 1 1 1 _B
00041B _H	ICR27	Interrupt control register 27			--- 1 1 1 1 1 _B
00041C _H	ICR28	Interrupt control register 28			--- 1 1 1 1 1 _B
00041D _H	ICR29	Interrupt control register 29			--- 1 1 1 1 1 _B
00041E _H	ICR30	Interrupt control register 30			--- 1 1 1 1 1 _B
00041F _H	ICR31	Interrupt control register 31			--- 1 1 1 1 1 _B
000420 _H	ICR32	Interrupt control register 32			--- 1 1 1 1 1 _B
000421 _H	ICR33	Interrupt control register 33			--- 1 1 1 1 1 _B
000422 _H	ICR34	Interrupt control register 34			--- 1 1 1 1 1 _B
000423 _H	ICR35	Interrupt control register 35			--- 1 1 1 1 1 _B
000424 _H	ICR36	Interrupt control register 36			--- 1 1 1 1 1 _B
000425 _H	ICR37	Interrupt control register 37			--- 1 1 1 1 1 _B
000426 _H	ICR38	Interrupt control register 38			--- 1 1 1 1 1 _B
000427 _H	ICR39	Interrupt control register 39			--- 1 1 1 1 1 _B
000428 _H	ICR40	Interrupt control register 40			--- 1 1 1 1 1 _B
000429 _H	ICR41	Interrupt control register 41			--- 1 1 1 1 1 _B
00042A _H	ICR42	Interrupt control register 42			--- 1 1 1 1 1 _B
00042B _H	ICR43	Interrupt control register 43			--- 1 1 1 1 1 _B
00042C _H	ICR44	Interrupt control register 44	--- 1 1 1 1 1 _B		
00042D _H	ICR45	Interrupt control register 45	--- 1 1 1 1 1 _B		
00042E _H	ICR46	Interrupt control register 46	--- 1 1 1 1 1 _B		
00042F _H	ICR47	Interrupt control register 47	--- 1 1 1 1 1 _B		
000430 _H	DICR	Delayed interrupt	R/W	Delayed Interrupt Controller Register	----- 0 _B
000431 _H	HRCL	Holding request withdrawal request level set register	R/W		--- 1 1 1 1 1 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

Address	Register name	Register name	Access	Resource name	Initial value
000480 _H	RSRR/ WTCR	Reset cause register/watchdog cycle control register	R/W	Clock Controller	1 XXXX – 0 0 _B
000481 _H	STCR	Stand-by controller register	R/W		0 0 0 1 1 1 – – _B
000482 _H	PDRR	DMA controller request prohibit resister	R/W		– – – – 0 0 0 0 _B
000483 _H	CTBR	Timebase timer clear register	W		XXXXXXXX _B
000484 _H	GCR	Gear controller register	R/W		1 1 0 0 1 1 – 1 _B
000485 _H	WPR	Watchdog reset generation postpone register	W		XXXXXXXX _B
000488 _H	PCTR	PLL controller register	W	PLL Controller	0 0 – – 0 – – – _B
000601 _H	DDR2	Port 2 data direction register	W	Port Direction Register	0 0 0 0 0 0 0 0 _B
000604 _H	DDR7	Port 7 data direction register	W		– – – – – – 0 _B
000605 _H	DDR6	Port 6 data direction register	W		0 0 0 0 0 0 0 0 _B
000608 _H	DDRB	Port B data direction register	W		0 0 0 0 0 0 0 0 _B
000609 _H	DDRA	Port A data direction register	W		– 0 0 0 0 0 0 – _B
00060B _H	DDR8	Port 8 data direction register	W		– – 0 0 0 0 0 0 _B
00060C _H	ASR1	Area selection register 1	W	External Bus Interface	0 0 0 0 0 0 0 0 _B
00060D _H					0 0 0 0 0 0 0 1 _B
00060E _H	AMR1	Area mask register 1	W		0 0 0 0 0 0 0 0 _B
00060F _H					0 0 0 0 0 0 0 0 _B
000610 _H	ASR2	Area selection register 2	W		0 0 0 0 0 0 0 0 _B
000611 _H					0 0 0 0 0 0 1 0 _B
000612 _H	AMR2	Area mask register 2	W		0 0 0 0 0 0 0 0 _B
000613 _H					0 0 0 0 0 0 0 0 _B
000614 _H	ASR3	Area selection register 3	W		0 0 0 0 0 0 0 0 _B
000615 _H					0 0 0 0 0 0 1 1 _B
000616 _H	AMR3	Area mask register 3	W		0 0 0 0 0 0 0 0 _B
000617 _H					0 0 0 0 0 0 0 0 _B
000618 _H	ASR4	Area selection register 4	W		0 0 0 0 0 0 0 0 _B
000619 _H					0 0 0 0 0 1 0 0 _B
00061A _H	AMR4	Area mask register 4	W		0 0 0 0 0 0 0 0 _B
00061B _H					0 0 0 0 0 0 0 0 _B
00061C _H	ASR5	Area selection register 5	W		0 0 0 0 0 0 0 0 _B
00061D _H					0 0 0 0 0 1 0 1 _B

Note : Do not execute an RMW-type instruction for any register containing a write-only bit.

(Continued)

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(Continued)

Address	Register name	Register name	Access	Resource name	Initial value	
00061E _H	AMR5	Area mask register 5	W	External Bus Interface	0 0 0 0 0 0 0 0 _B	
00061F _H					0 0 0 0 0 0 0 0 _B	
000620 _H	AMD0	Area mode register 0	R/W		---00111 _B	
000621 _H	AMD1	Area mode register 1	R/W		0--00000 _B	
000622 _H	AMD32	Area mode register 32	R/W		0 0 0 0 0 0 0 0 _B	
000623 _H	AMD4	Area mode register 4	R/W		0--00000 _B	
000624 _H	AMD5	Area mode register 5	R/W		0--00000 _B	
000625 _H	DSCR	DRAM signal control register	W		0 0 0 0 0 0 0 0 _B	
000626 _H	RFCR	Refresh control register	R/W		--XXXXXX _B	
000627 _H					00---000 _B	
000628 _H	EPCR0	External pin control register 0	W		----1100 _B	
000629 _H					-1111111 _B	
00062A _H	EPCR1	External pin control register 1	W		-----1 _B	
00062B _H					11111111 _B	
00062C _H	DMCR4	DRAM control register 4	R/W		0 0 0 0 0 0 0 0 _B	
00062D _H					0 0 0 0 0 0 0 - _B	
00062E _H	DMCR5	DRAM control register 5	R/W		0 0 0 0 0 0 0 0 _B	
00062F _H					0 0 0 0 0 0 0 - _B	
0007FE _H	LER	Little endian register	W		Little Endian Register	-----000 _B
0007FF _H	MODR	Mode register	W		Mode Register	XXXXXXXX _B

Note: Do not execute an RMW-type instruction for any register containing a write-only bit.

Note : RMW-type instructions (RMW: Read modify write)

AND	Rj, @Ri	OR	Rj, @Ri	EOR	Rj, @Ri
ANDH	Rj, @Ri	ORH	Rj, @Ri	EORH	Rj, @Ri
ANDB	Rj, @Ri	ORB	Rj, @Ri	EORB	Rj, @Ri
BANDL	#u4, @Ri	BORL	#u4, @Ri	BEORL	#u4, @Ri
BANDH	#u4, @Ri	BORH	#u4, @Ri	BEORH	#u4, @Ri

■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
Reset	0	00	—	3FC _H	0FFFFC _H
Reserved for system	1	01	—	3F8 _H	0FFFF8 _H
Reserved for system	2	02	—	3F4 _H	0FFFF4 _H
Reserved for system	3	03	—	3F0 _H	0FFFF0 _H
Reserved for system	4	04	—	3EC _H	0FFFE _C
Reserved for system	5	05	—	3E8 _H	0FFFE8 _H
Reserved for system	6	06	—	3E4 _H	0FFFE4 _H
Reserved for system	7	07	—	3E0 _H	0FFFE0 _H
Reserved for system	8	08	—	3DC _H	0FFFD _C
Reserved for system	9	09	—	3D8 _H	0FFFD8 _H
Reserved for system	10	0A	—	3D4 _H	0FFFD4 _H
Reserved for system	11	0B	—	3D0 _H	0FFFD0 _H
Reserved for system	12	0C	—	3CC _H	0FFF _C
Reserved for system	13	0D	—	3C8 _H	0FFFC8 _H
Exception for undefined instruction	14	0E	—	3C4 _H	0FFFC4 _H
NMI request	15	0F	F _H fixed	3C0 _H	0FFFC0 _H
External interrupt 0	16	10	ICR00	3BC _H	0FFFBC _H
External interrupt 1	17	11	ICR01	3B8 _H	0FFFB8 _H
External interrupt 2	18	12	ICR02	3B4 _H	0FFFB4 _H
External interrupt 3	19	13	ICR03	3B0 _H	0FFFB0 _H
UART0 receive complete	20	14	ICR04	3AC _H	0FFFAC _H
UART1 receive complete	21	15	ICR05	3A8 _H	0FFFA8 _H
UART2 receive complete	22	16	ICR06	3A4 _H	0FFFA4 _H
UART0 transmit complete	23	17	ICR07	3A0 _H	0FFFA0 _H
UART1 transmit complete	24	18	ICR08	39C _H	0FFF9C _H
UART2 transmit complete	25	19	ICR09	398 _H	0FFF98 _H
DMAC0 (complete, error)	26	1A	ICR10	394 _H	0FFF94 _H
DMAC1 (complete, error)	27	1B	ICR11	390 _H	0FFF90 _H
DMAC2 (complete, error)	28	1C	ICR12	38C _H	0FFF8C _H
DMAC3 (complete, error)	29	1D	ICR13	388 _H	0FFF88 _H
DMAC4 (complete, error)	30	1E	ICR14	384 _H	0FFF84 _H
DMAC5 (complete, error)	31	1F	ICR15	380 _H	0FFF80 _H
DMAC6 (complete, error)	32	20	ICR16	37C _H	0FFF7C _H
DMAC7 (complete, error)	33	21	ICR17	378 _H	0FFF78 _H

(Continued)

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(Continued)

Interrupt causes	Interrupt number		Interrupt level		TBR default address
	Decimal	Hexadecimal	Register	Offset	
A/D converter (successive approximation conversion type)	34	22	ICR18	374 _H	0FFF74 _H
Reload timer 0	35	23	ICR19	370 _H	0FFF70 _H
Reload timer 1	36	24	ICR20	36C _H	0FFF6C _H
Reload timer 2	37	25	ICR21	368 _H	0FFF68 _H
PWM0	38	26	ICR22	364 _H	0FFF64 _H
PWM1	39	27	ICR23	360 _H	0FFF60 _H
PWM2	40	28	ICR24	35C _H	0FFF5C _H
PWM3	41	29	ICR25	358 _H	0FFF58 _H
U-TIMER0	42	2A	ICR26	354 _H	0FFF54 _H
U-TIMER1	43	2B	ICR27	350 _H	0FFF50 _H
U-TIMER2	44	2C	ICR28	34C _H	0FFF4C _H
Reserved for system	45	2D	ICR29	348 _H	0FFF48 _H
Reserved for system	46	2E	ICR30	344 _H	0FFF44 _H
Reserved for system	47	2F	ICR31	340 _H	0FFF40 _H
Reserved for system	48	30	ICR32	33C _H	0FFF3C _H
Reserved for system	49	31	ICR33	338 _H	0FFF38 _H
Reserved for system	50	32	ICR34	334 _H	0FFF34 _H
Reserved for system	51	33	ICR35	330 _H	0FFF30 _H
Reserved for system	52	34	ICR36	32C _H	0FFF2C _H
Reserved for system	53	35	ICR37	328 _H	0FFF28 _H
Reserved for system	54	36	ICR38	324 _H	0FFF24 _H
Reserved for system	55	37	ICR39	320 _H	0FFF20 _H
Reserved for system	56	38	ICR40	31C _H	0FFF1C _H
Reserved for system	57	39	ICR41	318 _H	0FFF18 _H
Reserved for system	58	3A	ICR42	314 _H	0FFF14 _H
Reserved for system	59	3B	ICR43	310 _H	0FFF10 _H
Reserved for system	60	3C	ICR44	30C _H	0FFF0C _H
Reserved for system	61	3D	ICR45	308 _H	0FFF08 _H
Reserved for system	62	3E	ICR46	304 _H	0FFF04 _H
Delayed interrupt cause bit	63	3F	ICR47	300 _H	0FFF00 _H
Reserved for system (used in REALOS*)	64	40	—	2FC _H	0FFEFC _H
Reserved for system (used in REALOS*)	65	41	—	2F8 _H	0FFE8 _H
Used in INT instructions	66 to 255	42 to FF	—	2F4 _H to 000 _H	0FFE4 _H to 0FFC0 _H

*: When using in REALOS/FR, interrupt 0x40, 0x41 for system code.

■ PERIPHERAL RESOURCES

1. I/O Ports

There are 2 types of I/O port register structure; PDR (port data register) and DDR (data direction register) .

- For input (DDR = "0") setting;
 PDR reading operation: reads level of corresponding external pin.
 PDR writing operation: writes set value to PDR.
- For output (DDR = "1") setting;
 PDR reading operation: reads PDR value.
 PDR writing operation: outputs PDR value to corresponding external pin.

(1) Register configuration

•Port Data Register (PDR)				
Address	bit 7	bit 0	Initial value	Access
000001H	PDR2		XXXXXXXX _B	R/W
000005H	PDR6		XXXXXXXX _B	R/W
000004H	PDR7		-----X _B	R/W
00000BH	PDR8		--X--XXX _B	R/W
000009H	PDRA		-XXXXXX- _B	R/W
000008H	PDRB		XXXXXXXX _B	R/W
000012H	PDRE		XXXXXXXX _B	R/W
000013H	PDRF		XXXXXXXX _B	R/W
000014H	PDRG		XXXXXXXX _B	R/W
000015H	PDRH		XXXXXXXX0 _B	R/W
000016H	PDRI		-----XX _B	R/W

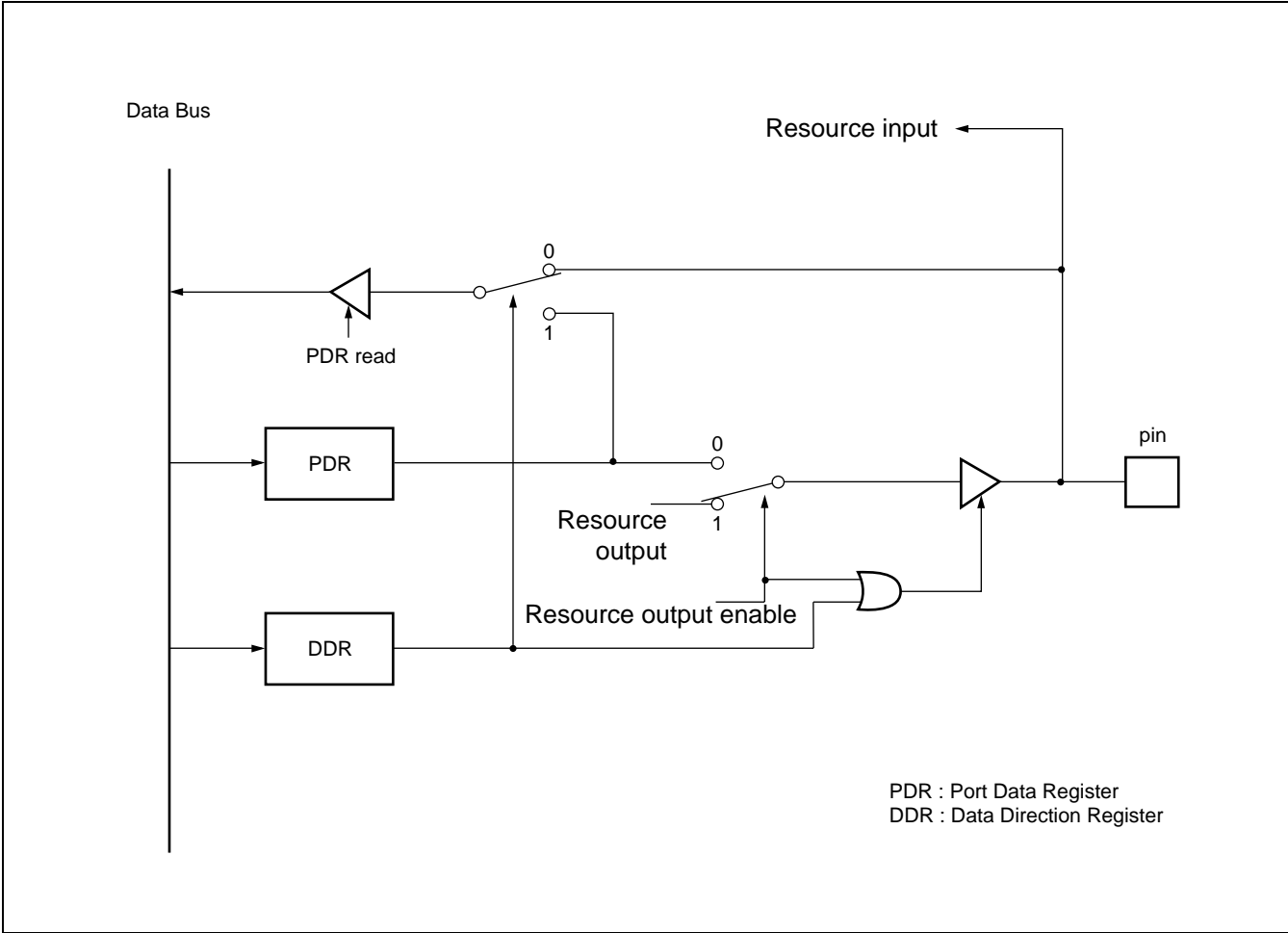
R/W : Readable and writable
 - : Unused
 X : Indeterminate

•Data Direction Register (DDR)

Address	bit 7	bit 0	Initial value	Access
000601H	DDR2		00000000 _B	W
000605H	DDR6		00000000 _B	W
000604H	DDR7		- - - - - 0 _B	W
00060BH	DDR8		- - 0 - - 00 _B	W
000609H	DDRA		- 000000 - _B	W
000608H	DDRB		00000000 _B	W
0000D2H	DDRE		00000000 _B	W
0000D3H	DDRF		00000000 _B	W
0000D4H	DDRG		00000000 _B	W
0000D5H	DDRH		00000001 _B	W
0000D6H	DDRI		- - - - - 00 _B	W

W : Write only
 - : Unused

(2) Block diagram



2. DMA Controller (DMAC)

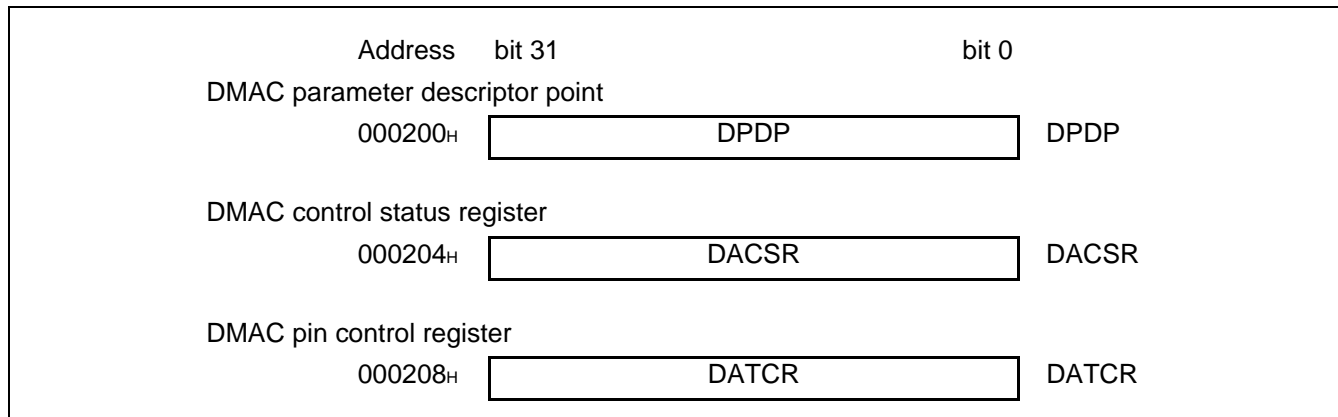
The DMA controller is a module embedded in FR family devices, and performs DMA (direct memory access) transfer.

DMA transfer performed by the DMA controller transfers data without intervention of CPU, contributing to enhanced performance of the system.

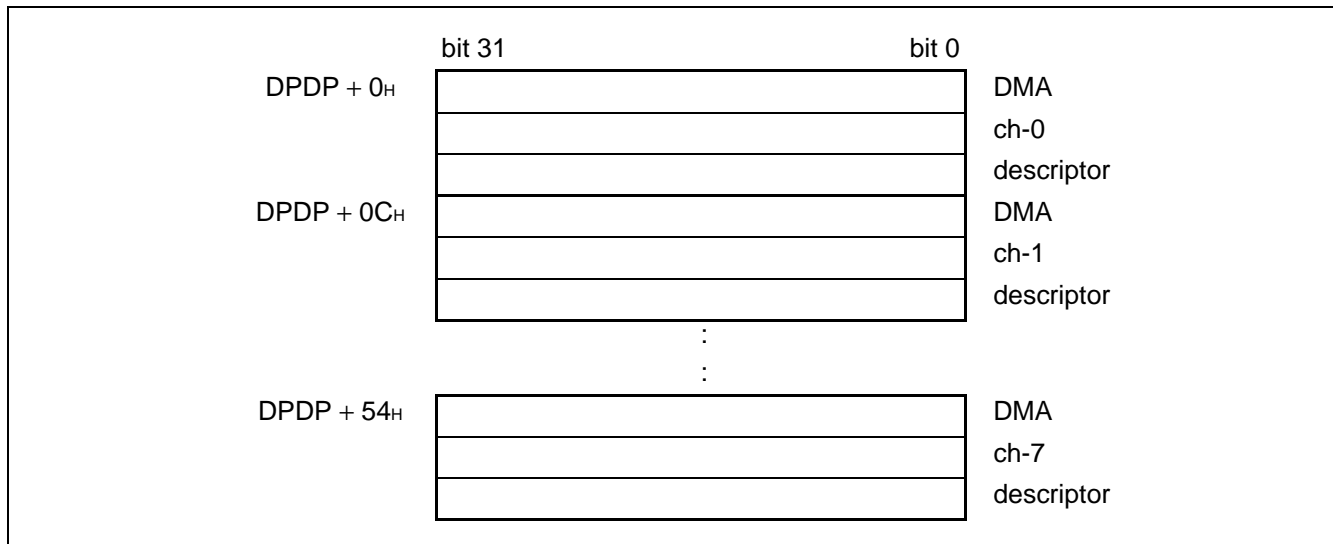
- 8 channels
- Mode: single/block transfer, burst transfer and continuous transfer: 3 kinds of transfer
- Transfer all through the area
- Max. 65536 of transfer cycles
- Interrupt function right after the transfer
- Selectable for address transfer increase/decrease by the software
- External transfer request input pin, external transfer request accept output pin, external transfer complete output pin three pins for each

(1) Register configuration

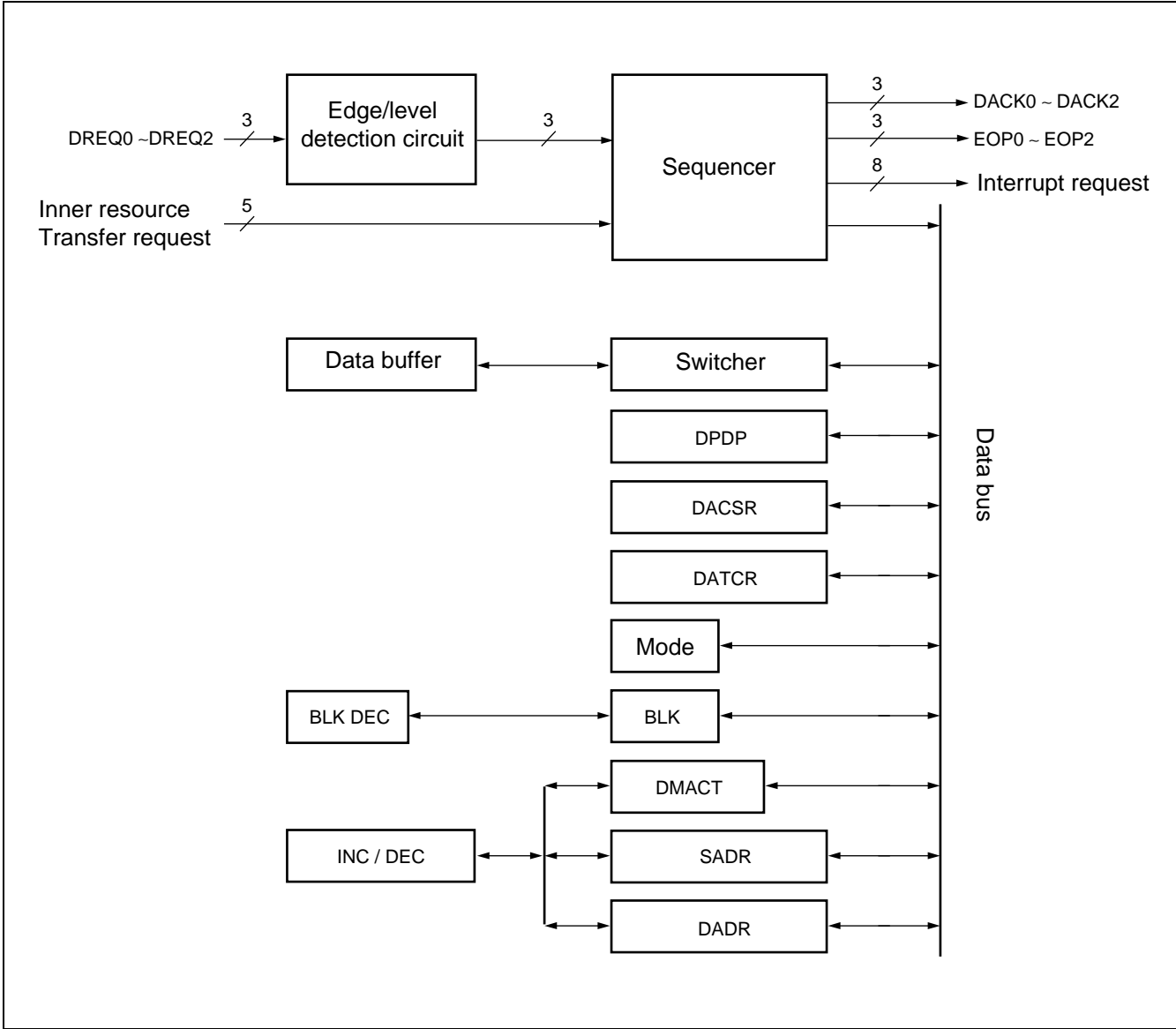
DMAC (DMAC internal registers)



RAM (DMA descriptor)



(2) Block diagram



3. UART

The UART is a serial I/O port for supporting asynchronous (start-stop system) communication or CLK synchronous communication, and it has the following features.

The MB91107 consists of 3 channels of UART.

- Full double double buffer
- Both a synchronous (start-stop system) communication and CLK synchronous communication are available.
- Supporting multi-processor mode
- Perfect programmable baud rate

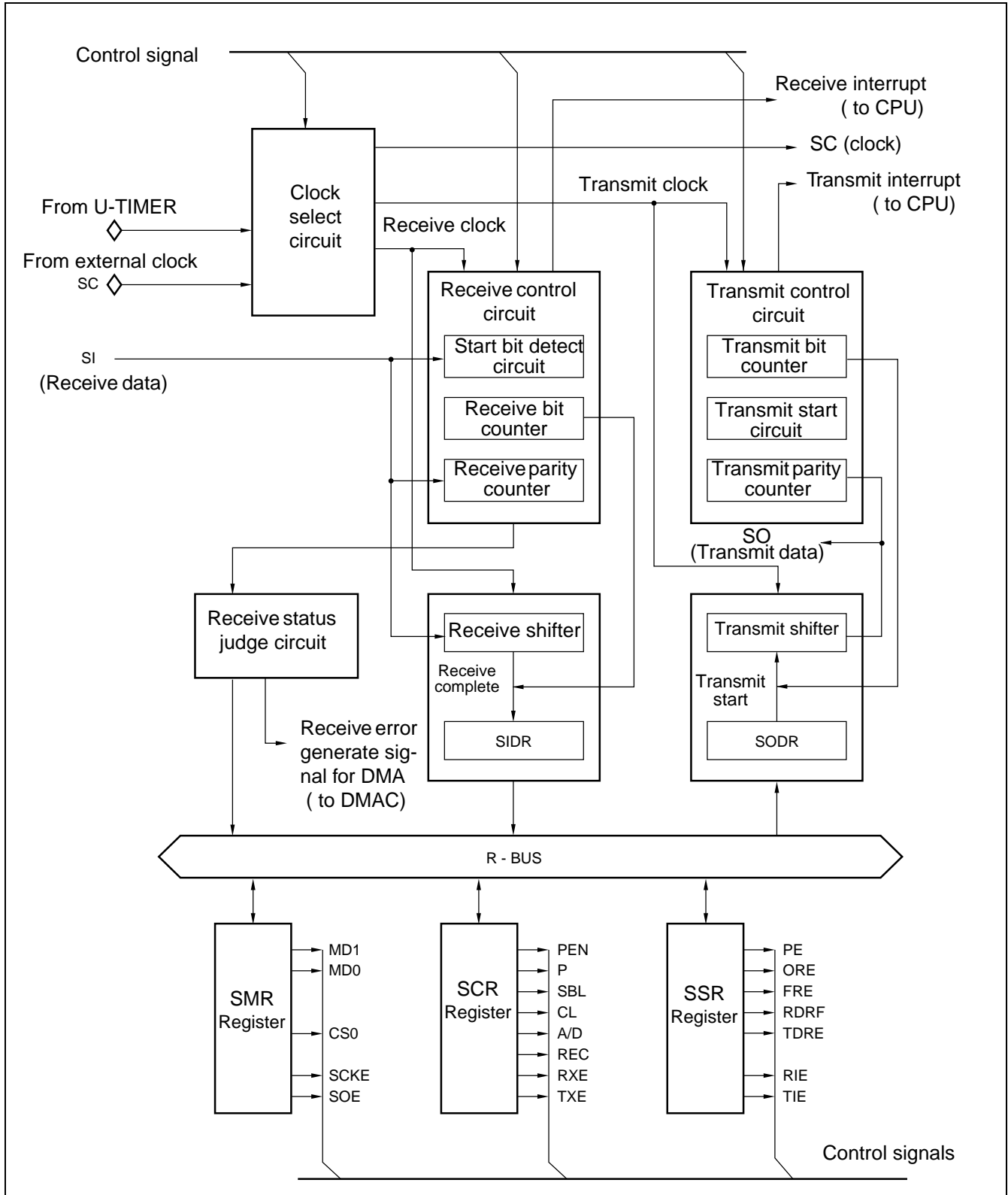
Any baud rate can be set by internal timer (refer to section “4. U-TIMER”).

- Any baud rate can be set by external clock.
- Error checking function (parity, framing and overrun)
- Transfer signal: NRZ code
- Enable DMA transfer/start by interrupt.

(1) Register configuration

•Serial control register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
SCR0 : 00001EH	SCR0 to SCR2		(SMR)		00000100 _B	R/W
SCR1 : 000022H						
SCR2 : 000026H						
•Serial mode register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
SMR0 : 00001FH	(SCR)		SMR0 to SMR2		00 - - 0 - 00 _B	R/W
SMR1 : 000023H						
SMR2 : 000027H						
•Serial status register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
SSR0 : 00001CH	SSR0 to SSR2		(SIDR/SODR)		00001 - 00 _B	R/W
SSR1 : 000020H						
SSR2 : 000024H						
•Serial input data register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
SIDR0 : 00001DH	(SSR)		(SIDR/SODR)		XXXXXXXX _B	R
SIDR1 : 000021H						
SIDR2 : 000025H						
•Serial output data register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
SIDR0 : 00001DH	(SSR)		(SIDR/SODR)		XXXXXXXX _B	R
SIDR1 : 000021H						
SIDR2 : 000025H						
R/W : Readable and writable - : Unused R : Read only X : Indeterminate W : Write only						

(2) Block diagram



4. U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-TIMER is a 16-bit timer for generating UART baud rate. Combination of chip operating frequency and reload value of U-TIMER allows flexible setting of baud rate.

The U-TIMER operates as an interval timer by using interrupt issued on counter underflow.

The MB91107 has 3 channel U-TIMER embedded on the chip. An interval of up to $2^{16} \times \phi$ can be counted.

(1) Register configuration

- U-TIMER register ch 0 to ch 2

Address	bit 15	bit 0	Initial value	Access
UTIM0 : 000078 _H	UTIM0 to UTIM2		00000000 _B	R
UTIM1 : 00007C _H			00000000 _B	
UTIM2 : 000080 _H				

- U-TIMER reload register ch 0 to ch 2

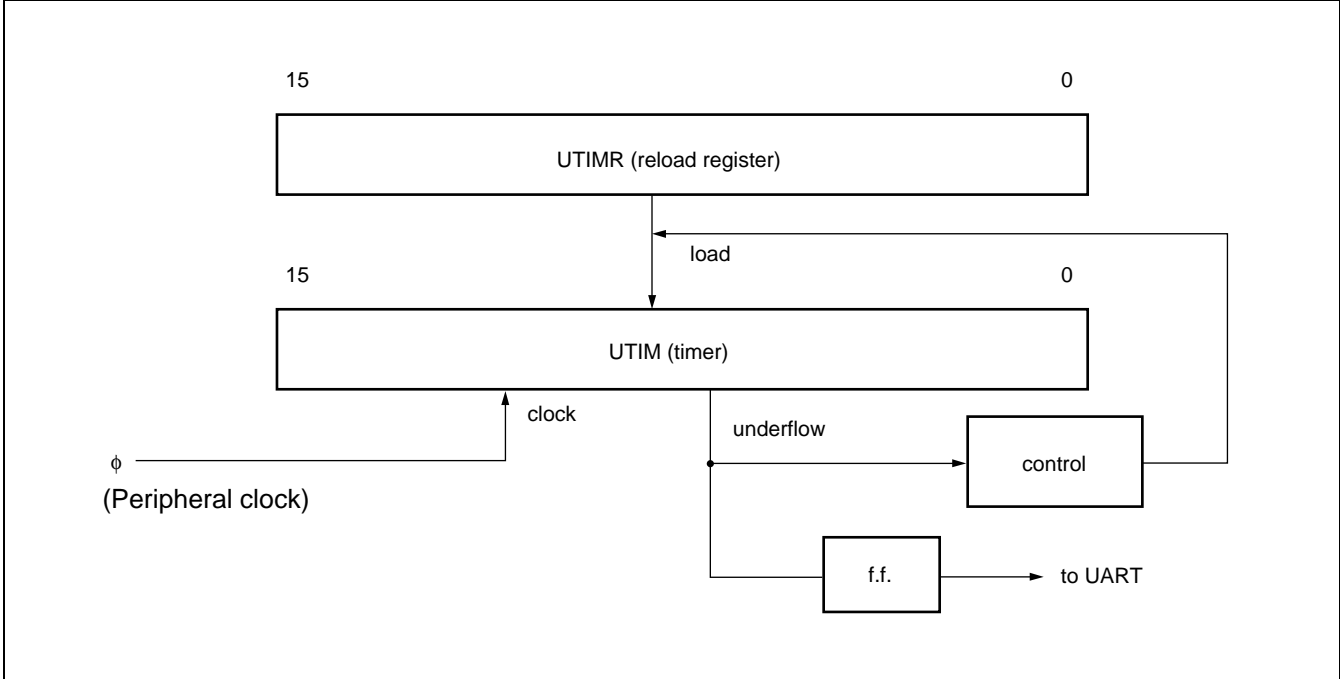
Address	bit 15	bit 0	Initial value	Access
UTIM0 : 000078 _H	UTIM0 to UTIM2		00000000 _B	W
UTIM1 : 00007C _H			00000000 _B	
UTIM2 : 000080 _H				

- U-TIMER control register ch 0 to ch 2

Address	bit 15	bit 0	Initial value	Access
UTIM0 : 00007B _H	(Vacancy)	UTIMC0 to UTIMC2	0 - - 00001 _B	R/W
UTIM1 : 00007F _H				
UTIM2 : 000083 _H				

R/W : Readable and writable
 R : Read only
 W : Write only
 - : Unused

(2) Block diagram



5. PWM Timer

The PWM timer can output high accurate PWM waves efficiently.

MB91101 has inner 4-channel PWM timers, and has the following features.

- Each channel consists of a 16-bit down counter, a 16-bit data register with a buffer for cycle setting, a 16-bit compare register with a buffer for duty setting, and a pin controller.
 - The count clock of a 16-bit down counter can be selected from the following four inner clocks.
 - Inner clock ϕ , $\phi/4$, $\phi/16$, $\phi/64$
 - The counter value can be initialized “FFFF_H” by the resetting or the counter borrow.
 - PWM output (each channel)
 - Resister description
 - Cycle setting register: Reload data register with a buffer
 - Duty factor setting register: Compare register with a buffer
 - Transfer from the buffers uses the counter borrow method.
 - Pin control outline
 - Set to '1' at a duty factor match. (Preferential)
 - Set to '0' at a counter borrow.
 - The output value fixed mode is available, which makes all 'L' (or 'H') output easy.
 - The polarity can also be specified.
 - Interrupt requests can be generated by selected a combination of events:
 - This timer is activated.
 - A counter borrow is generated (cycle match).
 - A duty factor match is generated.
 - A counter borrow is generated (cycle match) or a duty factor match is generated.
- DMA transfer can be invoked by the above interrupt request.
- Simultaneous activation of multiple channels of the PWM timer can be set by software or by using another interval timer. Restarting the PWM timer during operation can also be set.

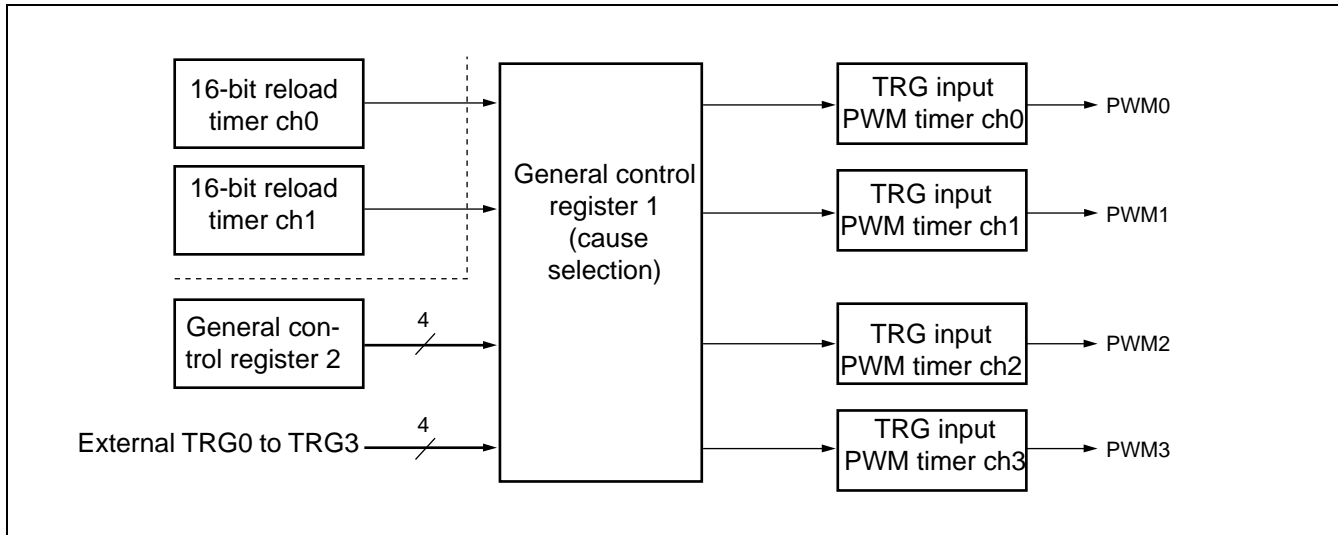
(1) Register configuration

Address	bit 15	bit 0	Initial value	Access	
0000DC _H	GCN1		00110010 _B 00010000 _B	R/W	General control register 1
0000DF _H	GCN2		00000000 _B	R/W	General control register 2
0000E0 _H	PTMR		11111111 _B 11111111 _B	R	ch0 timer register
0000E2 _H	PCSR		XXXXXXXX _B XXXXXXXX _B	W	ch0 cycle setting register
0000E4 _H	PDUT		XXXXXXXX _B XXXXXXXX _B	W	ch0 duty setting register
0000E6 _H	PCNH	PCNL	0000000- _B 00000000 _B	R/W	ch0 control status register
0000E8 _H	PTMR		11111111 _B 11111111 _B	R	ch1 timer register
0000EA _H	PCSR		XXXXXXXX _B XXXXXXXX _B	W	ch1 cycle setting register
0000EC _H	PDUT		XXXXXXXX _B XXXXXXXX _B	W	ch1 duty setting register
0000EE _H	PCNH	PCNL	0000000- _B 00000000 _B	R/W	ch1 control status register
0000F0 _H	PTMR		11111111 _B 11111111 _B	R	ch2 timer register
0000F2 _H	PCSR		XXXXXXXX _B XXXXXXXX _B	W	ch2 cycle setting register
0000F4 _H	PDUT		XXXXXXXX _B XXXXXXXX _B	W	ch2 duty setting register
0000F6 _H	PCNH	PCNL	0000000- _B 00000000 _B	R/W	ch2 control status register
0000F8 _H	PTMR		11111111 _B 11111111 _B	R	ch3 timer register
0000FA _H	PCSR		XXXXXXXX _B XXXXXXXX _B	(W)	ch3 cycle setting register
0000FC _H	PDUT		XXXXXXXX _B XXXXXXXX _B	W	ch3 duty setting register
0000FE _H	PCNH	PCNL	0000000- _B 00000000 _B	R/W	ch3 control status register

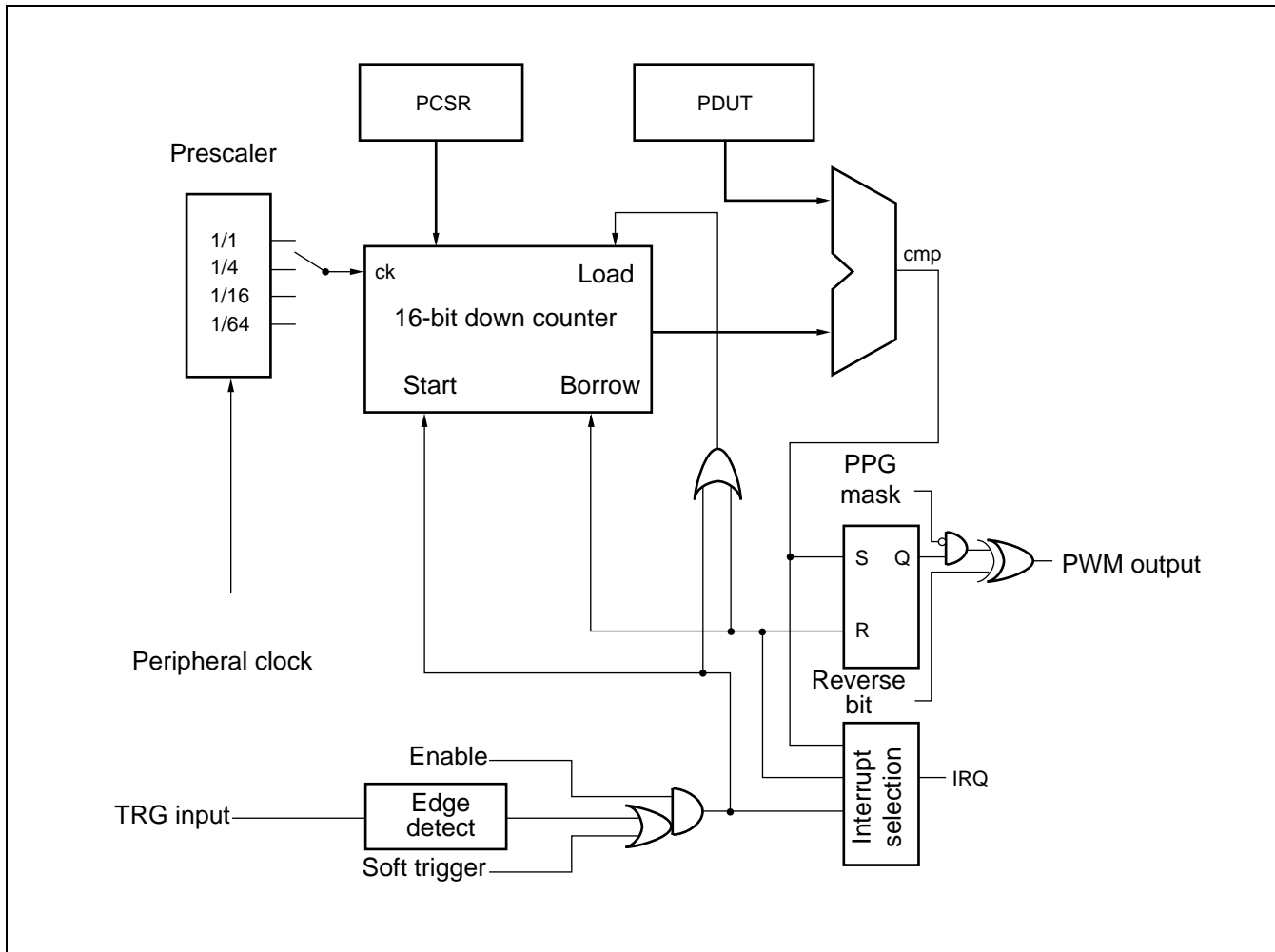
R/W	: Readable and writable	-	: Unused
R	: Read only	X	: Indeterminate
W	: Write only		

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(2) Block Diagram
•General construction



•For one channel



6. 16-bit Reload Timer

The 16-bit reload timer consists of a 16-bit down counter, a 16-bit reload timer, a prescaler for generating internal count clock and control registers.

Internal clock can be selected from 3 types of internal clocks (divided by 2/8/32 of machine clock).

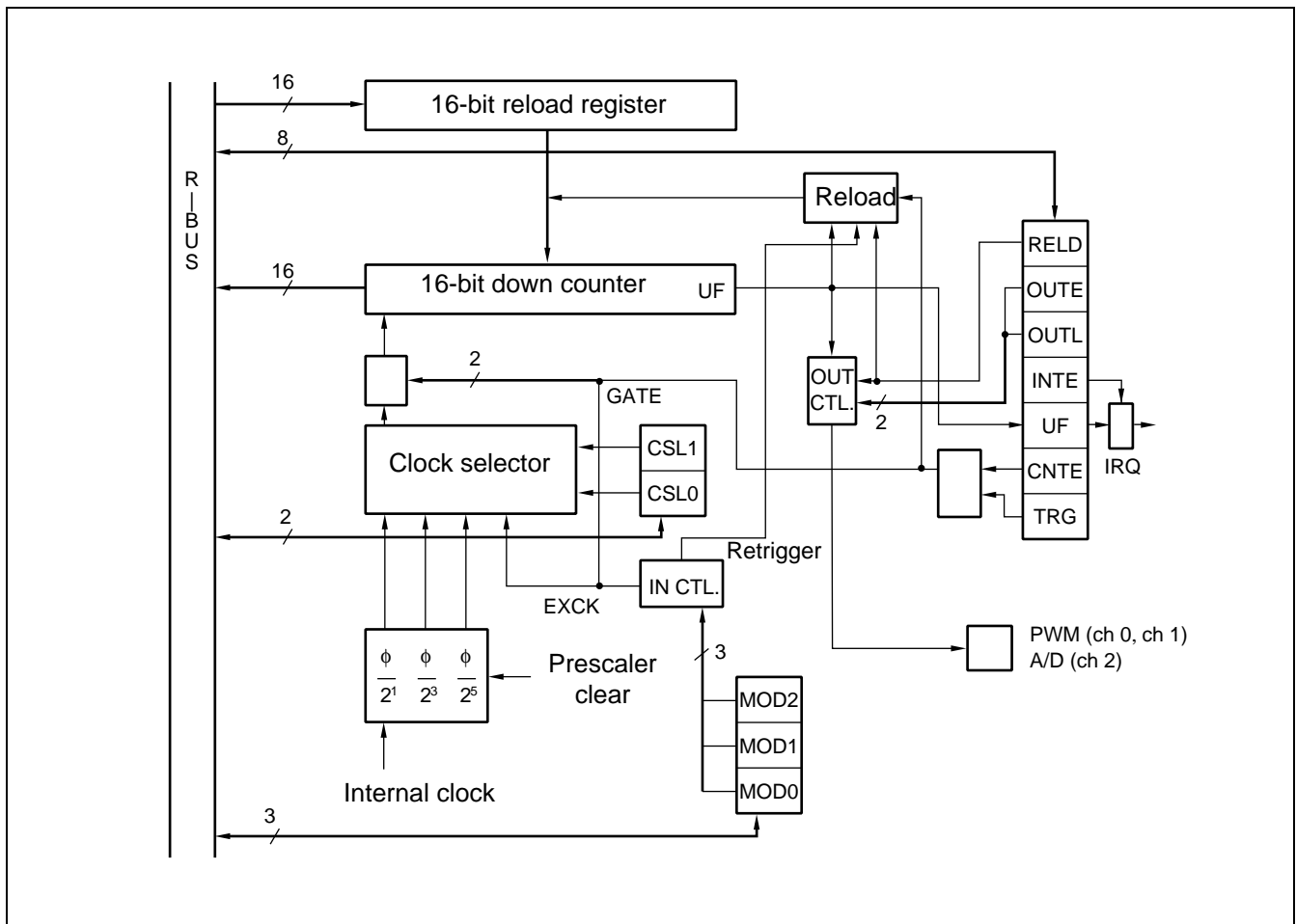
The DMA transfer can be started by the interruption.

The MB91107 consists of 3 channels of the 16-bit reload timer.

(1) Register configuration

•Control status register					
Address	bit 15	bit 0	Initial value	Access	
TMCSR0 : 00002EH	TMCSR0 to TMCSR2		---0000 _B	R/W	
TMCSR1 : 000036H			00000000 _B		
TMCSR2 : 000042H					
•16-bit timer register					
Address	bit 15	bit 0	Initial value	Access	
TMR0 : 00002AH	TMR0 to TMR2		XXXXXXXX _B	R	
TMR1 : 000032H			XXXXXXXX _B		
TMR2 : 00003EH					
•16-bit reload register					
Address	bit 15	bit 0	Initial value	Access	
TMRLR0 : 000028H	TMRLR0 to TMRLR2		XXXXXXXX _B	W	
TMRLR1 : 000030H			XXXXXXXX _B		
TMRLR2 : 00003CH					
R/W : Readable and writable - : Unused R : Read only X : Indeterminate W : Write only					

(2) Block diagram



7. Bit Search Module

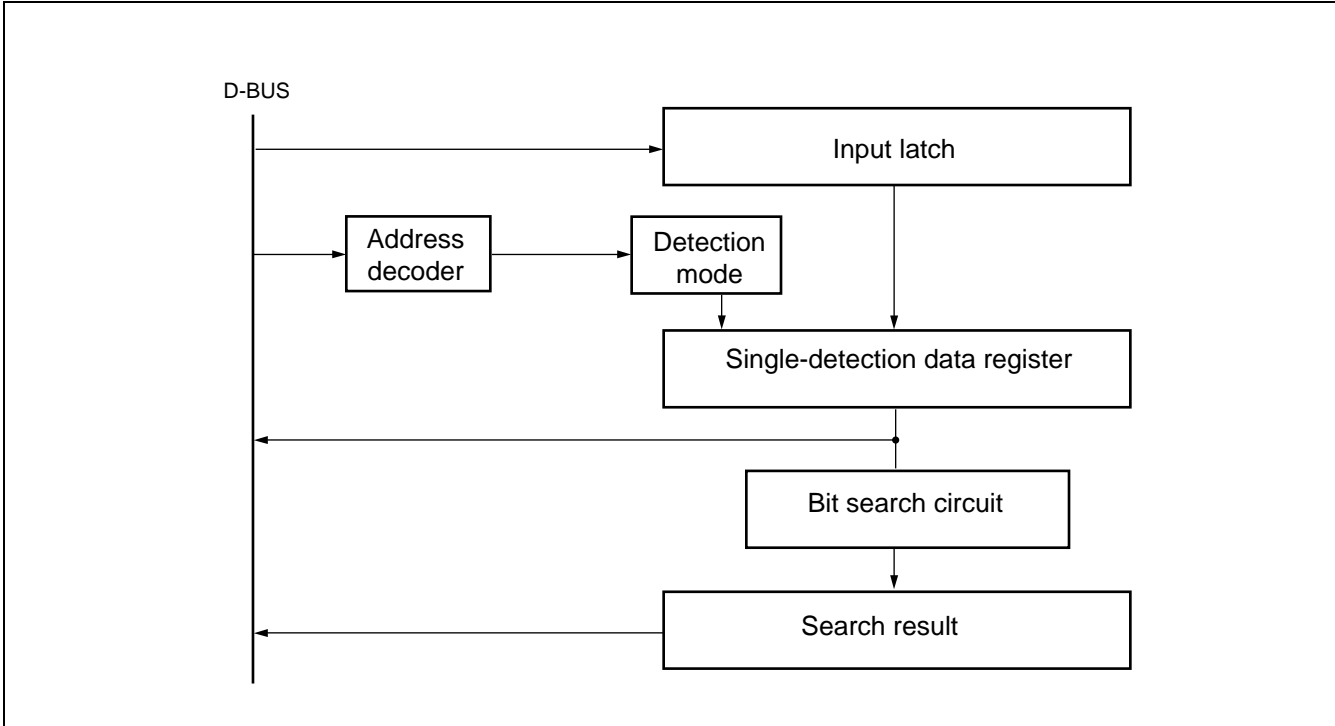
The bit search module detects transitions of data (0 to 1/1 to 0) on the data written on the input registers and returns locations of the transitions.

(1) Register configuration

Address	bit 31 bit 0	Initial value	Access
0003F0 _H	BSD0	XXXXXXXXXXXXXXXXXX _B XXXXXXXXXXXXXXXXXX _B	W Zero-detection data register
0003F4 _H	BSD1	XXXXXXXXXXXXXXXXXX _B XXXXXXXXXXXXXXXXXX _B	R/W Single-detection data register
0003F8 _H	BSDC	XXXXXXXXXXXXXXXXXX _B XXXXXXXXXXXXXXXXXX _B	W Detection data register
0003FC _H	BSRR	XXXXXXXXXXXXXXXXXX _B XXXXXXXXXXXXXXXXXX _B	R Search result register

R/W : Readable and writable
 R : Read only
 W : Write only
 X : Indeterminate

(2) Block diagram



8. A/D Converter (Successive Approximation Conversion Type)

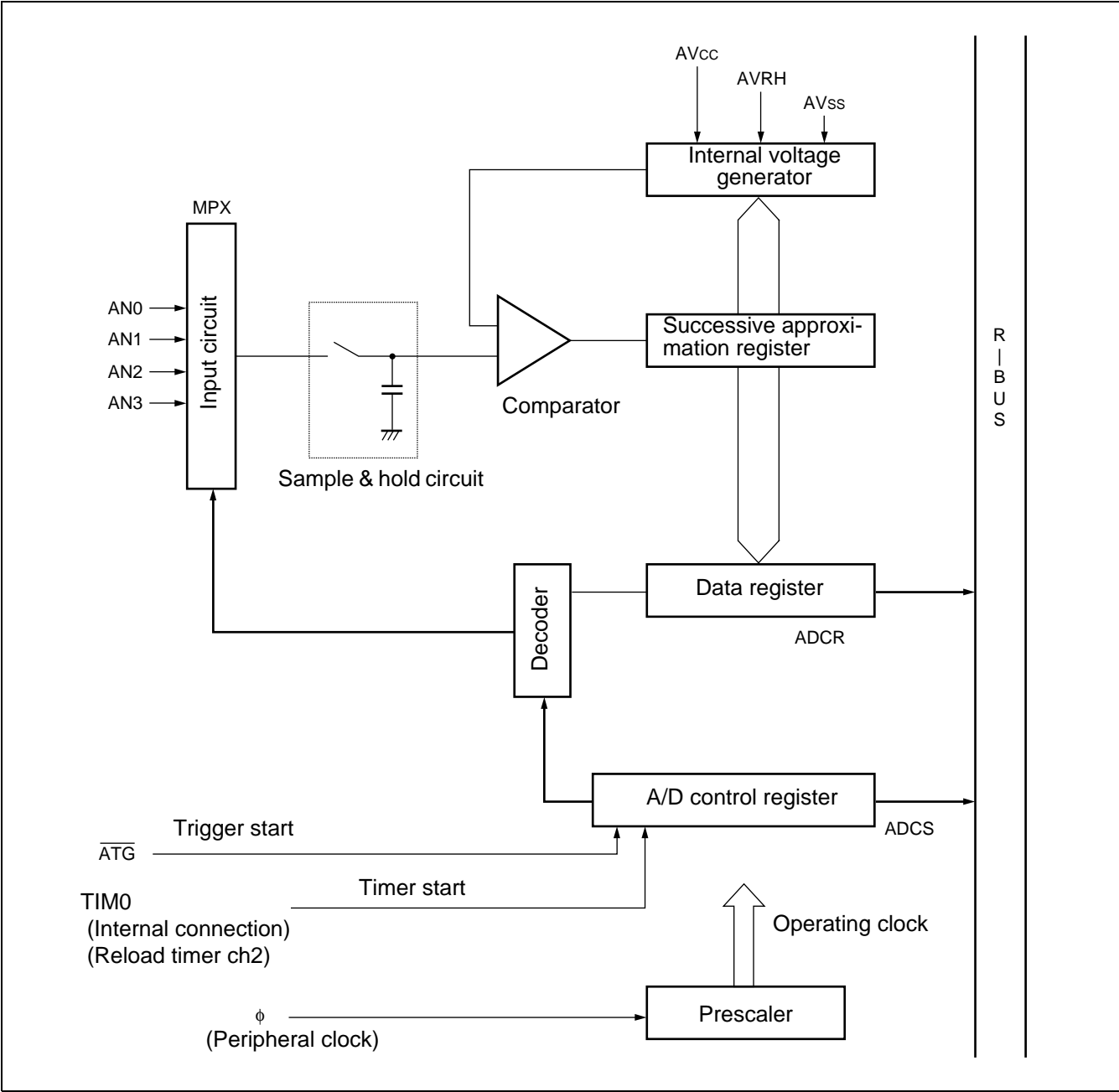
The A/D converter is the module which converts an analog input voltage to a digital value, and it has following features.

- Minimum converting time: 5.6 μ s/ch. (system clock: 25 MHz)
- Inner sample and hold circuit
- Resolution: 10 bits
- Analog input can be selected from 4 channels by program.
 - Single convert mode: 1 channel is selected and converted.
 - Scan convert mode: Converting continuous channels. Maximum 4 channels are programmable.
 - Continuous convert mode: Converting the specified channel repeatedly.
 - Stop convert mode: After converting one channel then stop and wait till next activation synchronising at the beginning of conversion can be performed.
- DMA transfer operation is available by interruption.
- Operating factor can be selected from the software, the external trigger (falling edge), and 16-bit reload timer (rising edge).

(1) Register configuration

•A/D converter control register					
Address	bit 15	bit 0	Initial value	Access	
00003AH	ADCS		00000000 _B 00000000 _B	R/W	
•A/D converter data register					
Address	bit 15	bit 0	Initial value	Access	
000038H	ADCR		-----XX _B XXXXXXXX _B	R	
R/W : Readable and writable R : Read only X : Indeterminate					

(2) Block diagram



9. Interrupt Controller

The interrupt controller processes interrupt acknowledgments and arbitration between interrupts.

•Hardware configuration

This module consists of the following components:

- ICR register
- Interrupt priority evaluation circuit
- Interrupt level/interrupt number (vector) generator
- HOLD request cancel request generator

•Main Features

The major functions of this module are listed below:

- NMI request/interrupt request detection
- Priority evaluation (interrupt level and number)
- Transfer of interrupt level as evaluation factor (to the CPU)
- Transfer of interrupt number as evaluation factor (to the CPU)
- Instruction of returning from the stop mode by NMI/interrupt generation
- Generating a request to cancel the HOLD request to the bus master

(1) Register configuration

•Interrupt control register 0 to 47

Address	bit 7	bit 0	Initial value	Access	Address	bit 7	bit 0	Initial value	Access
000400H	ICR00		--- 11111B	R/W	000419H	ICR25		--- 11111B	R/W
000401H	ICR01		--- 11111B	R/W	00041AH	ICR26		--- 11111B	R/W
000402H	ICR02		--- 11111B	R/W	00041BH	ICR27		--- 11111B	R/W
000403H	ICR03		--- 11111B	R/W	00041CH	ICR28		--- 11111B	R/W
000404H	ICR04		--- 11111B	R/W	00041DH	ICR29		--- 11111B	R/W
000405H	ICR05		--- 11111B	R/W	00041EH	ICR30		--- 11111B	R/W
000406H	ICR06		--- 11111B	R/W	00041FH	ICR31		--- 11111B	R/W
000407H	ICR07		--- 11111B	R/W	000420H	ICR32		--- 11111B	R/W
000408H	ICR08		--- 11111B	R/W	000421H	ICR33		--- 11111B	R/W
000409H	ICR09		--- 11111B	R/W	000422H	ICR34		--- 11111B	R/W
00040AH	ICR10		--- 11111B	R/W	000423H	ICR35		--- 11111B	R/W
00040BH	ICR11		--- 11111B	R/W	000424H	ICR36		--- 11111B	R/W
00040CH	ICR12		--- 11111B	R/W	000425H	ICR37		--- 11111B	R/W
00040DH	ICR13		--- 11111B	R/W	000426H	ICR38		--- 11111B	R/W
00040EH	ICR14		--- 11111B	R/W	000427H	ICR39		--- 11111B	R/W
00040FH	ICR15		--- 11111B	R/W	000428H	ICR40		--- 11111B	R/W
000410H	ICR16		--- 11111B	R/W	000429H	ICR41		--- 11111B	R/W
000411H	ICR17		--- 11111B	R/W	00042AH	ICR42		--- 11111B	R/W
000412H	ICR18		--- 11111B	R/W	00042BH	ICR43		--- 11111B	R/W
000413H	ICR19		--- 11111B	R/W	00042CH	ICR44		--- 11111B	R/W
000414H	ICR20		--- 11111B	R/W	00042DH	ICR45		--- 11111B	R/W
000415H	ICR21		--- 11111B	R/W	00042EH	ICR46		--- 11111B	R/W
000416H	ICR22		--- 11111B	R/W	00042FH	ICR47		--- 11111B	R/W
000417H	ICR23		--- 11111B	R/W					
000418H	ICR24		--- 11111B	R/W					

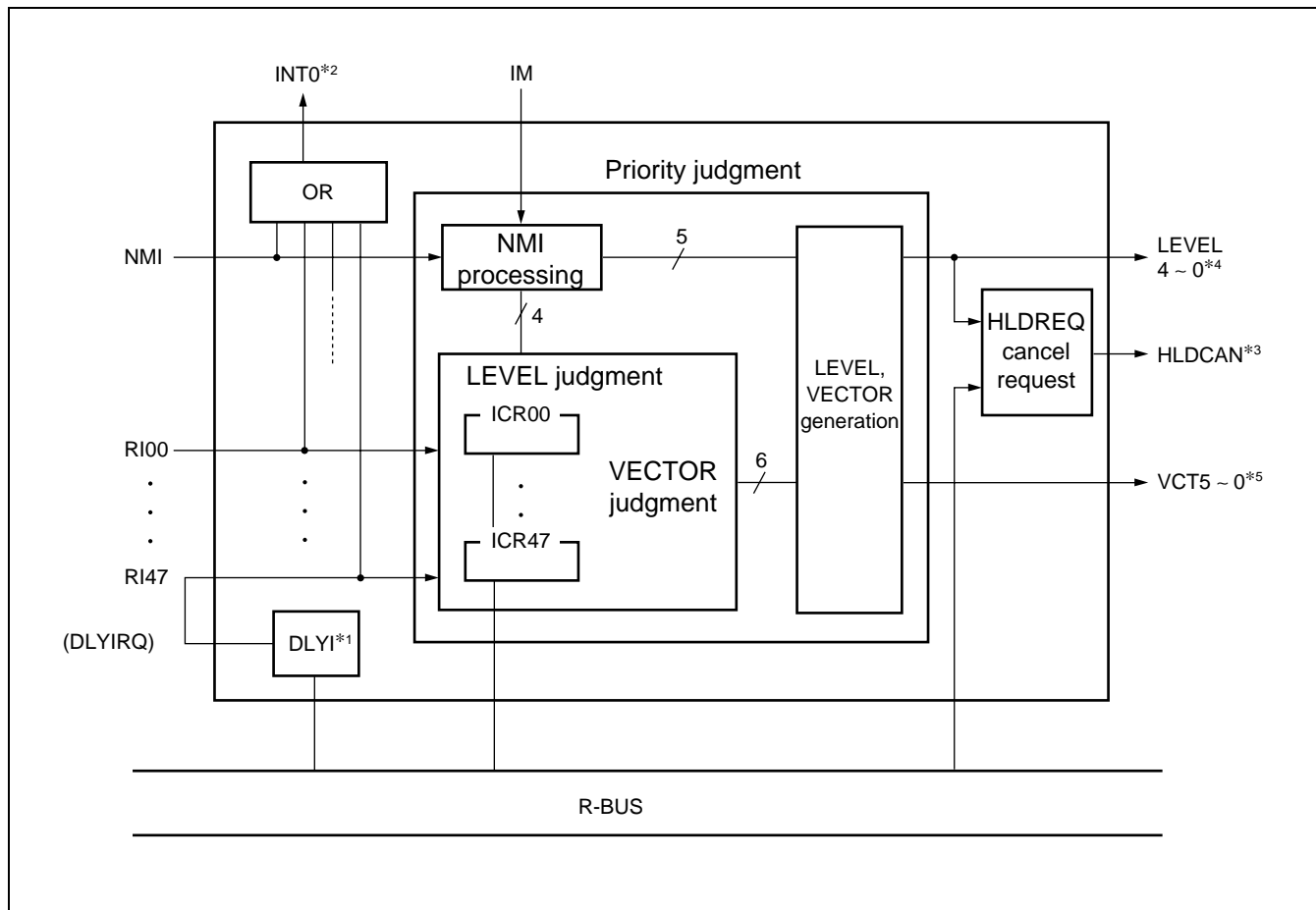
•Request level register for canceling hold request

Address	bit 7	bit 0	Initial value	Access
00000431H	HRCL		--- 11111B	R/W

R/W : Readable and writable

- : Unused

(2) Block diagram



*1 : DLY I stands for delayed interrupt module (delayed interrupt generation block) (refer to the section "11. Delayed Interrupt Module" for detail).

*2 : $INT0$ is a wake-up signal to clock control block in the sleep or stop status.

*3 : $HLDCAN$ is a bus release request signal for bus masters other than CPU.

*4 : LEVEL 4 to LEVEL 0 are interrupt level outputs.

*5 : $VCT5$ to $VCT0$ are interrupt vector outputs.

10. External Interrupt/NMI Control Block

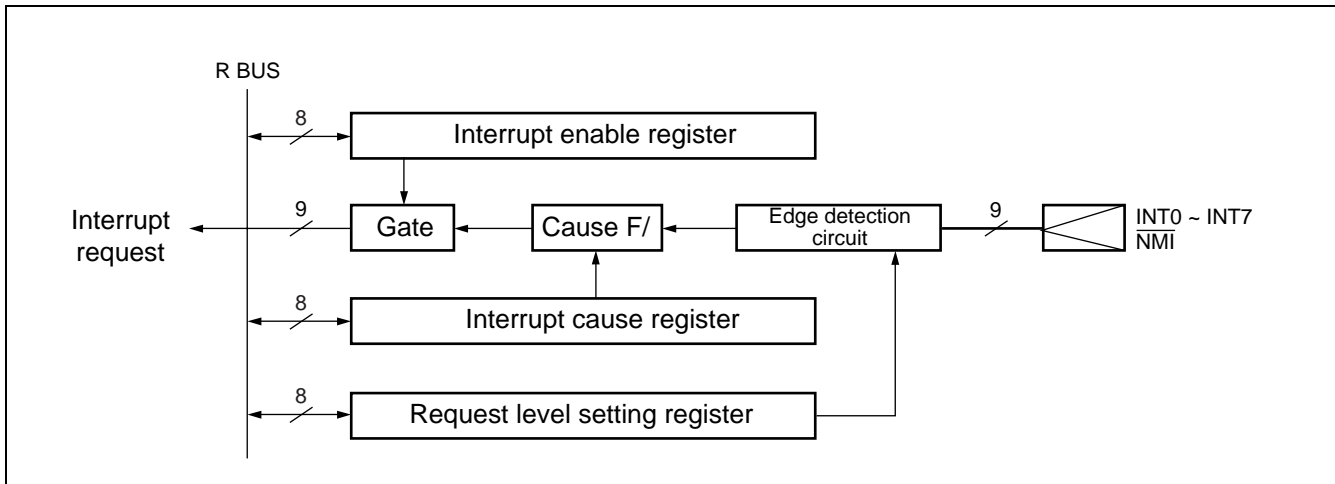
The external interrupt/NMI control block controls external interrupt request signals input to $\overline{\text{NMI}}$ pin and INT0 to INT7 pins.

Detecting levels can be selected from "H", "L", rising edge and falling edge (not for $\overline{\text{NMI}}$ pin).

(1) Register configuration

•Interrupt enable register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
000095 _H	EIRR	ENIR			00000000 _B	R/W
•External interrupt cause register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
000094 _H	EIRR	ENIR			00000000 _B	R/W
•Request level setting register						
Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
000099 _H	EIRR	ENIR			00000000 _B	R/W

(2) Block diagram



11. Delayed Interrupt Module

Delayed interrupt module is a module which generates a interrupt for changing a task. By using this delayed interrupt module, an interrupt request to CPU can be generated/cancelled by the software.
Refer to the section "9. Interrupt Controller" for delayed interrupt module block diagram.

•Register configuration

•Delayed interrupt control register				
Address	bit 7	bit 0	Initial value	Access
000430H	DICR		----- 0 _B	R/W
	R/W : Readable and writable			
	- : Unused			

12. Clock Generation (Low-power consumption mechanism)

The clock control block is a module which undertakes the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and cause hold
- Standby function (including hardware standby)
- DMA request prohibit
- PLL (multiplier circuit) embedded

(1) Register configuration

- Reset cause register/watchdog cycle control register

Address	bit 15	bit 10	bit 8	bit 0	Initial value	Access
000480 _H	RSRR		WTCR	(STCR)	1XXXX - 00 _B	R/W

- Stand-by controled register

Address	bit 15	bit 10	bit 8	bit 0	Initial value	Access
000481 _H	(RSRR/WTCR)		STCR		000111 - - _B	R/W

- DMA controlerrequest prohibit resister

Address	bit 15	bit 8	bit 0	Initial value	Access
000482 _H	PDRR		(CTBR)	- - - - 0000 _B	R/W

- Timebase timer clear resister

Address	bit 15	bit 8	bit 0	Initial value	Access
000483 _H	PDRR		(CTBR)	XXXXXXXX _B	W

- Gear control resister

Address	bit 15	bit 8	bit 0	Initial value	Access
000484 _H	GCR		(WPR)	- - - - 0000 _B	R/W

- Watchdog reset generation postpone resister

Address	bit 15	bit 8	bit 0	Initial value	Access
000485 _H	(GCR)		WPR	XXXXXXXX _B	W

- PLL control resister

Address	bit 15	bit 8	bit 0	Initial value	Access
000488 _H	PCTR		Vacancy	00 - - 0 - - - _B	W

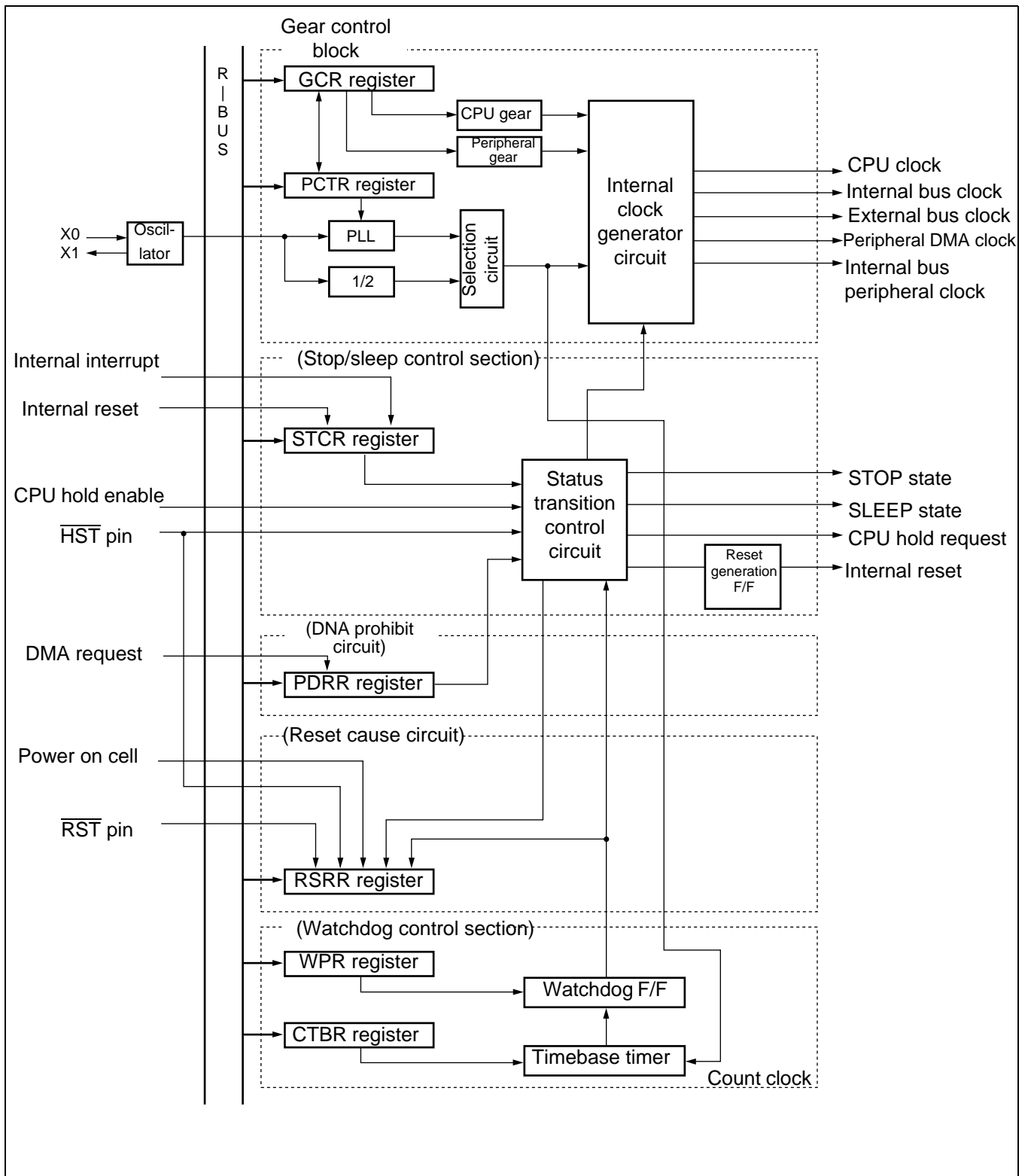
R/W : Readable and writable

W : Write only

- : Unused

X : Indeterminate

(2) Block diagram



13. External Bus Interface

The external bus interface controls the interface between the device and the external memory and also the external I/O, and has the following features.

- 25-bit (32 Mbytes) address output
- 6 independent banks owing to the chip select function.
Can be set to anywhere on the logical address space for minimum unit 64 Kbytes.
Total 32 Mbytes × 6 area setting is available by the address pin and the chip select pin.
- 8/16-bit bus width setting are available for every chip select area.
Areas 6 and 7 allow the inclusive areas to be set.
- Programmable automatic memory wait (max. for 7 cycles) can be inserted.
- DRAM interface support
- Three kinds of DRAM interface: Double CAS DRAM (normally DRAM I/F)
Single CAS DRAM
Hyper DRAM
- 2 banks independent control (RAS, CAS, etc. control signals)
- DRAM select is available from 2CAS/1WE and 1CAS/2WE.
- Hi-speed page mode supported
- CBR/self refresh supported
- Programmable wave form
- Unused address/data pin can be used for I/O port.
- Little endian mode supported
- Clock doubler: Internal bus 50 MHz, external bus 25 MHz

(1) Register configuration

•Area selection register 1 to 5					
Address	bit 15	bit 0	Initial value		Access
00060CH	ASR1		00000000 _B	00000001 _B	W
000610H	ASR2		00000000 _B	00000010 _B	W
000614H	ASR3		00000000 _B	00000011 _B	W
000618H	ASR4		00000000 _B	00000100 _B	W
00061CH	ASR5		00000000 _B	00000101 _B	W
•Area mask register 1 to 5					
Address	bit 15	bit 0	Initial value		
00060EH	AMR1		00000000 _B	00000000 _B	W
000612H	AMR2		00000000 _B	00000000 _B	W
000616H	AMR3		00000000 _B	00000000 _B	W
00061AH	AMR4		00000000 _B	00000000 _B	W
00061EH	AMR5		00000000 _B	00000000 _B	W

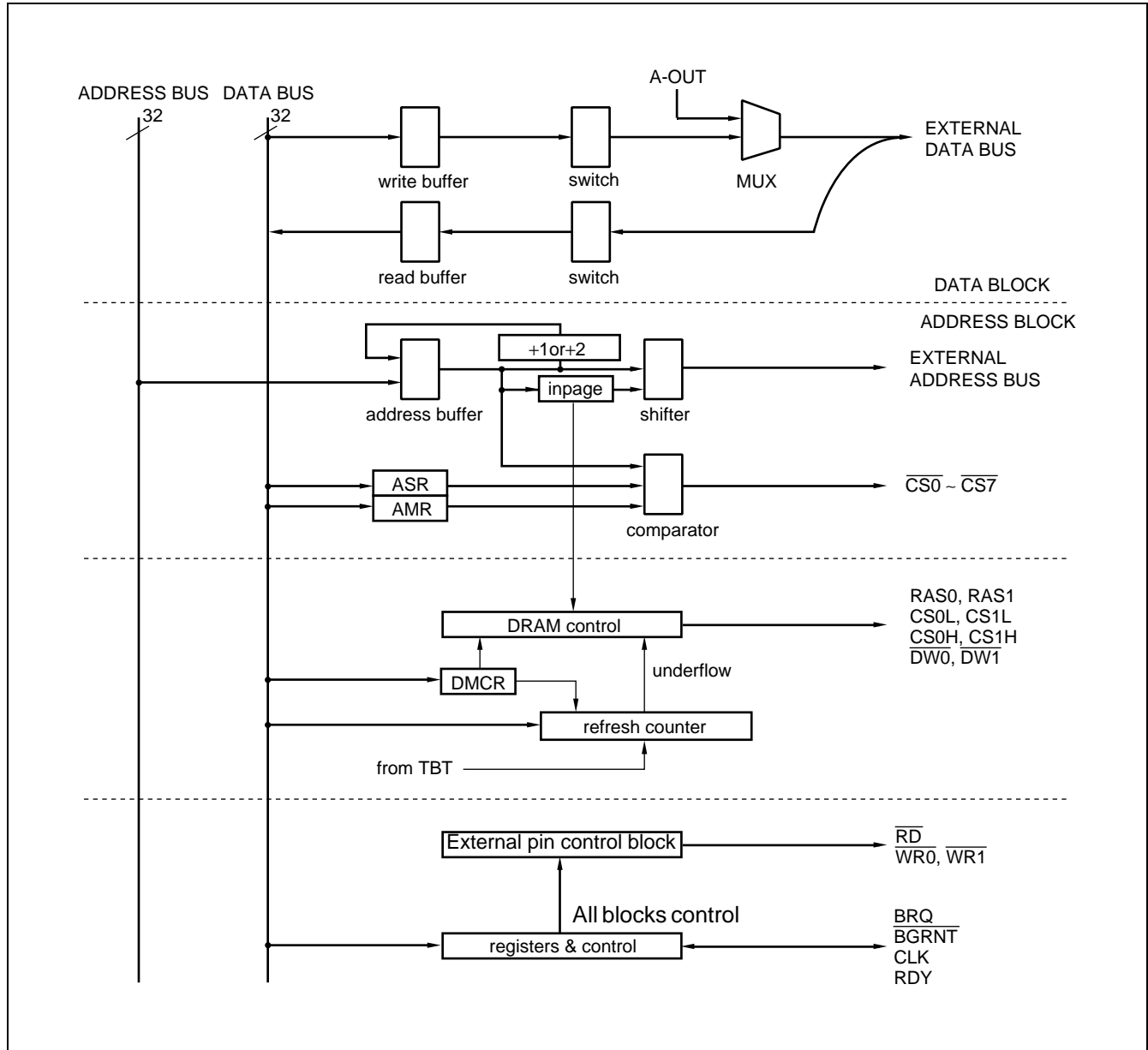
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•Area mode register 0, 1, 32, 4, 5							
	Address	bit 15	bit 8	bit 7	bit 0	Initial value	Access
AMD0	: 000620 _H	AMD0		AMD1		---00111 _B 0--00000 _B	R/W
AMD1	: 000621 _H						
AMD32	: 000622 _H	AMD32		AMD4		00000000 _B 0--00000 _B	R/W
AMD4	: 000023 _H						
AMD5	: 000624 _H	AMD5		(DSCR)		0--00000 _B	R/W
•DRAM signal control register							
	Address	bit 15	bit 8	bit 7	bit 0	Initial value	
	000625 _H	AMD5		DSCR		00000000 _B	W
•Refresh control register							
	Address	bit 15			bit 0	Initial value	
	000626 _H	RFCR				--XXXXXX _B 00---000 _B	R/W
•External pin control register							
	Address	bit 15			bit 0	Initial value	
	000628 _H	EPCR0				----1100 _B -1111111 _B	W
	00062A _H	EPCR1				-----1 _B 11111111 _B	W
•DRAM control register 4, 5							
	Address	bit 15			bit 0	Initial value	
	00062C _H	DMCR4				00000000 _B 0000000- _B	R/W
	00062E _H	DMCR5				00000000 _B 0000000- _B	R/W
•Little endian register							
	Address	bit 15	bit 8	bit 7	bit 0	Initial value	
	0007FE _H	LER		(MODR)		-----000 _B	W
•Mode register							
	Address	bit 15	bit 8	bit 7	bit 0	Initial value	
	0007FF _H	(MODR)		LER		XXXXXXXX _B	W
		R/W : Readable and writable					
		W : Write only					
		- : Unused					
		X : Indeterminate					

(2) Block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*1
Analog supply voltage	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
Analog reference voltage	AV_{RH}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	*2
Input voltage	V_I	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
Analog pin input voltage	V_{IA}	$V_{SS} - 0.3$	$AV_{CC} + 0.3$	V	
Output voltage	V_O	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	-10	mA	*3
“H” level average output current	I_{OHAV}	—	-4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	-50	mA	
“H” level total average output current	ΣI_{OHAV}	—	-20	mA	*5
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	0	+70	°C	
Storage temperature	T_{stg}	-55	+150	°C	

*1 : V_{CC} must not be less than $V_{SS} - 0.3\text{ V}$.

*2 : Care must be taken that AV_{CC} and AV_{RH} do not exceed $V_{CC} + 0.3\text{ V}$, such as when turning on the device. Also, care must be taken that AV_{RH} does not exceed AV_{CC} .

*3 : Maximum output current is a peak current value measured at a corresponding pin.

*4 : Average output current is an average current for a 100 ms period at a corresponding pin.

*5 : Average total output current is an average current for a 100 ms period for all corresponding pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($AV_{SS} = V_{SS} = 0.0\text{ V}$)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	3.6	V	Normal operation
	V_{CC}	3.0	3.6		Retaining the RAM state in stop mode
Analog supply voltage	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 3.6$	V	
Analog reference voltage	AV_{RH}	AV_{SS}	AV_{CC}	V	
Operating temperature	T_A	0	+70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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3. DC Characteristics

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	Input pin except for hysteresis input	—	$0.7 \times V_{CC}$	—	$V_{CC} + 0.3$	V	
"L" level input voltage	V_{IHS}	*1		$0.8 \times V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	V_{IL}	Input pin except for hysteresis input		$V_{SS} - 0.3$	—	$0.25 \times V_{CC}$	V	
	V_{ILS}	*1		$V_{SS} - 0.3$	—	$0.2 \times V_{CC}$	V	Hysteresis input
"H" level output voltage	V_{OH}	All output pins	$V_{CC} = 3.0\text{ V}$ $I_{OH} = -4.0\text{ mA}$	$V_{CC} - 0.5$	—	—	V	
"L" level output voltage	V_{OL}	All output pins	$V_{CC} = 3.0\text{ V}$ $I_{OL} = 8.0\text{ mA}$	—	—	0.4	V	
Input leak current (Hi-Z Output leak current)	I_{LI}	All output pins	$V_{CC} = 3.6\text{ V}$ $0.45\text{ V} < V_I < V_{CC}$	-5	—	+5	μA	
Pull-up resistance	R_{PULL}	$\overline{\text{RST}}$	$V_{CC} = 3.6\text{ V}$ $V_I = 0.45\text{ V}$	12	25	100	$\text{k}\Omega$	
Pull-down resistance	R_{DOWN}	BRQ	$V_{CC} = 3.6\text{ V}$ $V_I = 3.3\text{ V}$	12	25	100	$\text{k}\Omega$	
Power supply current*2	I_{CC}	V_{CC}	$F_C = 12.5\text{ MHz}$ $V_{CC} = 3.3\text{ V}$	—	80	150	mA	(Four multiplication) Operation at 50 MHz
	I_{CCS}		$F_C = 12.5\text{ MHz}$ $V_{CC} = 3.3\text{ V}$	—	40	120	mA	Sleep mode
	I_{CCH}		$T_A = +25\text{ }^\circ\text{C}$ $V_{CC} = 3.3\text{ V}$	—	5	—	μA	Stop mode
Input capacitance	C_{IN}	Except for V_{CC} , AV_{CC} , AV_{SS} , V_{SS}	—	—	10	—	pF	

*1 : Hysteresis input pin : $\overline{\text{NMI}}$, $\overline{\text{RST}}$, P40 to P47, P50 to P57, P60 to P67, P70, P81, P85, PA1 to PA6, PB0 to PB7, PE0 to PE7, PF0 to PF7, PG0 to PG7, PH0 to PH7, PI0, PI1

*2 : The MB91V107 (development model) has larger supply current than the production models because it contains an development tool interface circuit.

4. AC Characteristics

•Measurement Conditions

The following conditions applies to measurement items unless otherwise specified.

•AC characteristics measurement conditions

V_{IH}	$1 / 2 \times V_{CC}$	V_{OH}	$1 / 2 \times V_{CC}$
V_{IL}	$1 / 2 \times V_{CC}$	V_{OL}	$1 / 2 \times V_{CC}$

$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$

Note: The rise/fall time of input is 10 ns or less.

•Load conditions

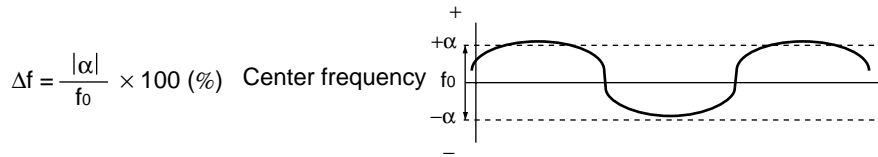
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(1) Clock Timings

(V_{CC} = 3.0 V to 3.6 V, AV_{SS} = V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

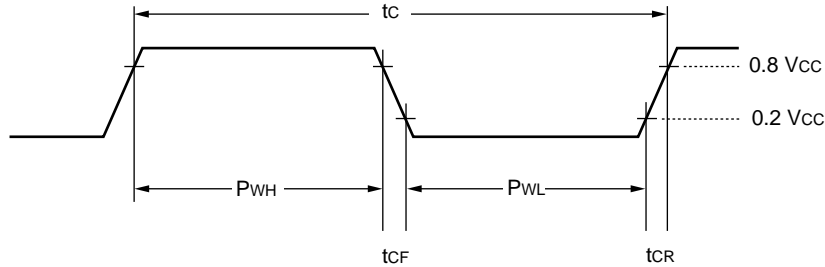
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency (1)	F _c	X0 X1	—	12.5	12.5	MHz	Self-oscillation 12.5 MHz Internal operation at 50 MHz (Using PLL, 4 multiplication)
Clock cycle time	t _c	X0 X1		—	80	ns	
Frequency shift ratio *1 (when locked)	Δf	—		—	5	%	
Clock frequency (2)	F _c	X0 X1	—	10	25	MHz	Self-oscillation (divide-by-2 input)
Clock frequency (3)	F _c	X0 X1		10	25	MHz	External clock (divide-by-2 input)
Clock cycle time	t _c	X0 X1		40	100	ns	
Input clock pulse width	P _{WH} P _{WL}	X0 X1	12.5 to 25 MHz	20	—	ns	Input to X0, X1
	P _{WH}	X0	Less than 12.5 MHz	25	—	ns	Input to X0 only
Input clock rising/falling time	t _{CR} t _{CF}	X0 X1	—	—	8	ns	(t _{CR} + t _{CF})
	Internal operating clock frequency	f _{CP}	—	—	0.625 × 2	50	MHz
f _{CPP}		—	0.625 × 2		25	MHz	Peripheral system
Internal operating clock cycle time	t _{CP}	—	—	20	1600*2	ns	CPU system
	t _{CPP}	—		40	1600*2	ns	Peripheral system

*1 : Frequency shift ratio stands for deviation ratio of the operating clock from the center frequency in the clock multiplication system.

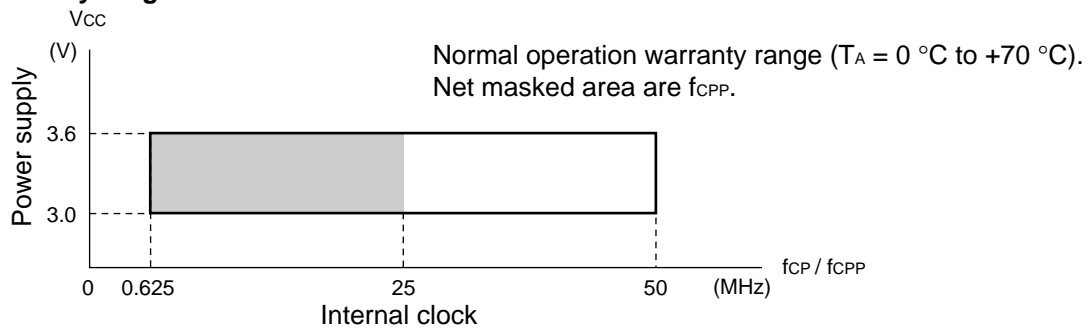


*2 : These values are for a minimum clock of 10 MHz input to X0, a divide-by-2 system of the source oscillation and a 1/8 gear.

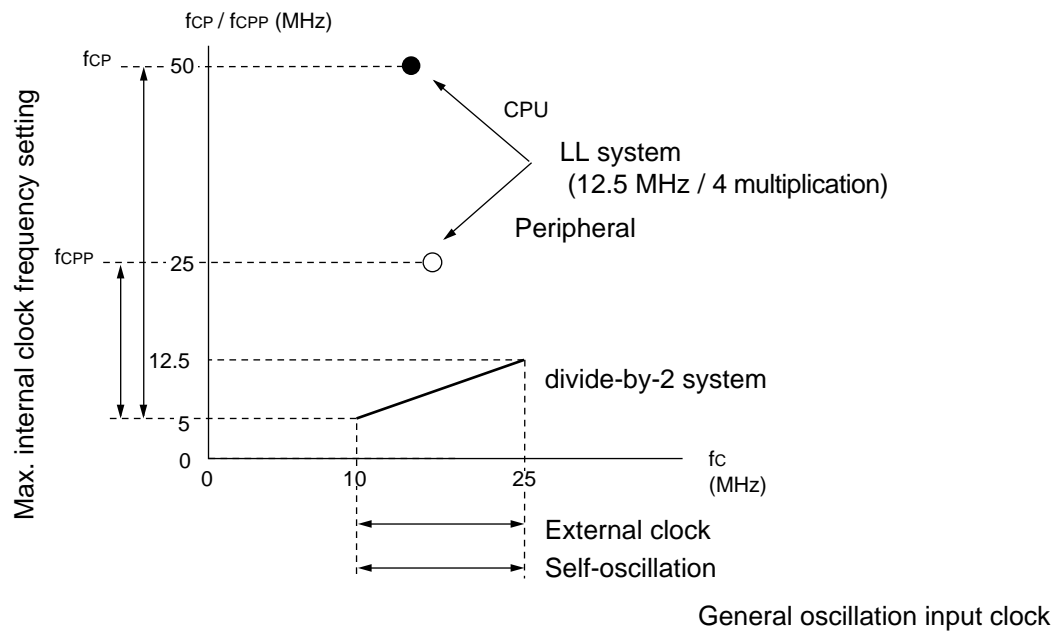
• Clock timing rating measurement conditions



• Operation warranty range



• External / internal clock setting range

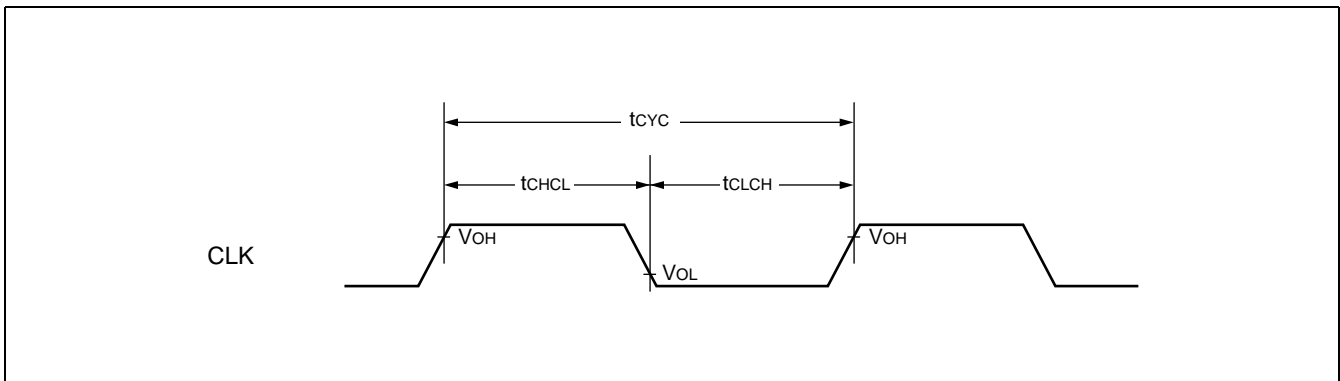


- Note:
- When using PLL, the external clock must be used need 12.5 MHz.
 - PLL oscillation stabilizing period $> 100\text{ }\mu\text{s}$
 - The setting of internal clock must be within above ranges.

(2) Clock Output Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Cycle time	t_{CYC}	CLK	—	t_{CP}	—	ns	*1
				$2 \times t_{CP}$	—		Using the doubler
CLK \uparrow →CLK \downarrow	t_{CHCL}	CLK	—	$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*2
CLK \downarrow →CLK \uparrow	t_{CLCH}	CLK	—	$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*3



*1 : t_{CYC} is a frequency for 1 clock cycle including a gear cycle.

*2 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min. : } (1 - n/2) \times t_{CYC} - 10$$

$$\text{Max. : } (1 - n/2) \times t_{CYC} + 10$$

Select a gear cycle of $\times 1$ when using the doubler.

*3 : Rating at a gear cycle of $\times 1$.

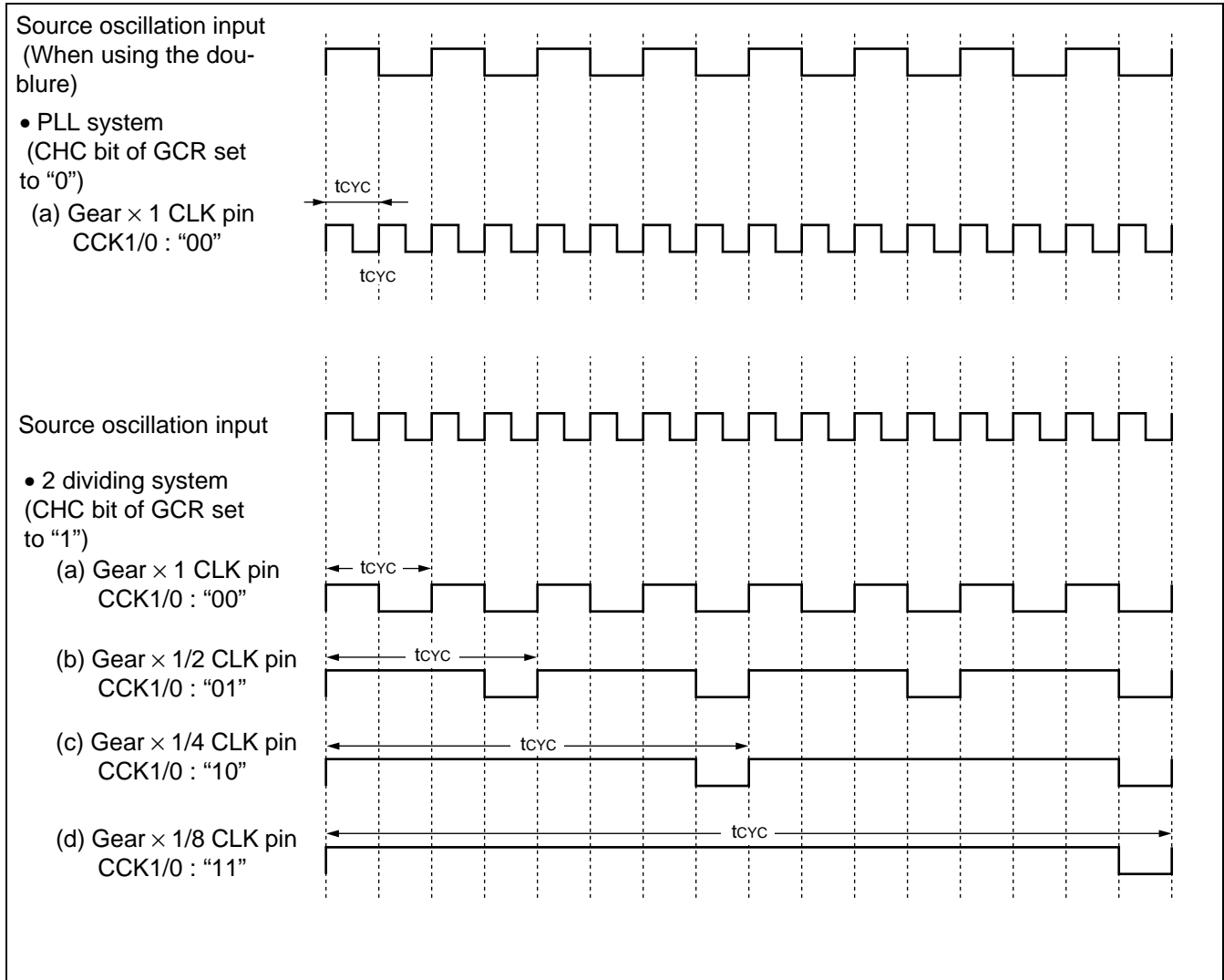
When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute "n" in the following equations with 1/2, 1/4, 1/8, respectively.

$$\text{Min.: } n/2 \times t_{CYC} - 10$$

$$\text{Max.: } n/2 \times t_{CYC} + 10$$

Select a gear cycle of $\times 1$ when using the doubler.

The relation between source oscillation input and CLK pin for configured by CHC/CCK1/CCK0 settings of GCR (gear control register) is as follows. However, in this chart source oscillation input means X0 input clock.

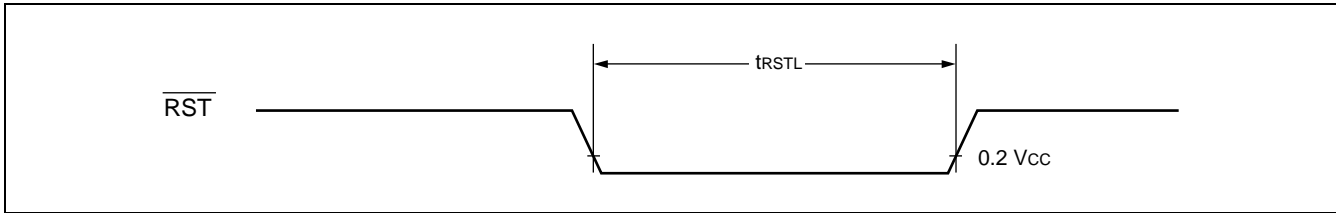


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(3) Reset Input Ratings

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $A V_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

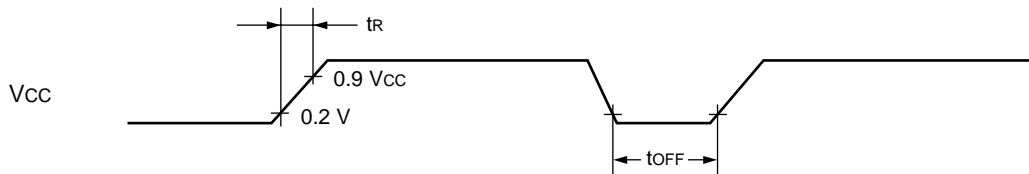
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	\overline{RST}	—	$t_{CP} \times 5$	—	ns	



(4) Power-on Reset

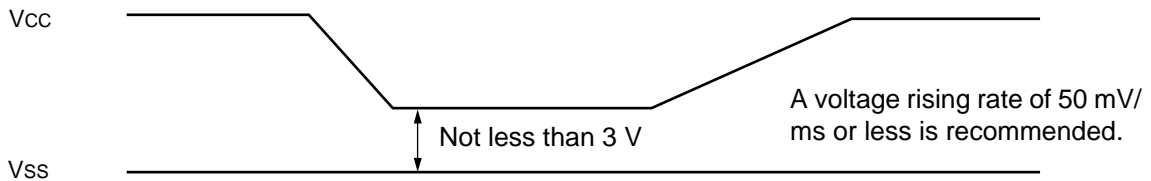
($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rising time	t_R	V_{CC}	$V_{CC} = 3.3\text{ V}$	—	18	ms	$V_{CC} < 0.2\text{ V}$ before the power supply rising
Power supply shut off time	t_{OFF}	V_{CC}	—	1	—	ms	Repeated operations

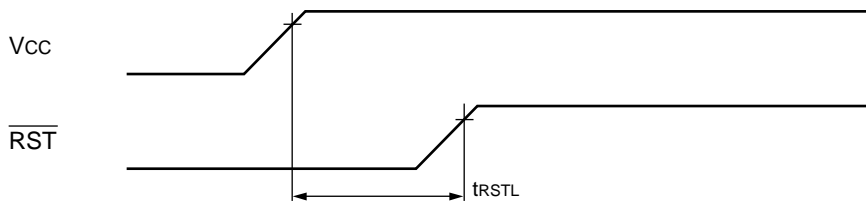


•Notes

1) Sudden change in supply voltage during operation may initiate a power-on sequence. To change supply voltage during operation, it is recommended to smoothly raise the voltage to avoid rapid fluctuations in the supply voltage.



2) Set \overline{RST} pin to "L" level when turning on the device, at least the t_{RSTL} duration after the supply voltage reaches V_{CC} is necessary before turning the \overline{RST} to "H" level.



3) If the supply voltage goes below the lower limit of the guaranteed operating voltage range, be sure to restart the power supply from the V_{SS} level. This is because an internal power-on reset must be generated to restart operation without allowing the internal circuit to run out of control. The guaranteed operating voltage range of MB91107 is from 3.0 to 3.6 V.

(5) Normal Bus Access Read/write Operation

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$)

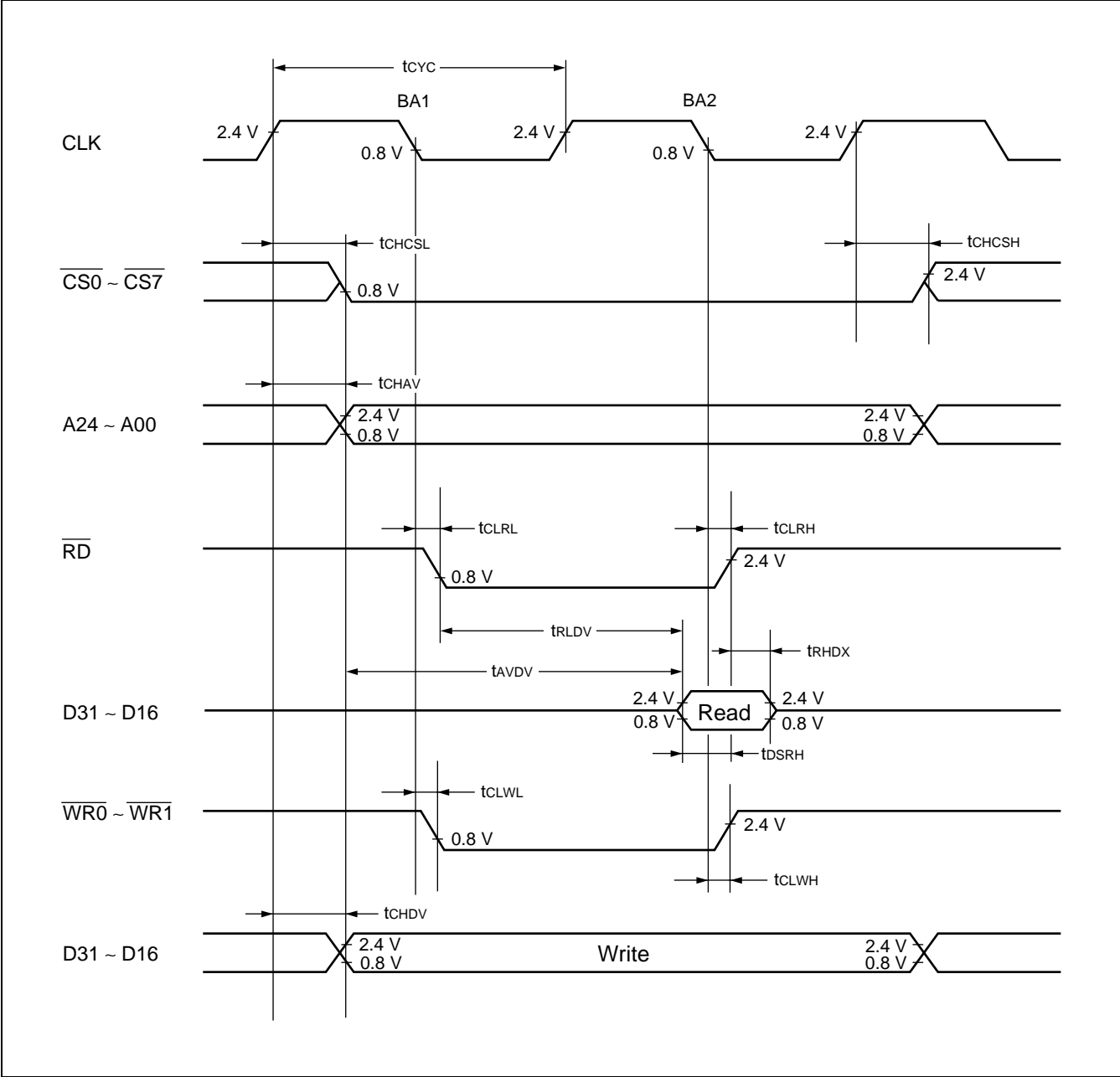
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
$\overline{CS0}$ to $\overline{CS7}$ delay time	t_{CHCSL}	CLK	—	—	15	ns	
$\overline{CS0}$ to $\overline{CS7}$ delay time	t_{CHCSH}	$\overline{CS0}$ to $\overline{CS7}$		—	15	ns	
Address delay time	t_{CHAV}	CLK A24 to A00		—	15	ns	
Data delay time	t_{CHDV}	CLK D31 to D16		—	15	ns	
\overline{RD} delay time	$t_{CLR L}$	CLK		—	15	ns	
\overline{RD} delay time	$t_{CLR H}$	\overline{RD}		—	15	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWL}	CLK		—	15	ns	
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{CLWH}	$\overline{WR0}$ to $\overline{WR1}$		—	15	ns	
Valid address → valid data input time	t_{AVDV}	A24 to A00 D31 to D16		—	$3/2 \times t_{CYC} - 25$	ns	*1 *2
$\overline{RD} \downarrow \rightarrow$ valid data input time	t_{RLDV}	\overline{RD} D31 to D16		—	$t_{CYC} - 10$	ns	*1
Data set up → $\overline{RD} \uparrow$ time	t_{DSRH}			10	—	ns	
$\overline{RD} \uparrow \rightarrow$ data hold time	t_{RHDX}			0	—	ns	

*1: When bus timing is delayed by automatic wait insertion or RDY input, add ($t_{CYC} \times$ extended cycle number for delay) to this rating.

*2: Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

$$\text{Equation: } (2 - n/2) \times t_{CYC} - 25$$

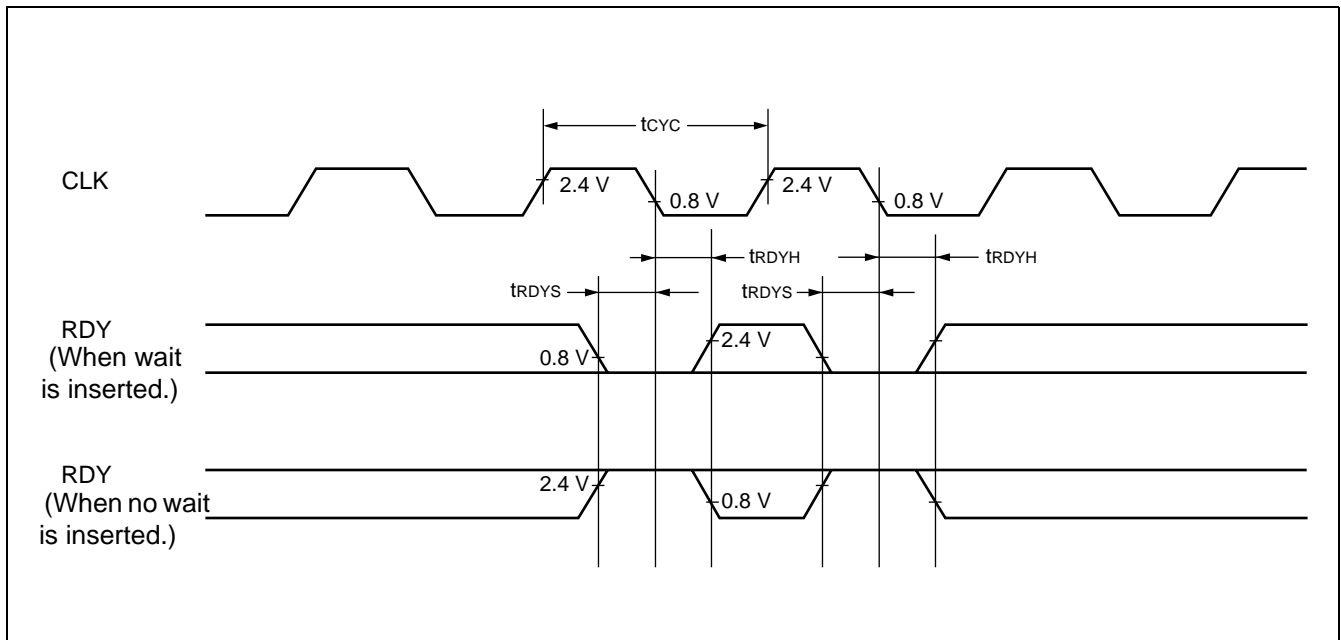


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(6) Ready Input Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RDY set up time \rightarrow CLK \downarrow	t_{RDYS}	RDY CLK	—	15	—	ns	
CLK $\downarrow \rightarrow$ RDY hold time	t_{RDYH}	CLK RDY		0	—	ns	

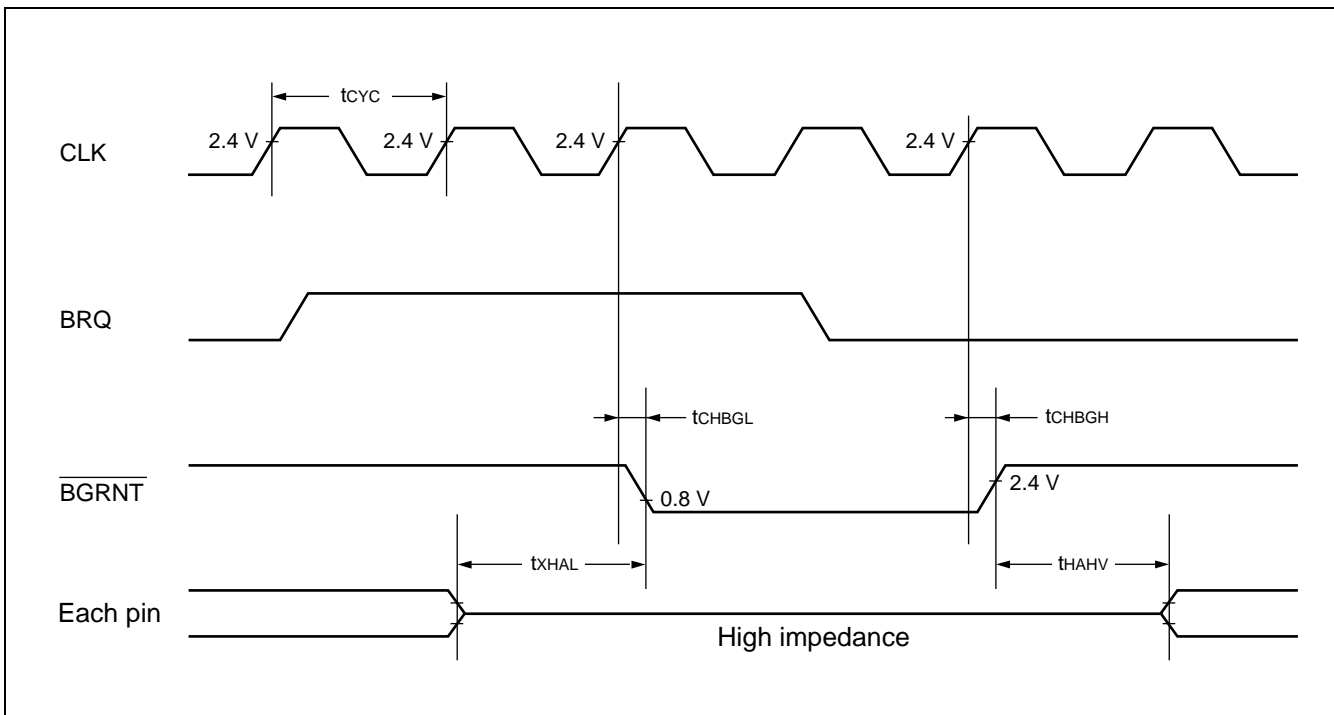


(7) Hold Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
BGRNT delay time	t_{CHBGL}	CLK BGRNT	—	—	6	ns	
BGRNT delay time	t_{CHBGH}			—	6	ns	
Pin floating \rightarrow BGRNT \downarrow time	t_{XHAL}	BGRNT	—	$t_{CYC} - 10$	$t_{CYC} + 10$	ns	
BGRNT \uparrow \rightarrow pin valid time	t_{HAHV}			$t_{CYC} - 10$	$t_{CYC} + 10$	ns	

Note : There is a delay time of more than 1 cycle from BRQ input to BGRNT change.



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(8) Normal DRAM Mode Read/Write Cycle

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

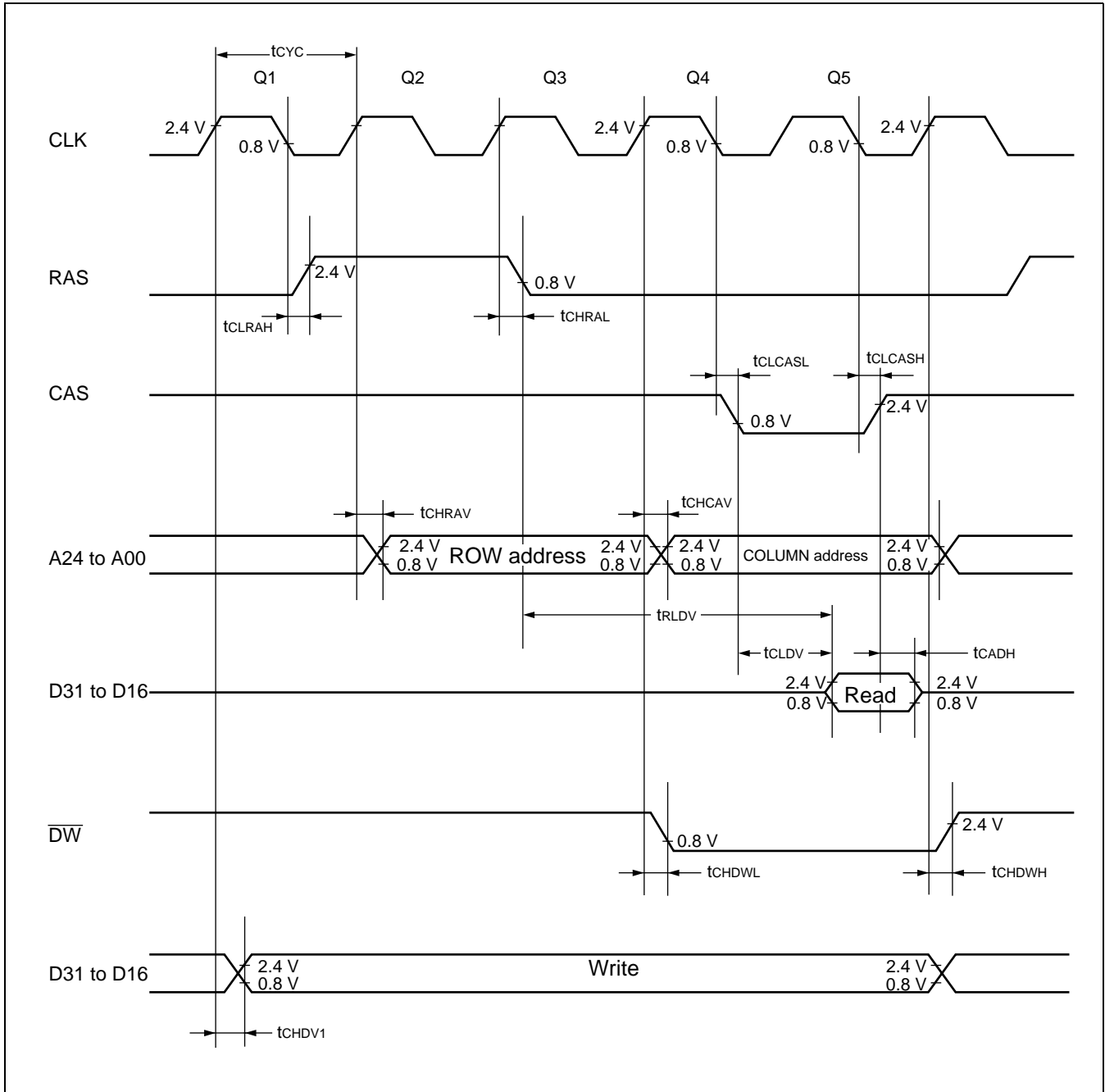
Parameter	Symbol	Pin name	Condi- tion	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	15	ns	
RAS delay time	t_{CHRAL}			—	15	ns	
CAS delay time	t_{CLCASL}	CLK CAS		—	15	ns	
CAS delay time	t_{CLCASH}			—	15	ns	
ROW address delay time	t_{CHRAV}	CLK A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV}			—	15	ns	
\overline{DW} delay time	t_{CHDWL}	CLK \overline{DW}		—	15	ns	
\overline{DW} delay time	t_{CHDWH}			—	15	ns	
Output data delay time	t_{CHDV1}	CLK D31 to D16		—	15	ns	
RAS $\downarrow \rightarrow$ valid data input time	t_{RLDV}	RAS D31 to D16		—	$5 / 2 \times t_{CYC} - 16$	ns	*1 *2
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV}	CAS		—	$t_{CYC} - 17$	ns	*1
CAS $\uparrow \rightarrow$ data hold time	t_{CADH}	D31 to D16		0	—	ns	

*1 : When Q1 cycle or Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

*2 : Rating at a gear cycle of $\times 1$.

When a gear cycle of 1/2, 1/4, 1/8 is selected, substitute “n” in the following equation with 1/2, 1/4, 1/8, respectively.

•Equation: $(3 - n/2) \times t_{CYC} - 16$



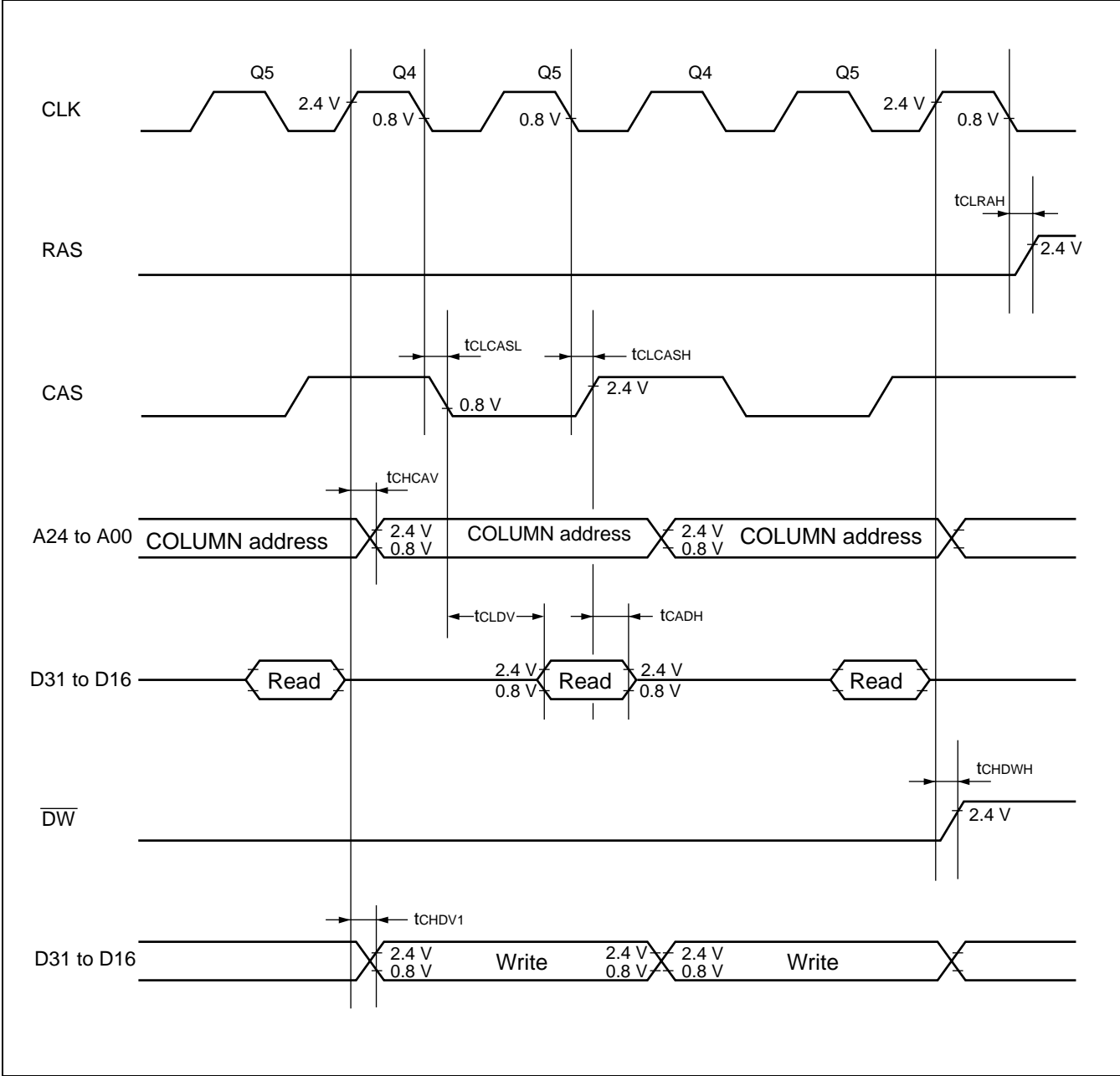
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(9) Normal DRAM Mode Fast Page Read/Write Cycle

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tion	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK, RAS	—	—	15	ns	
CAS delay time	t_{CLCASL}	CLK		—	15	ns	
CAS delay time	t_{CLCASH}	CAS		—	15	ns	
COLUMN address delay time	t_{CHCAV}	CLK A24 to A00		—	15	ns	
\overline{DW} delay time	t_{CHDWH}	CLK, \overline{DW}		—	15	ns	
Output data delay time	t_{CHDV1}	CLK D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV}	CAS		—	$t_{CYC} - 17$	ns	*
CAS $\uparrow \rightarrow$ data hold time	t_{CADH}	D31 to D16		0	—	ns	

* : When Q4 cycle is extended for 1 cycle, add t_{CYC} time to this rating.

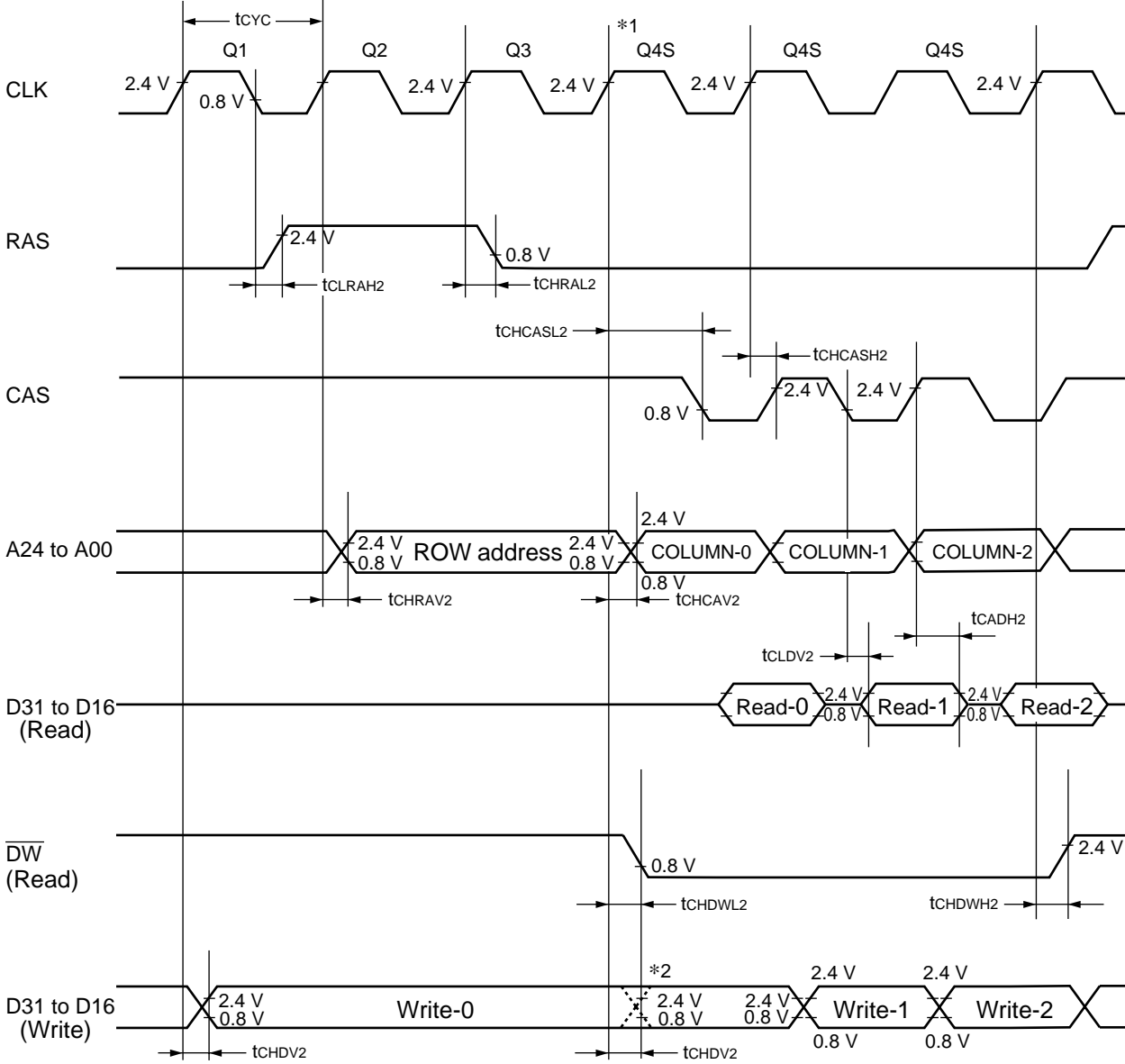


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(10) Single DRAM Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condi- tion	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH2}	CLK RAS	—	—	15	ns	
RAS delay time	t_{CHRAL2}			—	15	ns	
CAS delay time	$t_{CHCASL2}$	CLK CAS		—	$n/2 \times t_{CYC}$ + $t_{CHCASH2}$	ns	
CAS delay time	$t_{CHCASH2}$			—	15	ns	
ROW address delay time	t_{CHRAV2}	CLK A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV2}			—	15	ns	
\overline{DW} delay time	t_{CHDWL2}	CLK \overline{DW}		—	15	ns	
\overline{DW} delay time	t_{CHDWH2}			—	15	ns	
Output data delay time	t_{CHDV2}	CLK, D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ Valid data input time	t_{CLDV2}	CAS D31 to D16		—	$(1 - n/2) \times t_{CYC}$ - 17	ns	
CAS $\uparrow \rightarrow$ data hold time	t_{CADH2}		0	—	ns		



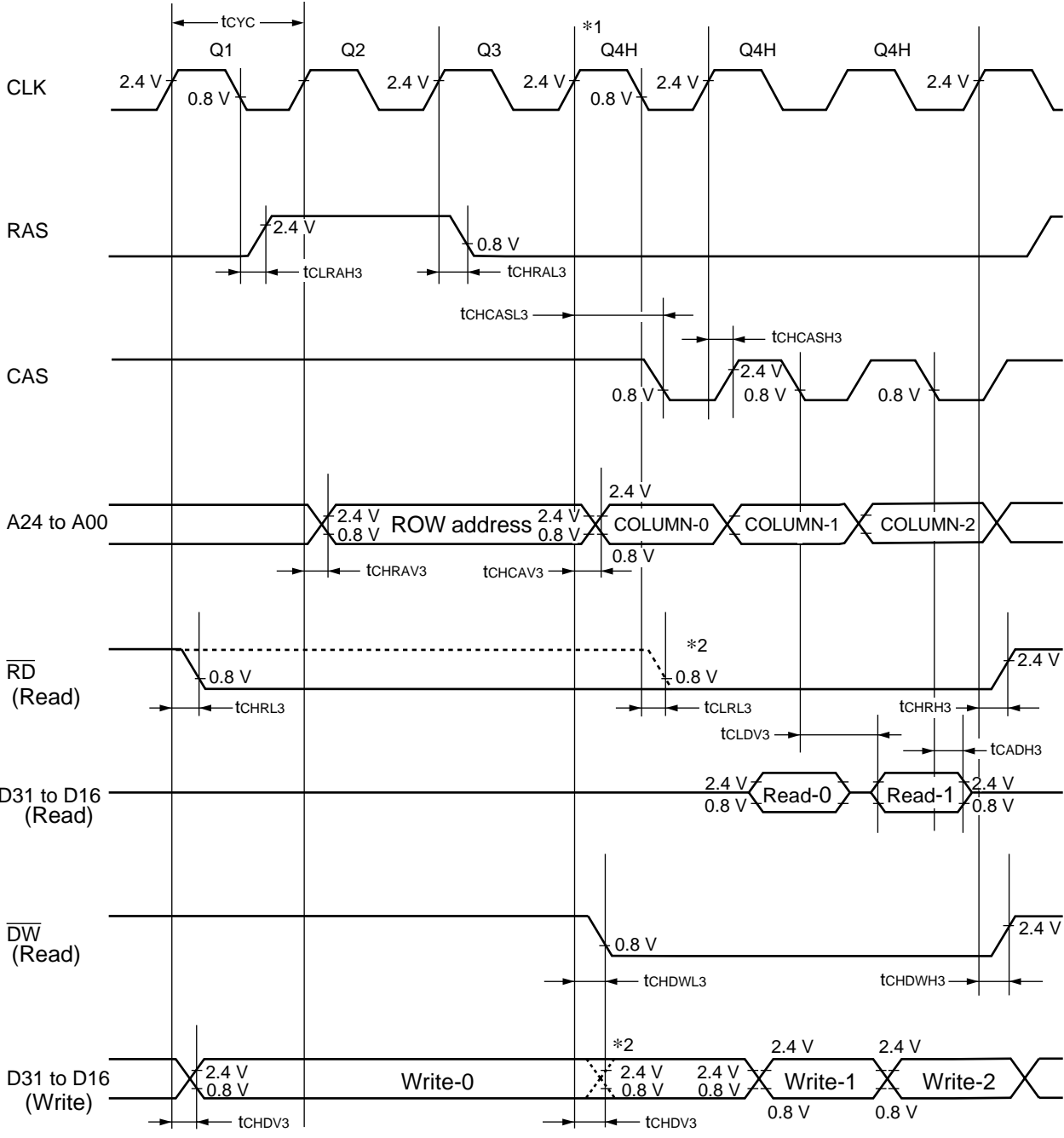
*1 : Q4S indicates Q4SR (Read) of Single DRAM cycle or Q4SW (Write) cycle.
 *2 : indicates the timing when the bus cycle begins from the high speed page mode.

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(11) Hyper DRAM Timing

($V_{CC} = 3.0\text{ V to } 3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH3}	CLK RAS	—	—	15	ns	
RAS delay time	t_{CHRAL3}			—	15	ns	
CAS delay time	$t_{CHCASL3}$	CLK CAS		—	$n / 2 \times t_{CYC}$ + $t_{CHCASH3}$	ns	
CAS delay time	$t_{CHCASH3}$			—	15	ns	
ROW address delay time	t_{CHRAV3}	CLK A24 to A00		—	15	ns	
COLUMN address delay time	t_{CHCAV3}			—	15	ns	
\overline{RD} delay time	t_{CHRL3}	CLK \overline{RD}		—	15	ns	
\overline{RD} delay time	t_{CHRH3}			—	15	ns	
\overline{RD} delay time	t_{CLRL3}			—	15	ns	
\overline{DW} delay time	t_{CHDWL3}	CLK \overline{DW}		—	15	ns	
\overline{DW} delay time	t_{CHDWH3}			—	15	ns	
Output data delay time	t_{CHDV3}	CLK D31 to D16		—	15	ns	
CAS $\downarrow \rightarrow$ valid data input time	t_{CLDV3}	CAS D31 to D16		—	$t_{CYC} - 17$	ns	
CAS $\downarrow \rightarrow$ data hold time	t_{CADH3}			0	—	ns	



*1 : Q4S indicates Q4HR (Read) of Single DRAM cycle or Q4HW (Write) cycle.

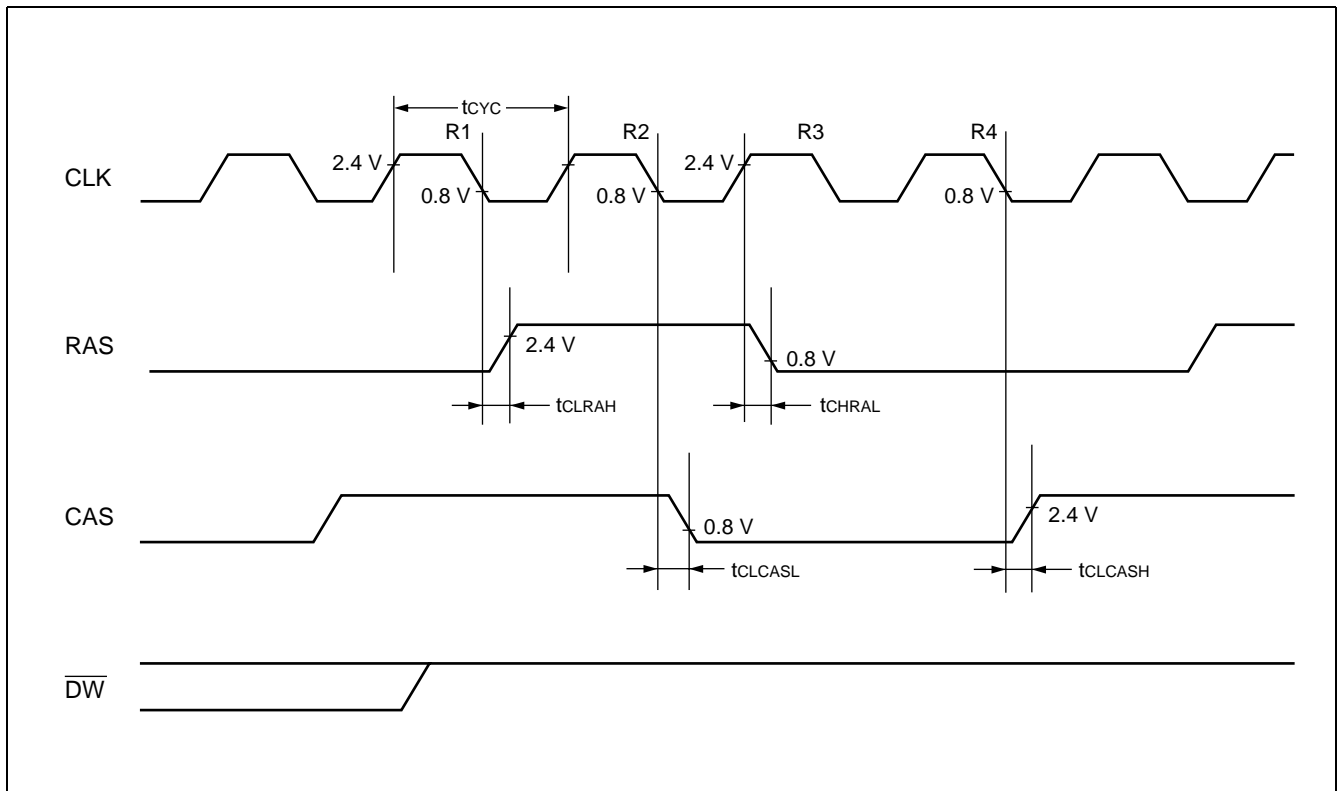
*2 : - - - - indicates the timing when the bus cycle begins from the high speed page mode.

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(12) CBR Refresh

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

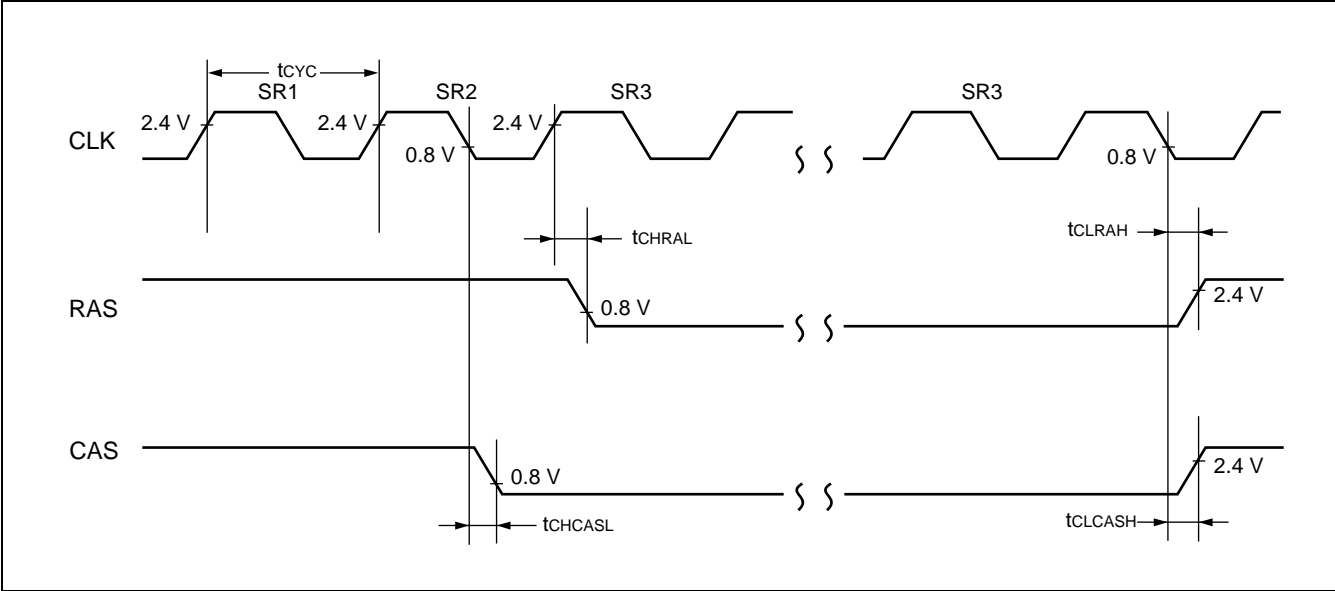
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t_{CLRAH}	CLK RAS	—	—	15	ns	
RAS delay time	t_{CHRAL}			—	15	ns	
CAS delay time	t_{CLCASL}	CLK CAS	—	—	15	ns	
CAS delay time	t_{CLCASH}			—	15	ns	



(13) Self Refresh

(V_{CC} = 3.0 V to 3.6 V, AV_{SS} = V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

Parameter	Symbol	Pin name	Condi- tion	Value		Unit	Remarks
				Min.	Max.		
RAS delay time	t _{CLRAH}	CLK RAS	—	—	15	ns	
RAS delay time	t _{CHRAL}			—	15	ns	
CAS delay time	t _{CLCASL}	CLK CAS		—	15	ns	
CAS delay time	t _{CLCASH}			—	15	ns	



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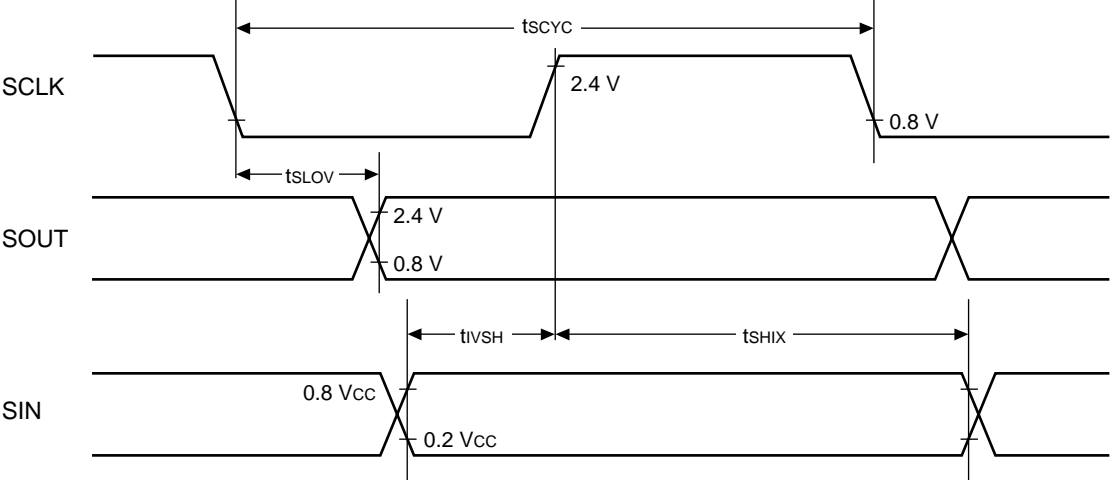
(14) UART Timing

(V_{CC} = 3.0 V to 3.6 V, AV_{SS} = V_{SS} = 0.0 V, T_A = 0 °C to +70 °C)

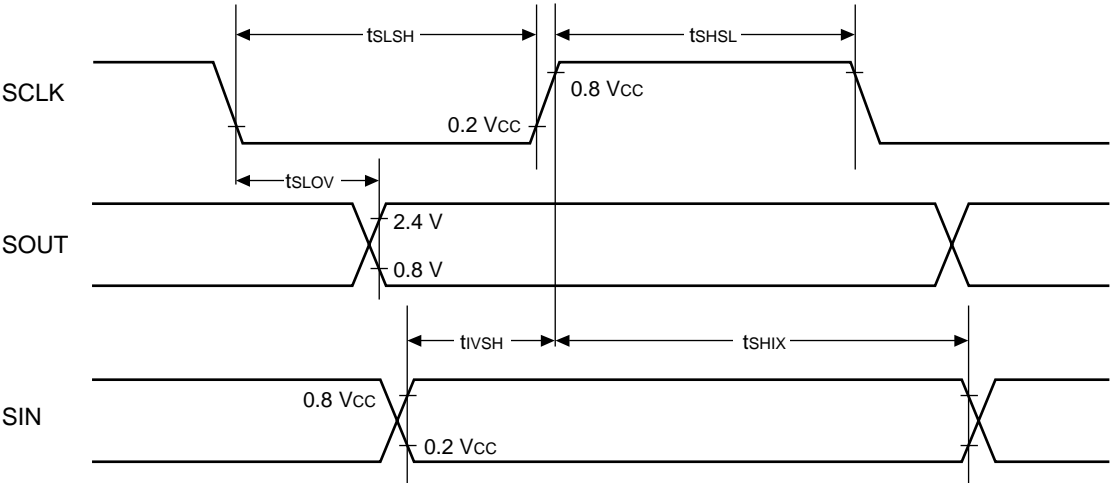
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t _{SCYC}	—	Internal shift clock mode	8 t _{CYCP}	—	ns	
SCLK ↓→ SOUT delay time	t _{SLOV}	—		-80	80	ns	
Valid SIN → SCLK ↑	t _{IVSH}	—		100	—	ns	
SCLK ↑→ valid SIN hold time	t _{SHIX}	—		60	—	ns	
Serial clock "H" pulse width	t _{SHSL}	—	External shift clock mode	4 t _{CYCP}	—	ns	
Serial clock "L" pulse width	t _{SLSH}	—		4 t _{CYCP}	—	ns	
SCLK ↓→ SOUT delay time	t _{SLOV}	—		—	150	ns	
Valid SIN → SCLK ↑	t _{IVSH}	—		60	—	ns	
SCLK ↑→ valid SIN hold time	t _{SHIX}	—		60	—	ns	

- Notes:
- This rating is for AC characteristics in CLK synchronous mode.
 - t_{CYCP}: A cycle time of peripheral system clock

• Internal shift clock mode



• External shift clock mode



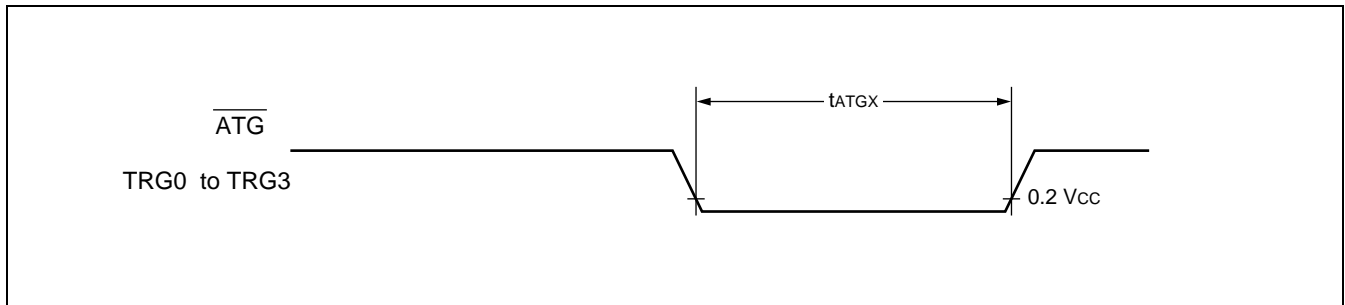
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(15) Trigger System Input Timing to

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $A_{V_{SS}} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
A/D start trigger input time	t_{ATGX}	\overline{ATG}	—	$5 t_{CYCP}$	—	ns	
PPG start trigger input time	t_{PTGR}	TRG0 to TRG3	—	$5 t_{CYCP}$	—	ns	

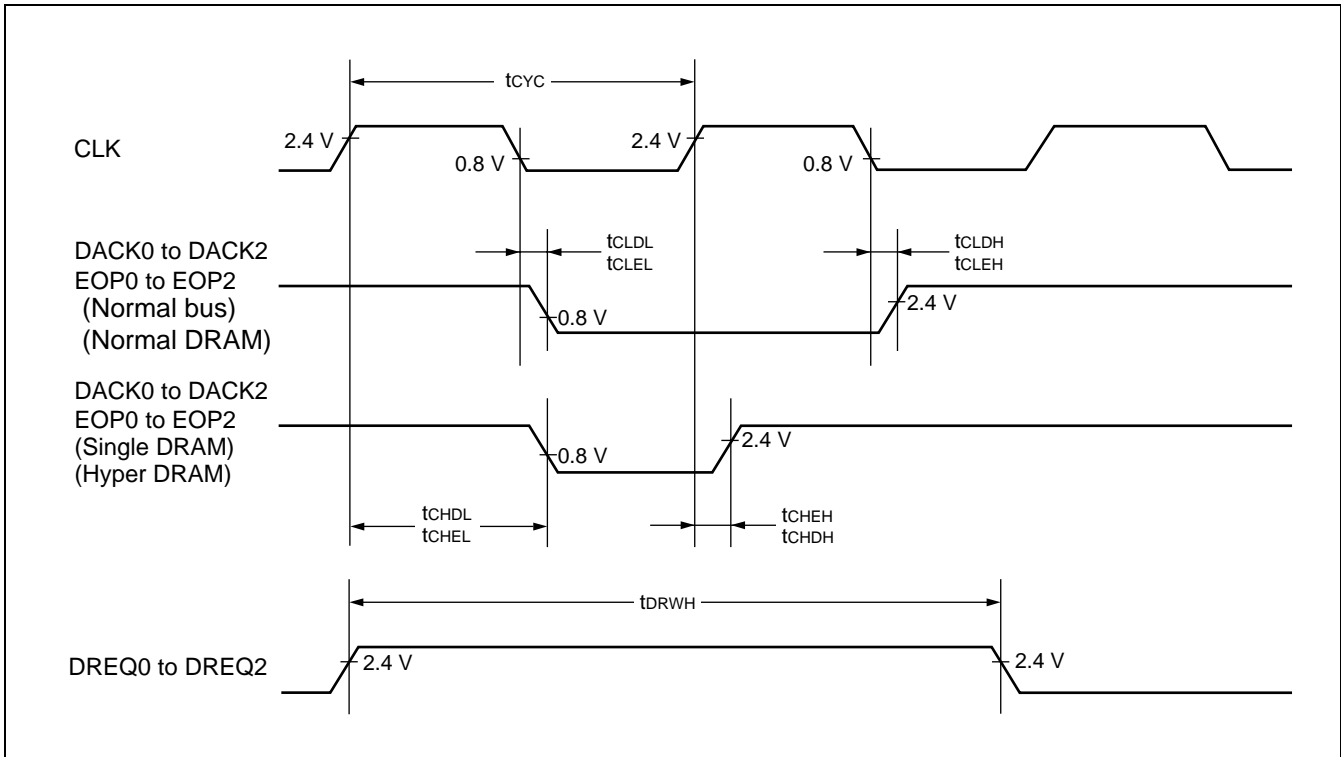
Note : t_{CYCP} : A cycle time of peripheral system clock



(16) DMA Controller Timing

($V_{CC} = 3.0\text{ V to }3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C to }+70\text{ }^\circ\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
DREQ input pulse width	t_{DRWH}	DREQ0 to DREQ2	—	$2 t_{CYC}$	—	ns	
DACK delay time (Normal bus) (Normal DRAM)	t_{CLDL}	CLK DACK0 to DACK2		—	6	ns	
	t_{CLDH}	DACK0 to DACK2		—	6	ns	
EOP delay time (Normal bus) (Normal DRAM)	t_{CLEL}	CLK EOP0 to EOP2		—	6	ns	
	t_{CLEH}			—	6	ns	
DACK delay time (Single DRAM) (Hyper DRAM)	t_{CHDL}	CLK DACK0 to DACK2		—	$n / 2 \times t_{CYC}$	ns	
	t_{CHDH}			—	6	ns	
EOP delay time (Single DRAM) (Hyper DRAM)	t_{CHEL}	CLK EOP0 to EOP2		—	$n / 2 \times t_{CYC}$	ns	
	t_{CHEH}			—	6	ns	



5. A/D Converter Block Electrical Characteristics

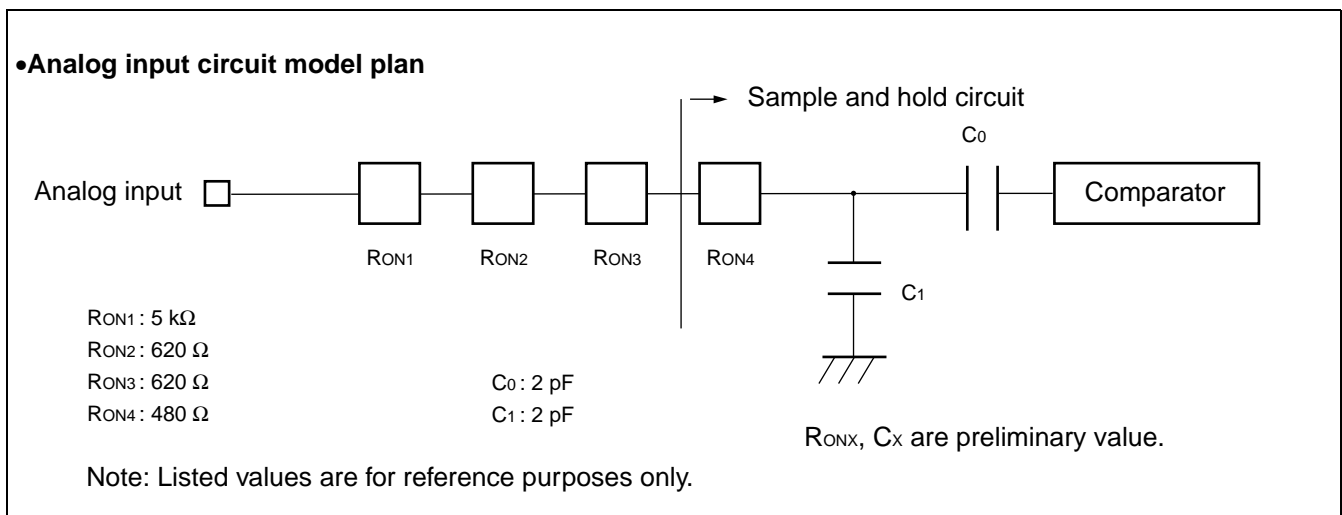
($AV_{CC} = V_{CC} = +3.0\text{ V to }+3.6\text{ V}$, $AV_{SS} = V_{SS} = 0.0\text{ V}$, $AV_{RH} = +3.0\text{ V to }+3.6\text{ V}$, $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit
			Min.	Typ.	Max.	
Resolution	—	—	—	10	10	bit
Total error	—	—	—	—	± 4.0	LSB
Linearity error	—	—	—	—	± 3.0	LSB
Differentiation linearity error	—	—	—	—	± 2.5	LSB
Zero transition voltage	V_{OT}	AN0 to AN3	-1.5	+0.5	+2.5	LSB
Full-scale transition voltage	V_{FST}	AN0 to AN3	$AV_{RH} - 4.5$	$AV_{RH} - 1.5$	$AV_{RH} + 0.5$	LSB
Conversion time	—	—	5.6^{*1}	—	—	μs
Analog port input current	I_{AIN}	AN0 to AN3	—	0.1	10	μA
Analog input voltage	V_{AIN}	AN0 to AN3	AV_{SS}	—	AV_{RH}	V
Reference voltage	—	AV_{RH}	AV_{SS}	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	500	—	μA
	I_{AH}		—	—	5^{*2}	μA
Reference voltage supply current	I_R	AV_{RH}	—	500	—	μA
	I_{RH}		—	—	5^{*2}	μA
Conversion variance between channels	—	AN0 to AN3	—	—	4	LSB

*1: $AV_{CC} = V_{CC} = 3.0\text{ V to }3.6\text{ V}$ (for a machine clock of 25 MHz).

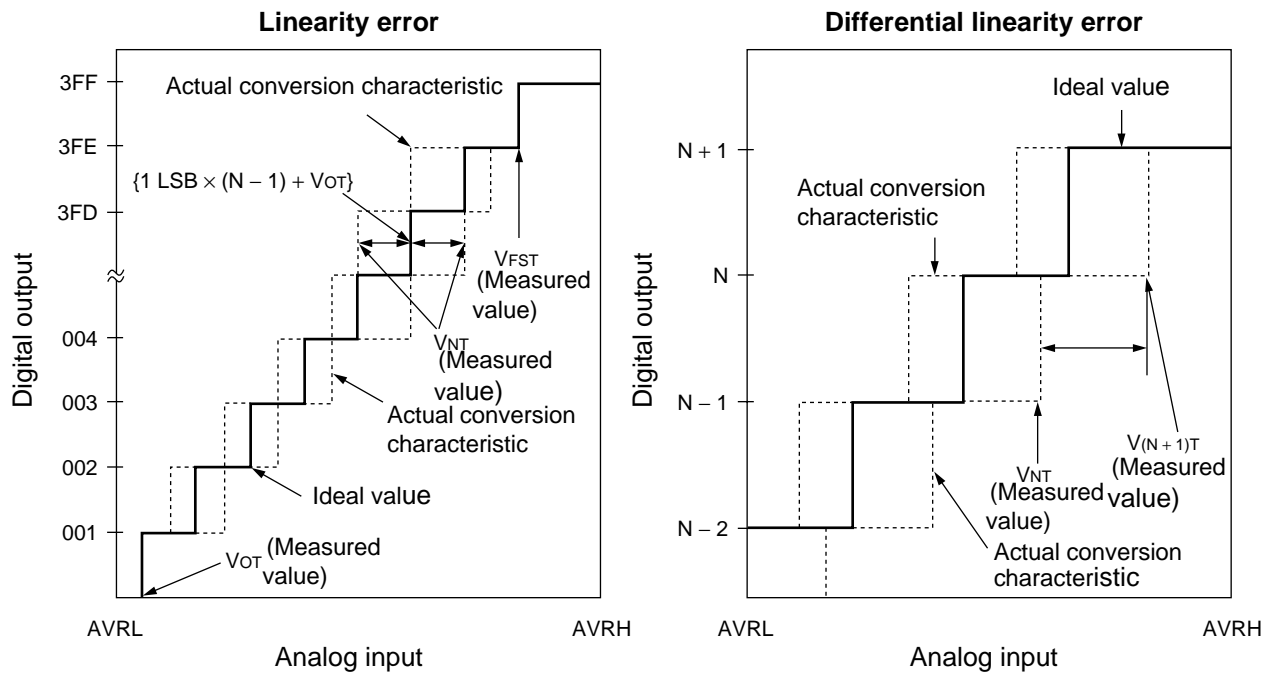
*2: Current value for A/D converters not in operation, CPU stop mode ($V_{CC} = AV_{CC} = AV_{RH} = 3.6\text{ V}$)

- Notes:
- As the absolute value of AV_{RH} decreases, relative error increases.
 - Output impedance of external circuit of analog input under following conditions;
Output impedance of external circuit $< 7\text{ k}\Omega$.
If output impedance of external circuit is too high, analog voltage sampling time may be too short for accurate sampling.



6. A/D Converter Glossary

- Resolution
The smallest change in analog voltage detected by A/D converter.
- Linearity error
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”).
- Differential linearity error
A deviation of a step voltage for changing the LSB of output code from ideal input voltage



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

$$1 \text{ LSB (Ideal value)} = \frac{AVRH - AVRL}{1024} \quad [\text{V}]$$

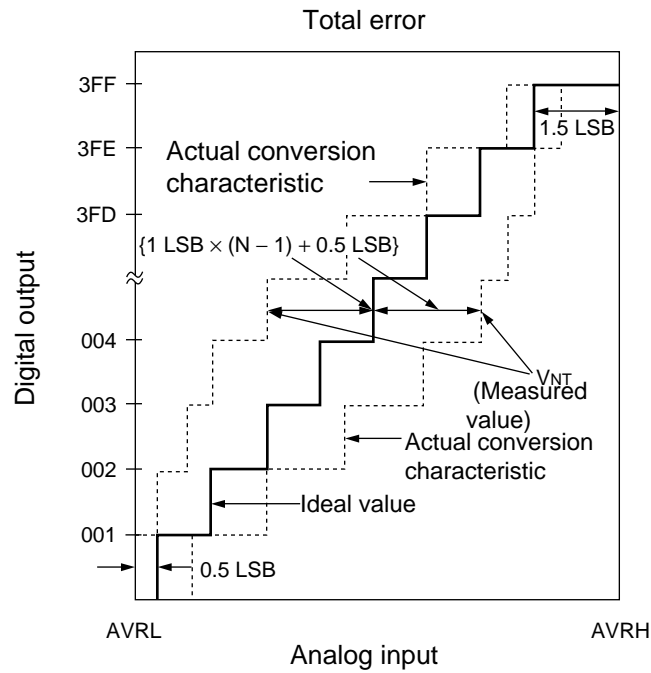
V_{OT} : A voltage for causing transition of digital output from (000)_H to (001)_H

V_{FST} : A voltage for causing transition of digital output from (3FE)_H to (3FF)_H

V_{NT} : A voltage for causing transition of digital output from (N - 1) to N

- Total error

A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

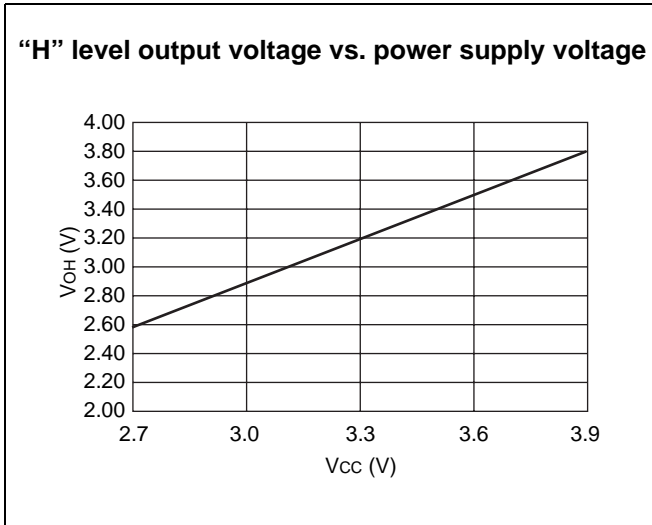
$$V_{OT} \text{ (Ideal value)} = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} \text{ (Ideal value)} = AVRH - 1.5 \text{ LSB [V]}$$

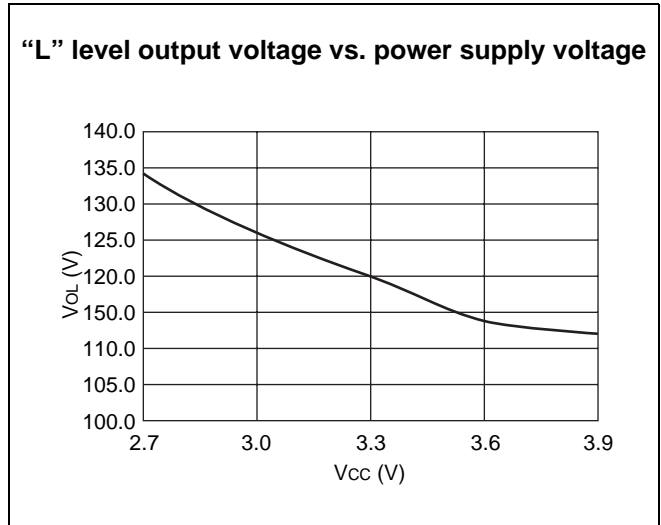
V_{NT} : A voltage for causing transition of digital output from $(N - 1)$ to N

REFERENCE DATA

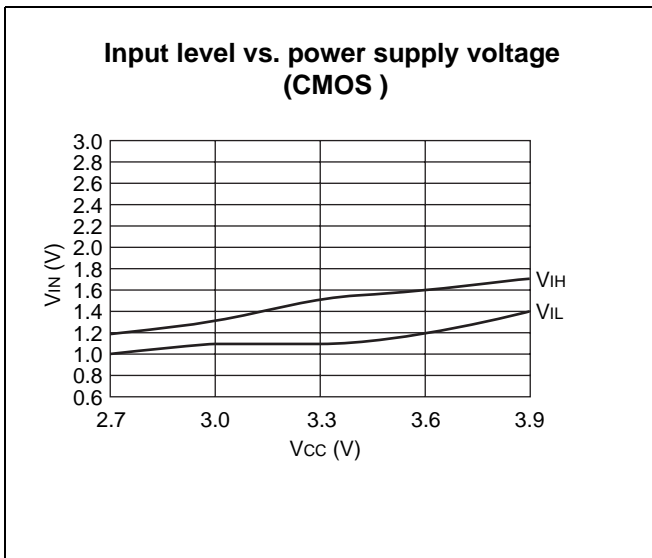
(1) "H" level output voltage



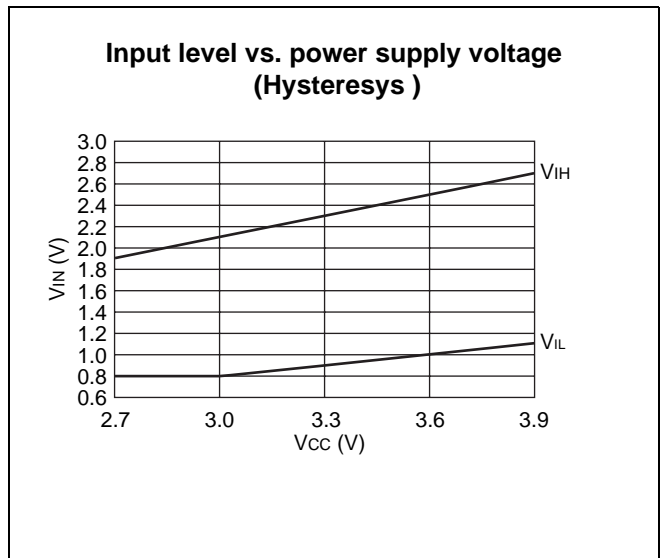
(2) "L" level output voltage



(3) "H" level input / "L" level input voltage
(CMOS input)

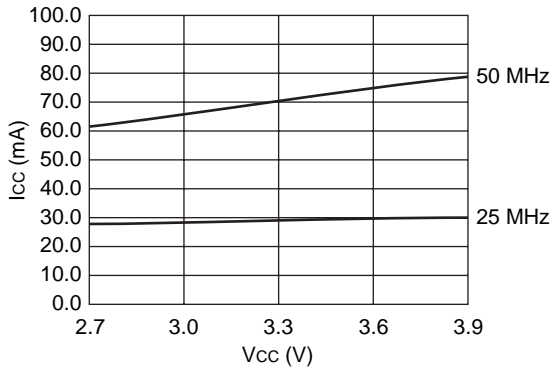


(4) "H" level input / "L" level input voltage
(Hysteresys input)

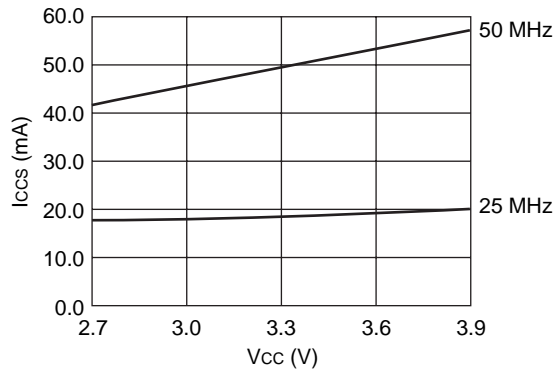


(5) Power supply current

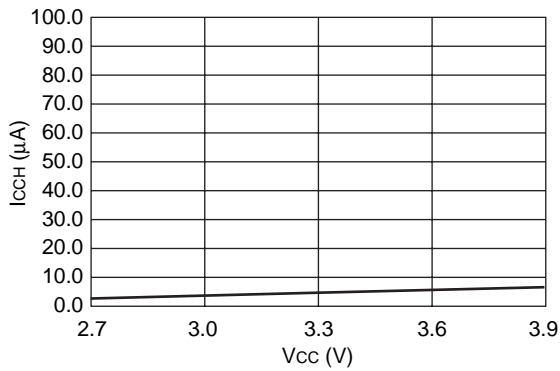
Power supply current vs. voltage



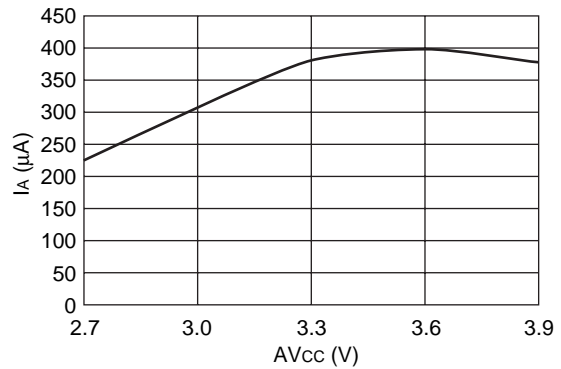
Power supply current (sleep mode) vs. power supply current



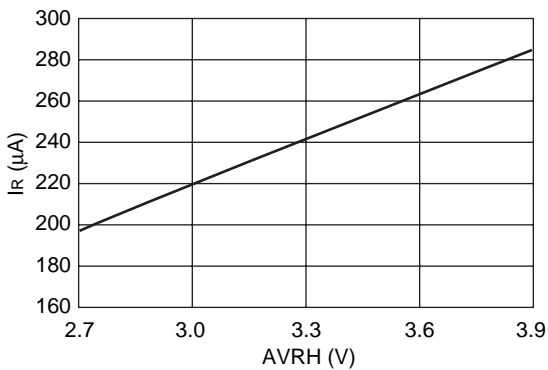
Power supply current (stop mode) vs. power supply voltage



A/D conversion block Power supply current vs. power supply voltage (25 MHz)

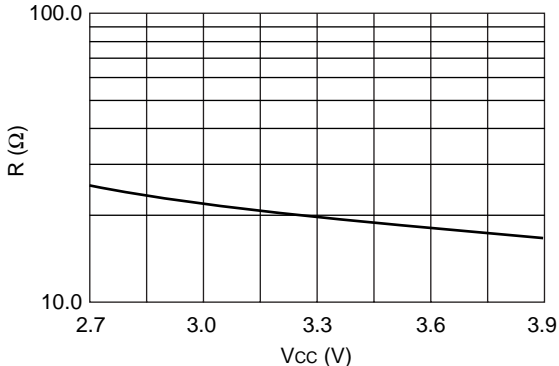


A/D conversion block reference voltage supply current vs. voltage (25 MHz)

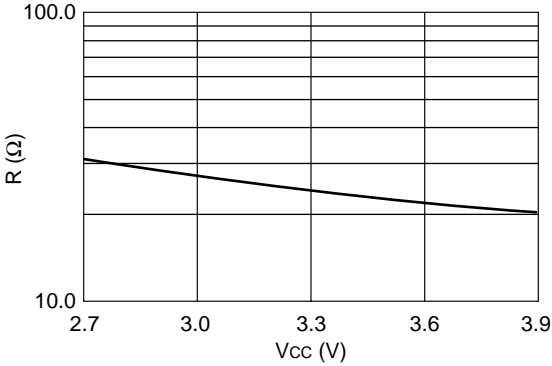


(6) Pull-up / pull-down resistance

Pull-down resistance vs. power supply voltage



Pull-up resistance vs. power supply voltage



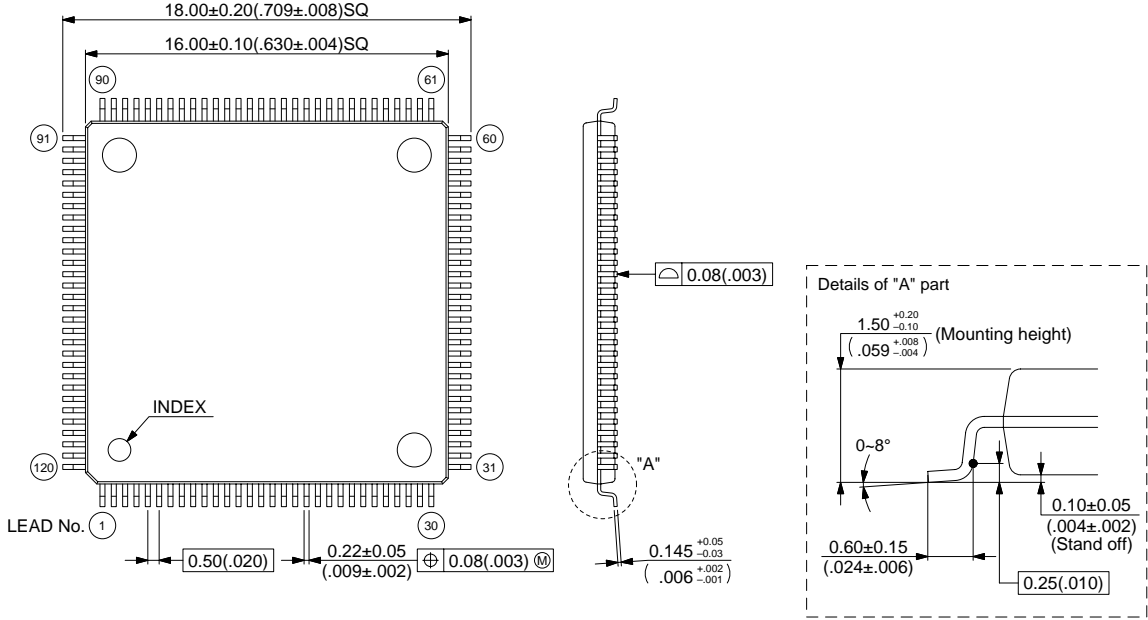
MB91107/108

■ ORDERING INFORMATION

Part number	Package	Remarks
MB91107PFV MB91108PFV	120-pin Plastic LQFP (FPT-120P-M21)	

■ PACKAGE DIMENSIONS

120-pin Plastic LQFP
(FPT-120P-M21)



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Dimensions in mm (inches)

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