FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16202-2E

32-bit Proprietary Microcontroller

CMOS

FR Family MB91191/192 Series

MB91191R/MB91192/MB91F191A/MB91F192

■ DESCRIPTION

The MB91191/192 series is a single-chip microcontroller using a 32-bit RISC-CPU (FR series) as its core. It contains peripheral I/O resources suitable for software servo control in applications such as VTRs that require high-speed CPU processing.

■ FEATURES

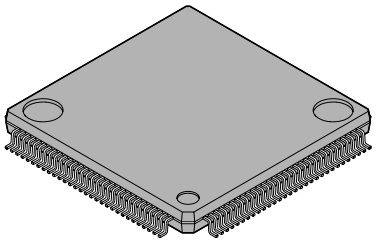
CPU

- 32-bit RISC (FR series) , load/store architecture, 5-stage pipeline
- General-purpose registers : 16 × 32-bit
- 16-bit fixed-length instructions (basic instructions) , 1 instruction per cycle
- Includes memory-to-memory transfer, bit manipulation, and barrel shift instructions :
  Optimized for embedded applications
- Includes function entry/exit instructions and multiple-register load/store instructions :
  Instruction set supports high level languages
- Register interlock function : For efficient assembly language coding
- Branch instructions with delay slots : Reduced overhead for branch operations
- Internal multiplier unit is supported at instruction level
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupts (PC and PS saving) : 6 cycles, 16 priority levels

(Continued)

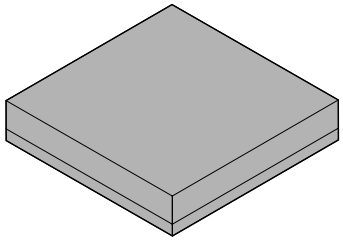
■ PACKAGE

Plastic, LQFP, 120-pin



(FPT-120P-M05)

Plastic, FLGA, 144-pin



(LGA-144P-M02)

FUJITSU

Bus Interface
- 16-bit address output, 8/16-bit data input and output
- Basic bus cycle : 2 clock cycles
- Supports interfaces for various types of memory
- Multiplexed data/address input/output
- Automatic wait cycles : Between 0 and 7 wait cycles can be specified independently for each memory area
- Unused data/address pins can be configured as input/output ports
- Supports little endian mode

Bit Search Module
- Searches, starting from the MSB, for the position of the first 1/0 bit transition in a word. The operation is performed in one cycle.

Serial I/O
- 3 channels with internal buffer RAM (automatic transfer of up to 128 bytes)
- Independent send and receive buffer mode (automatic transfer of up to 64 bytes)

A/D Converter (Successive Approximation Type)
- 10-bit × 16 channels
- Uses successive approximation conversion method (conversion time : 8.4 μs @ 20 MHz)
- Channel scan function
- Hardware and software conversion start functions
- Internal FIFO (Software conversion : 6 stages, Hardware conversion : 6 stages)

Timers
- 16-bit × 4 channels
- 16-bit timer/counter × 1 channel (with square wave output)
- 8/16-bit timer/counter × 1 channel (with square wave output)

FG input unit
- Incorporates capstan, drum, and reel input circuits

Capture unit
- Internal 24-bit free-run counter (Minimum resolution = 50 ns @ 20 MHz)
- Internal FIFO (Data : 21-bit × 8, Detection : 8-bit × 8)

Programmable pattern generator
- Internal RAM buffer (PPG0 : 256 bytes, PPG1 : 64 bytes)
- Output timing resolution : 800 ns @ 20 MHz
- Includes an A/D converter hardware start function

Realtime timing generator
- RTG : 3 circuits
- Output timing resolution : 400 ns or 800 ns selectable
- Timing output ports : 5 ports

PWM
- 12-bit PWM × 6 channels (rate, multi-type)
- Base frequency = 78.1 kHz or 39.0 kHz (@ 20 MHz) selectable

(Continued)

(Continued)

PWC

- 8-bit PWC × 1 channel (with mask input)
- Measurement resolution : 400 ns @ 20 MHz

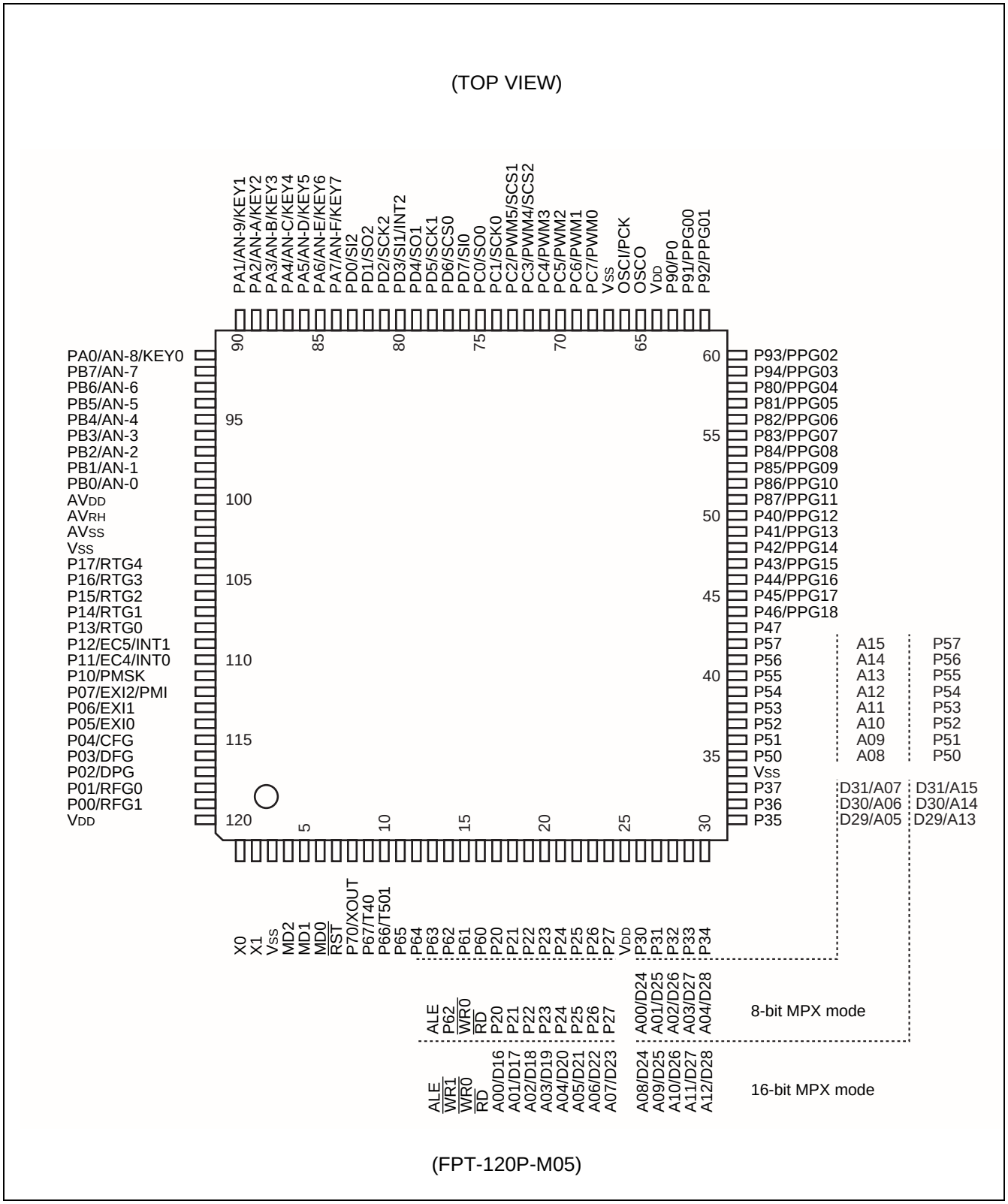
General-purpose prescaler

- 10-bit prescaler × 1 channel (with square wave and pulse outputs)
- Dedicated internal oscillator circuit
- Includes load function driven by PPG output

Interrupt control

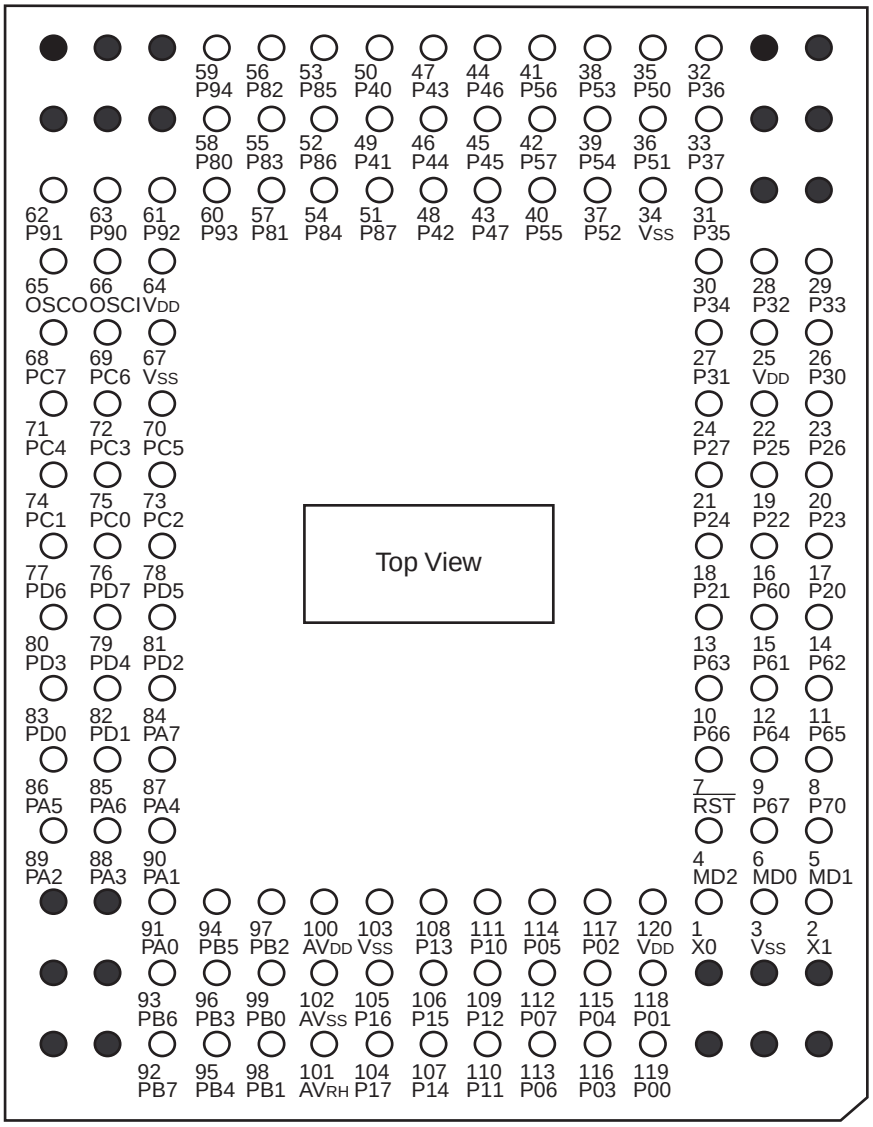
- External interrupts : 3 inputs
- Key input interrupt : 8 inputs

■ PIN ASSIGNMENT



(Continued)

(Continued)



(LGA-144P-M02)

Note : The FLGA-144 package is not supplied for the MB91191 series.
It is supplied only for the MB91192 series.

■ PIN DESCRIPTIONS

Pin No.	Pin Name	Circuit Type	Function
1	X0 (I)	A	Crystal oscillator pins
2	X1 (O)		
3	V_{SS}	—	V_{SS} pin
4	MD2	B	Operation mode setting pins CMOS Schmitt inputs
5	MD1		
6	MD0		
7	$\overline{RST}$	B	Reset input pin. CMOS Schmitt input.
8	P70/XOUT	C	Shared pin with clock output (X0/2, PCK/2) . CMOS input.
9	P67/T40	C	Shared pin with timer 4 square wave output. CMOS input.
10	P66/T501		Shared pin with timer 5 square wave output. CMOS input.
11	P65		General-purpose I/O port. CMOS input.
12	P64		General-purpose I/O port. CMOS input.
13	P63/ALE/ALE		Shared pin with address strobe output. CMOS input.
14	P62/P62/$\overline{WR1}$		Shared pin with write strobe output 1. CMOS input.
15	P61/$\overline{WR0}$/$\overline{WR0}$		Shared pin with write strobe output 0. CMOS input.
16	P60/$\overline{RD}$/$\overline{RD}$		Shared pin with read strobe output. CMOS input.
17	P20/P20/D16 : A00	C	General-purpose I/O ports. CMOS inputs.
18	P21/P21/D17 : A01		
19	P22/P22/D18 : A02		
20	P23/P23/D19 : A03		
21	P24/P24/D20 : A04		
22	P25/P25/D21 : A05		
23	P26/P26/D22 : A06		
24	P27/P27/D23 : A07		
25	V_{DD}	—	Power supply pin
26	P30/D24 : A00/D24 : A08	C	Shared external bus pins and high-current I/O ports. CMOS inputs.
27	P31/D25 : A01/D25 : A09		
28	P32/D26 : A02/D26 : A10		
29	P33/D27 : A03/D27 : A11		
30	P34/D28 : A04/D28 : A12		
31	P35/D29 : A05/D29 : A13		
32	P36/D30 : A06/D30 : A14		
33	P37/D31 : A07/D31 : A15		
34	V_{SS}	—	V_{SS} pin

(Continued)

Pin No.	Pin Name	Circuit Type	Function
35	P50/A08/P50	C	Shared external bus pins and high-current I/O ports. CMOS inputs.
36	P51/A09/P51		
37	P52/A10/P52		
38	P53/A11/P53		
39	P54/A12/P54		
40	P55/A13/P55		
41	P56/A14/P56		
42	P57/A15/P57		
43	P47	C	General-purpose I/O port. CMOS input.
44	P46/PPG18		Shared pins with PPG outputs. CMOS inputs.
45	P45/PPG17		
46	P44/PPG16		
47	P43/PPG15		
48	P42/PPG14		
49	P41/PPG13		
50	P40/PPG12		
51	P87/PPG11	C	Shared pins with PPG outputs. CMOS inputs.
52	P86/PPG10		
53	P85/PPG09		
54	P84/PPG08		
55	P83/PPG07		
56	P82/PPG06		
57	P81/PPG05		
58	P80/PPG04		
59	P94/PPG03	C	Shared pins with PPG outputs. CMOS inputs.
60	P93/PPG02		
61	P92/PPG01	C	Shared pins with PPG outputs. CMOS inputs.
62	P91/PPG00		
63	P90/P0		Shared pin with general-purpose prescaler output. CMOS input.
64	V_{DD}	—	Power supply pin
65	OSCO (O)	A	Crystal oscillator pins for dedicated general-purpose prescaler oscillation.
66	OSCI/PCK (I)		
67	V_{SS}	—	V_{SS} pin

(Continued)

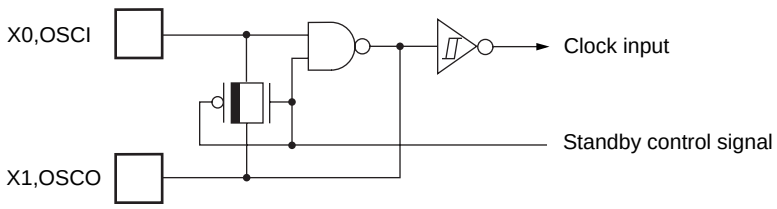
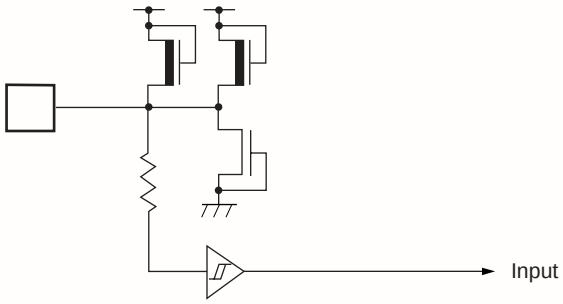
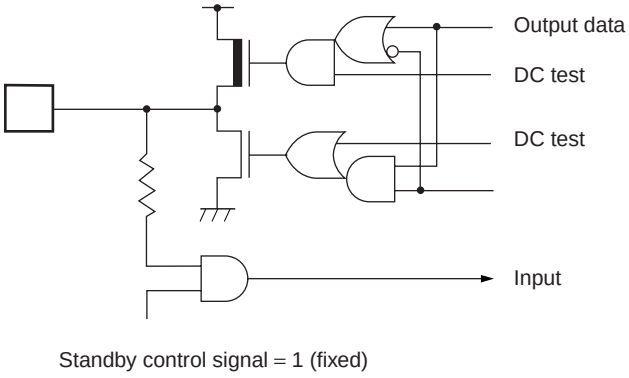
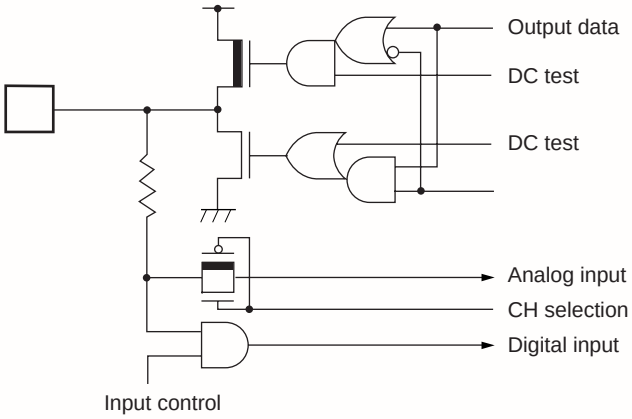
Pin No.	Pin Name	Circuit Type	Function
68	PC7/PWM0	C	Shared pins with PWM outputs. CMOS inputs.
69	PC6/PWM1		
70	PC5/PWM2		
71	PC4/PWM3		
72	PC3/PWM4/SCS2	F	Shared pin with PWM output and serial 2 chip select. CMOS Schmitt input.
73	PC2/PWM5/SCS1		Shared pin with PWM output and serial 1 chip select. CMOS Schmitt input.
74	PC1/SCK0		Shared pin with serial 0 shift clock. CMOS Schmitt input.
75	PC0/SO0	C	Shared pin with serial 0 serial output. CMOS input.
76	PD7/SI0	F	Shared pin with serial 0 serial input. CMOS Schmitt input.
77	PD6/SCS0		Shared pin with serial 0 chip select input. CMOS Schmitt input.
78	PD5/SCK1		Shared pin with serial 1 shift clock. CMOS Schmitt input.
79	PD4/SO1	C	Shared pin with serial 1 serial output. CMOS input.
80	PD3/SI1/INT2	F	Shared pin with serial 1 serial input and external interrupt 2. CMOS Schmitt input.
81	PD2/SCK2		Shared pin with serial 2 shift clock. CMOS Schmitt input.
82	PD1/SO2	C	Shared pin with serial 2 serial output. CMOS input.
83	PD0/SI2	F	Shared pin with serial 2 serial input. CMOS Schmitt input.
84	PA7/AN-F/KEY7	E	Shared pins with analog inputs and key inputs. CMOS Schmitt inputs
85	PA6/AN-E/KEY6		
86	PA5/AN-D/KEY5		
87	PA4/AN-C/KEY4		
88	PA3/AN-B/KEY3		
89	PA2/AN-A/KEY2		
90	PA1/AN-9/KEY1		
91	PA0/AN-8/KEY0		

(Continued)

(Continued)

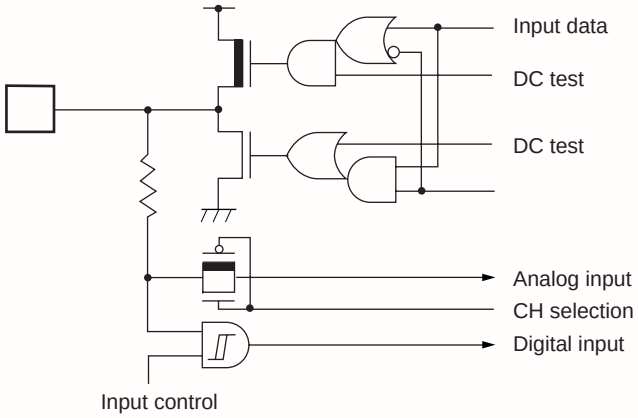
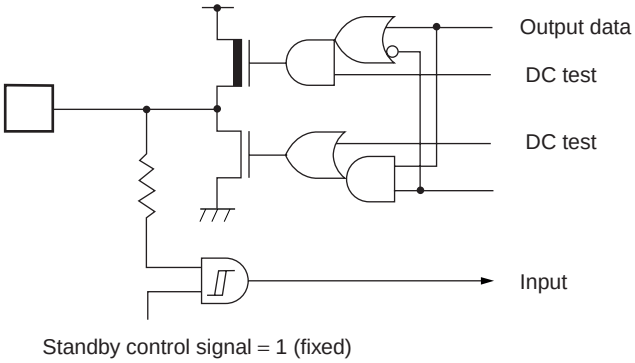
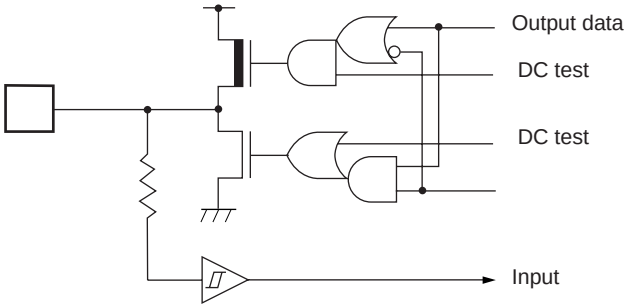
Pin No.	Pin Name	Circuit Type	Function
92	PB7/AN-7	D	Shared pins with analog inputs. CMOS Schmitt inputs.
93	PB6/AN-6		
94	PB5/AN-5		
95	PB4/AN-4		
96	PB3/AN-3		
97	PB2/AN-2		
98	PB1/AN-1		
99	PB0/AN-0		
100	AV_{DD}	—	A/D converter power supply pin
101	AV_{RH}	—	A/D converter reference power supply pin
102	AV_{SS}	—	A/D converter V_{SS} pin
103	V_{SS}	—	V_{SS} pin
104	P17/RTG4	C	Shared pins with RTG outputs. CMOS inputs.
105	P16/RTG3		
106	P15/RTG2		
107	P14/RTG1		
108	P13/RTG0		
109	P12/EC5/INT1	F	Shared pin with timer 5 clock input and external interrupt input. CMOS Schmitt input.
110	P11/EC4/INT0		Shared pin with timer 4 clock input and external interrupt input. CMOS Schmitt input.
111	P10/PMSK		Shared pin with PWC mask input. CMOS Schmitt input.
112	P07/EXI2/PMI	F	Shared pin with external capture input and PWC input. CMOS Schmitt input.
113	P06/EXI1		Shared pin with external capture input. CMOS Schmitt input.
114	P05/EXI0		
115	P04/CFG		Shared pin with capstan FG input. CMOS Schmitt input.
116	P03/DFG		Shared pin with drum FG input. CMOS Schmitt input.
117	P02/DPG		Shared pin with drum pulse input. CMOS Schmitt input.
118	P01/RFG0		Shared pins with reel FG inputs. CMOS Schmitt inputs.
119	P00/RFG1		
120	V_{DD}	—	Power supply pin

■ I/O CIRCUITS

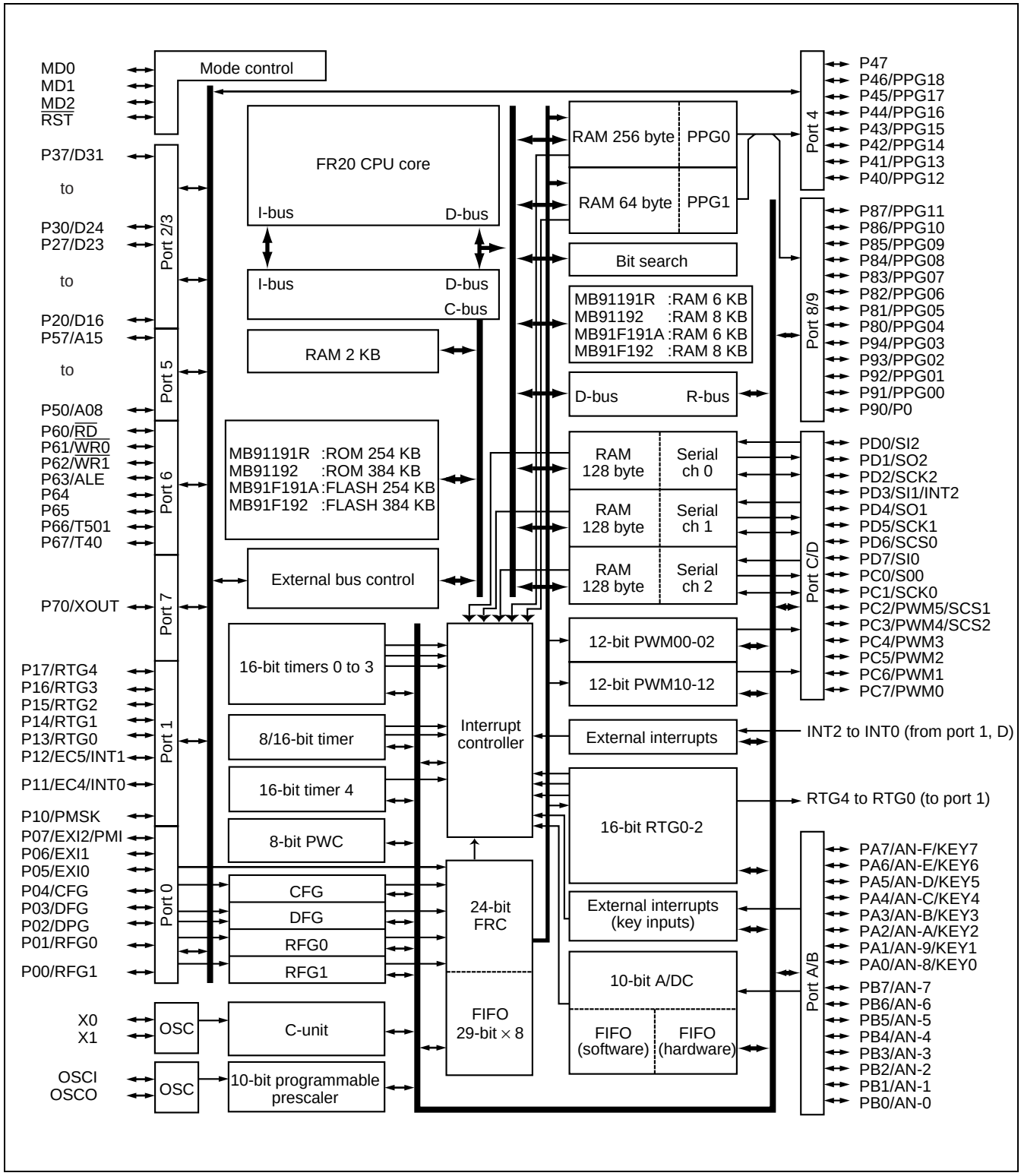
Type	Circuit	Remarks
A		• Oscillation feedback resistor : 1 MΩ approx.
B		• CMOS Schmitt input
C		• CMOS level output • CMOS input No standby control
D		• CMOS level output • CMOS input with input control • Analog input

(Continued)

(Continued)

Type	Circuit	Remarks
E		• CMOS level output • CMOS Schmitt input with input control • Analog input
F		• CMOS level output • CMOS Schmitt input No standby control
H		• CMOS level output • CMOS Schmitt input No standby control

■ BLOCK DIAGRAM



(Bus names)

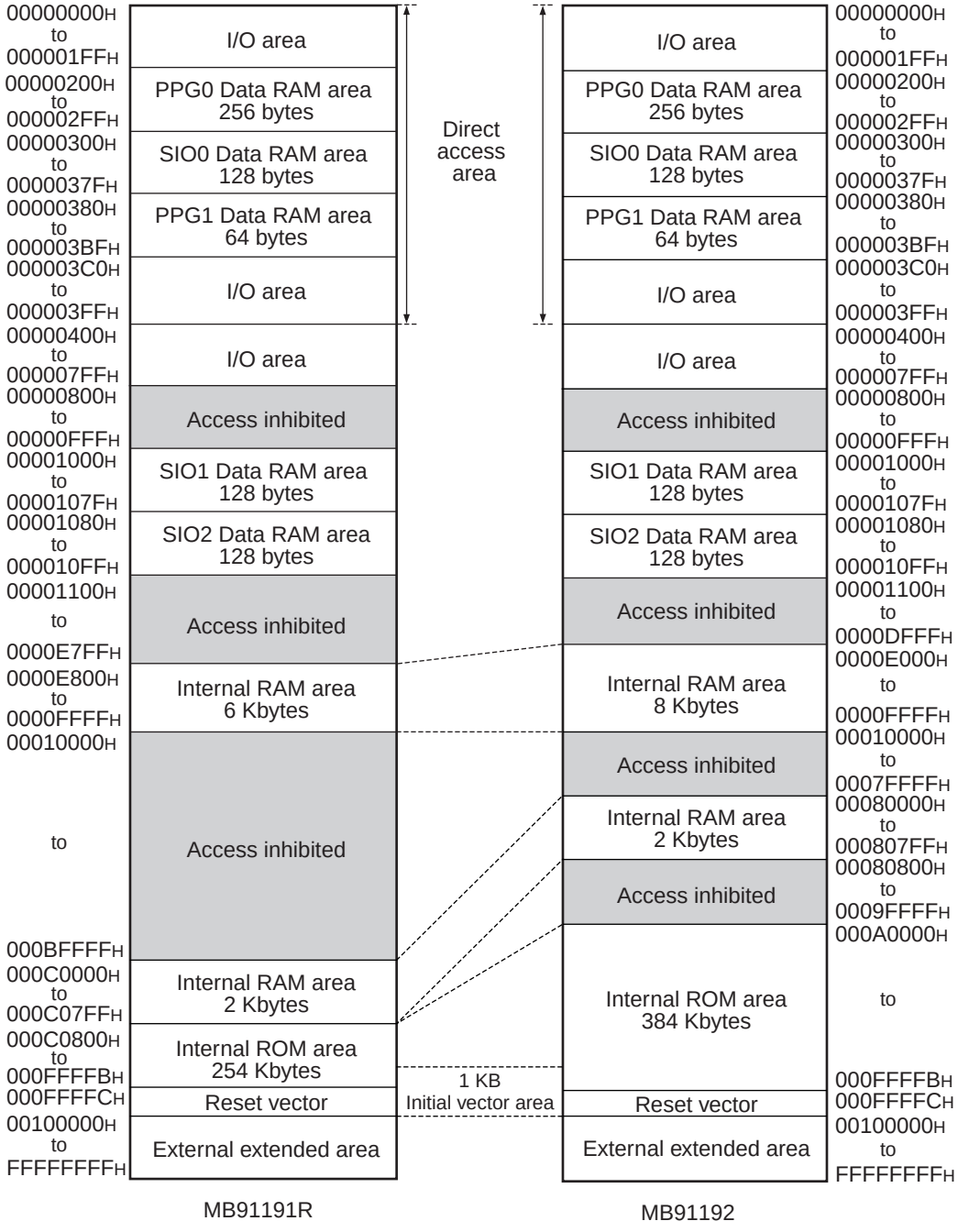
- I bus : 16-bit bus for internal instructions. As the FR family of CPUs use the Harvard architecture, instructions and data use separate buses. A bus converter is connected to the I bus.

- D bus : Internal 32-bit data bus. The internal peripherals are connected to the D bus.

- C bus : Internal multiplexed bus. Connected to the I and D buses via a switch. An external interface module is connected to the C bus. Data and instructions are multiplexed on the external data bus.

- R bus : Internal 16-bit data bus. The R bus connects to the D bus via an adapter. The I/O, clock oscillator, and interrupt controller are connected to the R bus. As the R bus is only 16 bits wide, address and data are multiplexed on the bus and therefore multiple cycles are required when the CPU accesses these resources.

■ MEMORY MAP



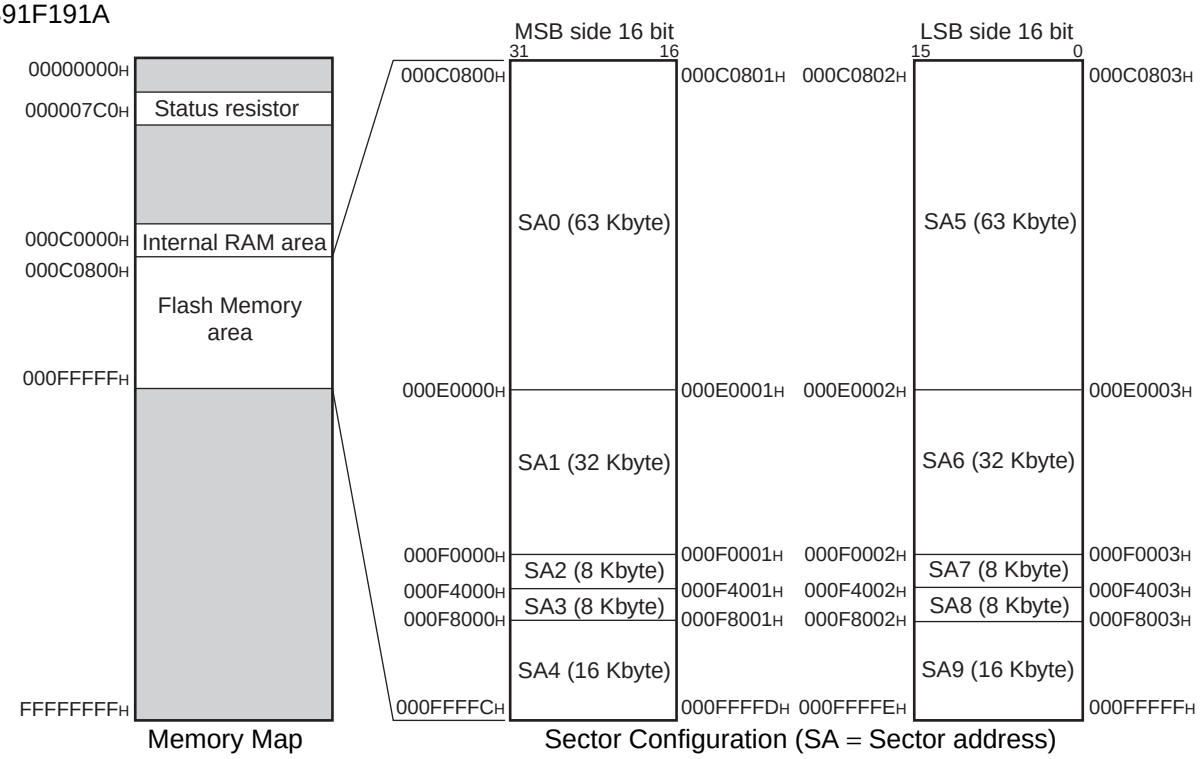
Note : The single chip mode does not allow access to the external extended area.
For access to the external extended area, use the mode register to select the internal ROM external bus mode.

■ FLASH MEMORY MAP AND SECTOR CONFIGURATION

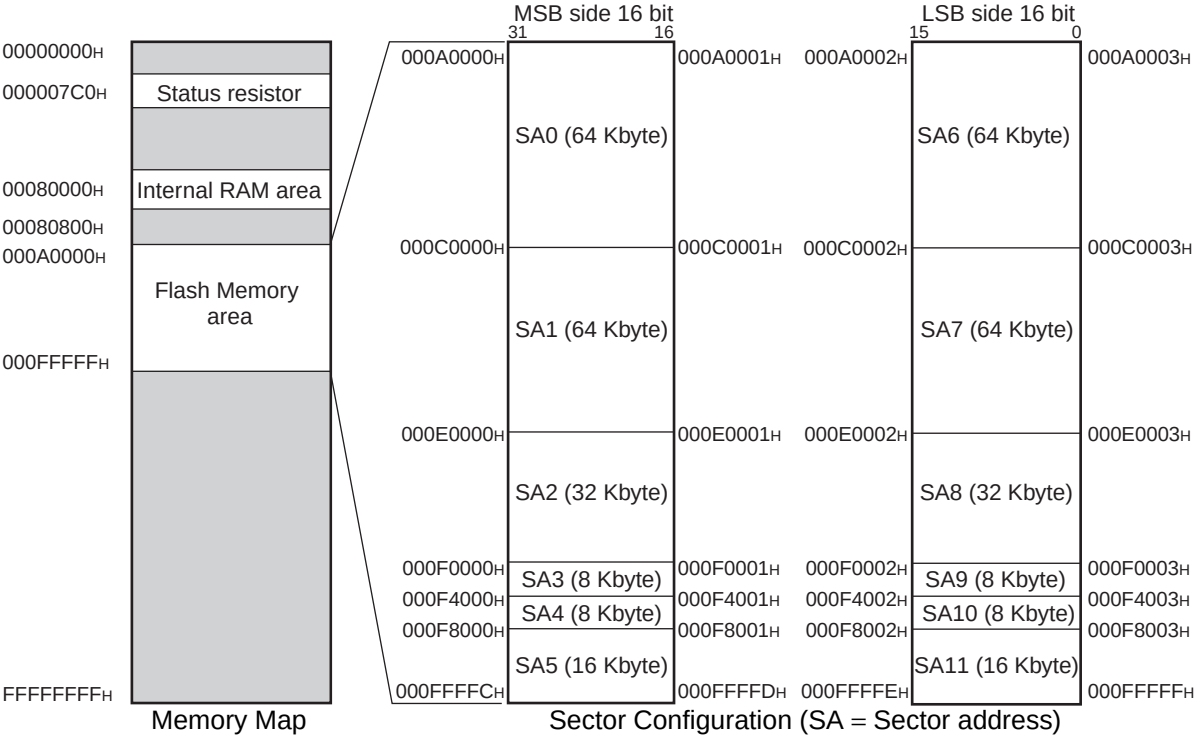
Flash memory is address-mapped differently between when accessed from the FR-CPU and when accessed from the ROM programmer.* Shown below is address mapping at access from the CPU.

* : While the on-board flash memory uses the little endian format, the FR-CPU interface circuit converts data into big endian. As this conversion function does not work during access from the ROM programmer, address mapping is different from that in CPU mode.

• MB91F191A



• MB91F192



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 3.5	V	
Analog power supply voltage	AV_{DD}	V_{SS} – 0.3	V_{SS} + 3.5	V	*1
Analog reference voltage	AV_{RH}	V_{SS} – 0.3	V_{SS} + 3.5	V	*1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 3.5	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 3.5	V	*2
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–10	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
“H” level total average output current	ΣI_{OHAV}	—	–20	mA	*5
Power consumption	P_D	—	500	mW	
Operating temperature	T_A	–20	+70	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : Care must be taken that AV_{DD} and AV_{RH} do not exceed V_{DD} + 0.3 V such as when turning on the device. Also care must be taken that AV_{RH} does not exceed AV_{DD}.

*2 : V_I and V_O may not exceed V_{DD} + 0.3 V.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output current is the average current for a single pin over a period of 100 ms.

*5 : The total average output current is the average current for all pins over a period of 100 ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{DD}	2.7	3.3	V	Normal operation
		2.0	3.3		Maintaining RAM state in stop mode
Analog power supply voltage	AV_{DD}	V_{SS} – 0.3	V_{DD} + 0.2	V	
Analog reference voltage	AV_{RH}	AV_{SS}	AV_{DD}	V	
Operating temperature	T_A	–20	70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{DD} = 3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	*3	—	0.7 V_{DD}	—	V_{DD} + 0.3	V	
	V_{IHS}	*1	—	V_{DD} – 0.4	—	V_{DD} + 0.3	V	
		*2		0.8 V_{DD}	—	V_{DD} + 0.3	V	
	V_{IHM}	MD2 to MD0	—	V_{DD}	—	V_{DD} + 0.3	V	
"L" level input voltage	V_{IL}	*3	—	V_{SS} – 0.3	—	0.2 V_{DD}	V	
	V_{ILS}	*1	—	V_{SS} – 0.3	—	V_{SS} + 0.4	V	
		*2		V_{SS} – 0.3	—	0.2 V_{DD}	V	
	V_{ILM}	MD2 to MD0	—	V_{SS} – 0.3	—	V_{SS}	V	
"H" level output voltage	V_{OH1}	*4	V_{DD} = 3.0 V, I_{OH} = –4.0 mA	2.4	—	—	V	MB91F191A
				2.4	—	—	V	MB91191R
	V_{OH2}	*5, *6	V_{DD} = 3.0 V, I_{OH} = –8.0 mA	2.4	—	—	V	MB91F191A
				2.4	—	—	V	MB91191R
"L" level output voltage	V_{OL1}	*4	V_{DD} = 3.0 V, I_{OL} = 4.0 mA	—	—	0.6	V	
	V_{OL2}	*5, *6	V_{DD} = 3.0 V, I_{OL} = 8.0 mA	—	—	0.6	V	
	V_{OL3}	*4, *5, *6	V_{DD} = 3.0 V, I_{OL} = 1.0 mA	—	—	0.3	V	MB91191R
Input leak current	I_{LI1}	*2	V_{DD} = 3.0 V, V_{SS} < V_I < V_{DD}	—	±1	±5	µA	
	I_{LIX}	X0, OSCI		—	±8	±20	µA	
Power supply current	I_{DD}	V_{DD}	V_{DD} = 3.0 V, *7	—	50.1	60	mA	MB91F191A
				—	16	25	mA	MB91191R
	I_{DDS}		V_{DD} = 3.0 V, *8	—	24	36	mA	MB91F191A
				—	13	18	mA	MB91191R
	I_{DDH}		V_{DD} = 3.0 V, T_A = 25 °C, *9	—	1	240	µA	MB91F191A
				—	10	300	µA	MB91191R
Input capacitance	C_{IN}	Other than V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, and AV_{RH}	—	—	10	—	pF	

*1 : X0, X1, OSCI, OSCO

*2 : $\overline{RST}$, PC3 to PC1, PD6, PD5, PD3, PD2, PA7 to PA0, P12 to P10, P07 to P00, PD7, PD0

*3 : Inputs other than *1, *2, MD2 to MD0

*4 : P07 to P00, P17 to P10, P27 to P20, P47 to P40, P67 to P60, P70, P87 to P80, P94 to P90, PA7 to PA0, PB7 to PB0, PC7 to PC2, PD7, PD6, PD3, PD0

*5 : P37 to P30, P57 to P50

*6 : PD5, PD4, PD2, PD1, PC1, PC0

*7 : Operating current for X0 = 20 MHz, OSCI = V_{SS} (fixed) , all port outputs = low, gear selection : CPU = 10 MHz, peripherals = 20 MHz

*8 : Operating current in sleep mode for X0 = 20 MHz, OSCI = V_{SS} (fixed), all port outputs = low, gear selection : CPU = 10 MHz, peripherals = 20 MHz

*9 : Operating current in stop mode for X0 = 20 MHz, OSCI = V_{SS} (fixed) , all port outputs = low, gear selection : CPU = 10 MHz, peripherals = 20 MHz

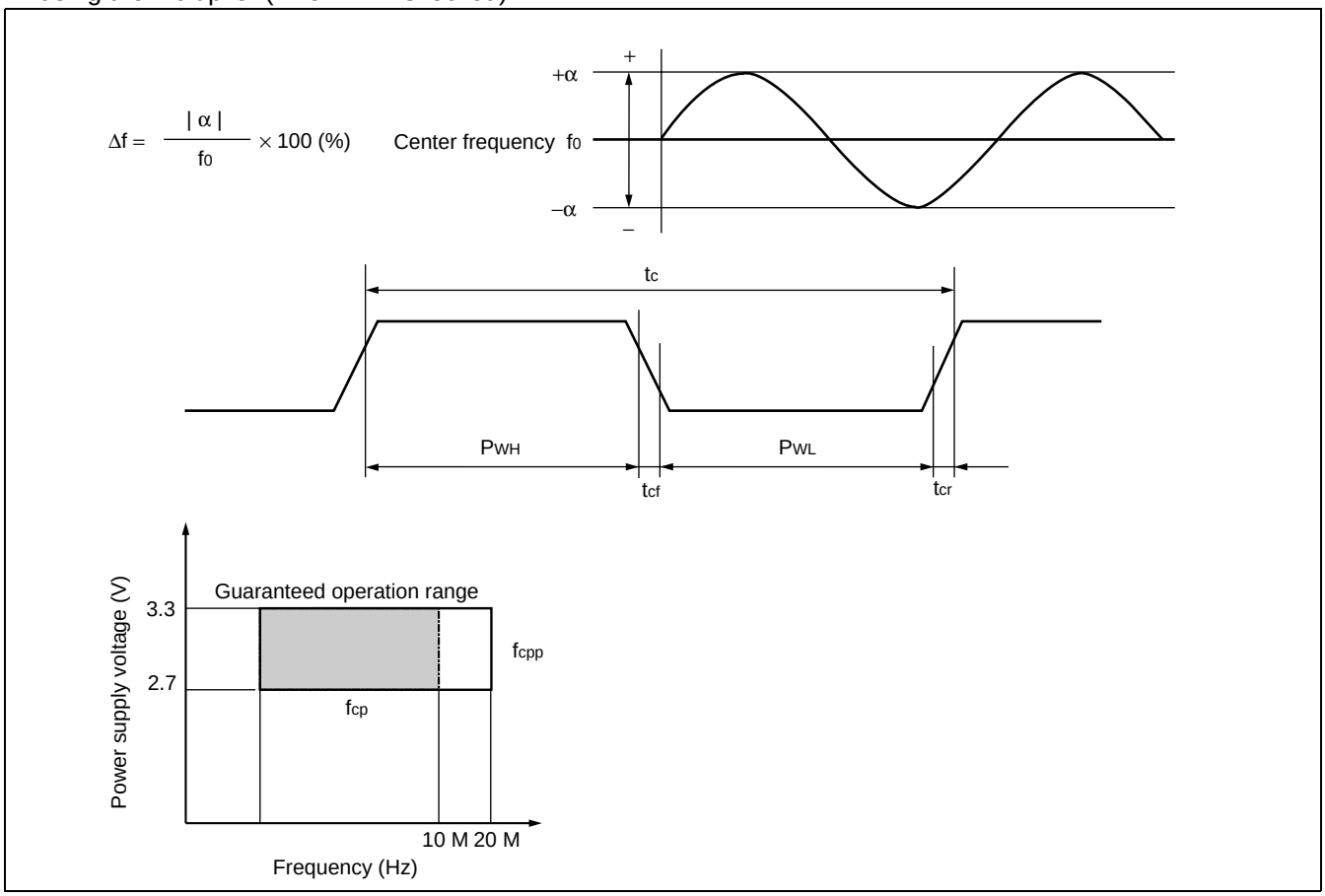
4. AC Characteristics

(1) Clock Timings

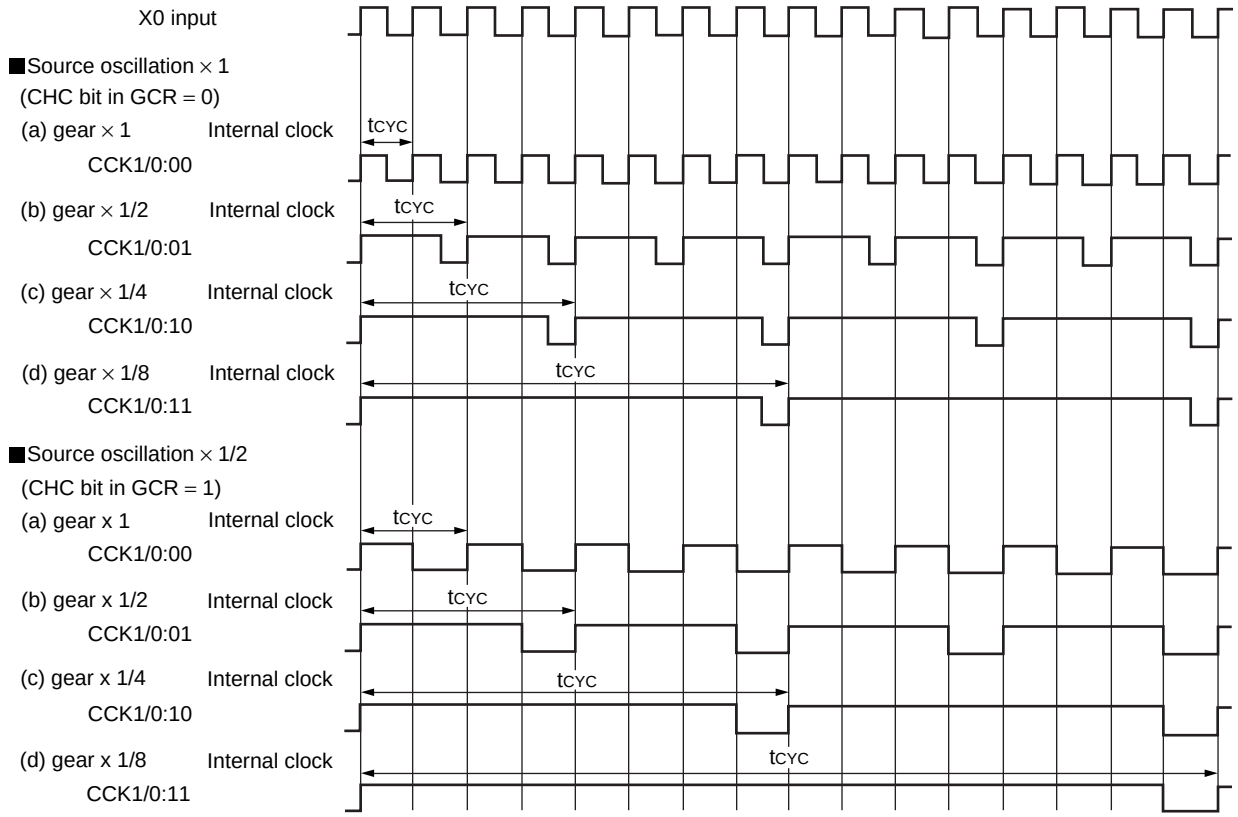
(V_{DD} = 3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter		Symbol	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency		f_C	—	10	20	MHz	
Clock cycle time		t_C	—	50	100	ns	
Frequency fluctuation* (PLL locked)		Δr	—	—	10	%	
Input clock pulse width		P_{WH}	—	20	—	ns	
		P_{WL}					
Input clock rise/fall time		t_{CR}	—	—	8	ns	
		t_{CF}					
Internal operating clock frequency	CPU	f_{CP}	When wait controller set to 1 wait cycle	5	20	MHz	
	Peripherals	f_{CPP}		10	20	MHz	
Internal operating clock cycle time	CPU	t_{CP}		50	200	ns	
	Peripherals	t_{CPP}		50	100	ns	

* : The frequency fluctuation value is the maximum percentage deviation from the preset center frequency when using the multiplier (when PLL is locked) .



The figure below shows the relationship between the X0 input and the internal clock based on the GCR (Gear Control Register) , CHC, CCK1, and CCK0 bit settings.



Where t_{CYCH} is the H level width of the internal clock and t_{CYCL} is the L level width.

For example, when set to source oscillation × 1/2, gear × 1/4 and X0 input frequency = 20 MHz : t_{CYC} = 400 ns, t_{CYCH} = 350 ns, t_{CYCL} = 50 ns

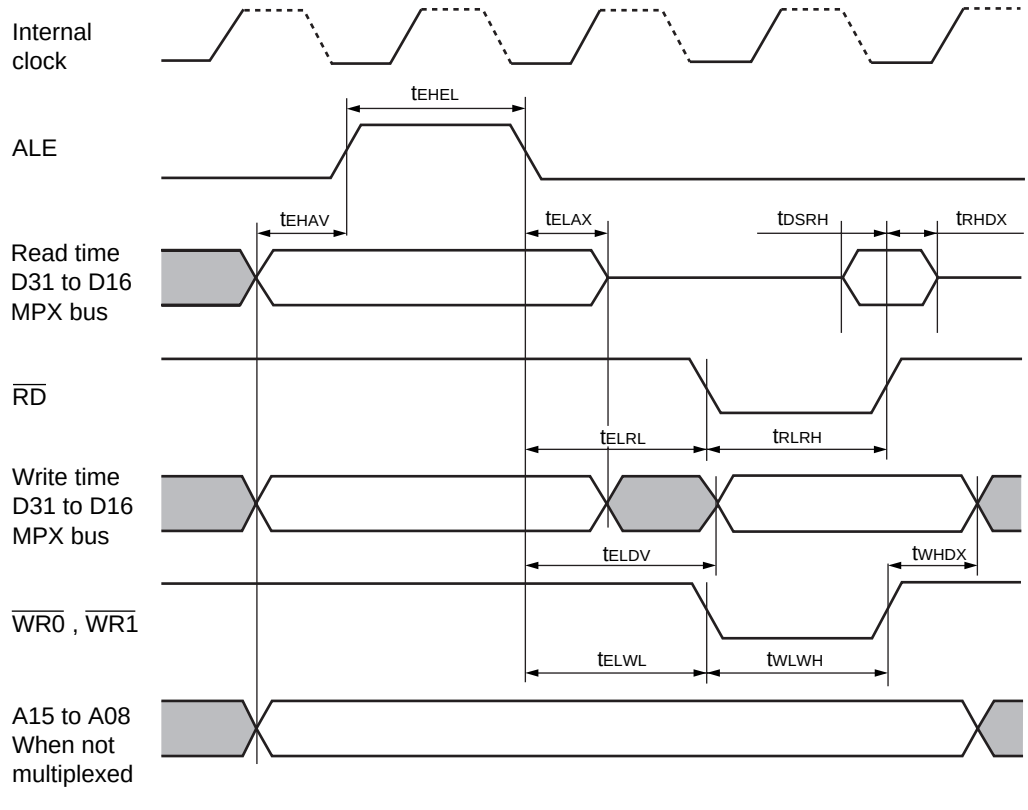
(2) Multiplex Bus Read/Write Operation

(V_{DD} = +3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
ALE pulse width	t_{EHEL}	ALE	—	t_{CYC} – 10	—	—	ns	
Address delay time	t_{EHAV}	A15 to A0, D31 to D16	—	t_{CYCH} – 15	t_{CYCH}	t_{CYCH} + 15	ns	*2
Address clear time	t_{EHAX}		—	t_{CYCL} – 2	t_{CYCL}	t_{CYCL} + 10	ns	*2
Data delay time	t_{ELDV}	D31 to D16	—	—	—	t_{CYCL} + 26	ns	*2
$\overline{RD}$ delay time	t_{ELRL}	$\overline{RD}$	—	t_{CYC} – 11	t_{CYC}	t_{CYC} + 11	ns	
$\overline{RD}$ pulse width	t_{RLRH}		—	t_{CYC} – 11	t_{CYC}	t_{CYC} + 11	ns	*1
$\overline{WR0}$, $\overline{WR1}$ delay time	t_{ELWL}	$\overline{WR0}$, $\overline{WR1}$	—	t_{CYC} – 11	t_{CYC}	t_{CYC} + 11	ns	
$\overline{WR0}$, $\overline{WR1}$ pulse width	t_{WLWH}		—	t_{CYC} – 11	t_{CYC}	t_{CYC} + 11	ns	*1
Data setup → $\overline{RD}$ ↑ time	t_{DSRH}	$\overline{RD}$, D31 to D16	—	15	—	—	ns	
$\overline{RD}$ ↑→ Data hold time	t_{RHDX}		—	0	—	—	ns	

*1 : When the bus is delayed by automatic wait insertion, add (t_{CYC} × number of wait cycles) to this value.

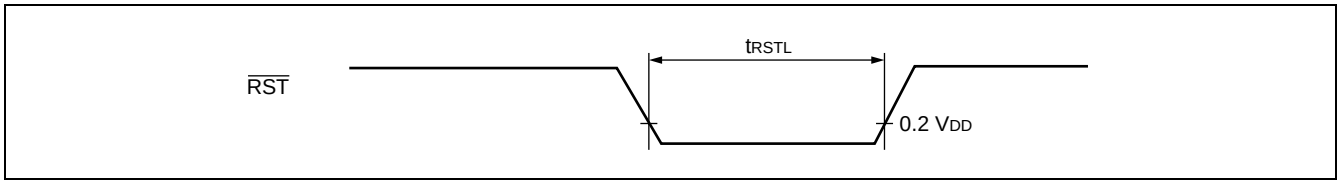
*2 : This value is for gear setting = ×1
For the value for gear settings 1/2, 1/4, and 1/8, substitute 1/2, 1/4, and 1/8 respectively for n in the formula below.
Formula : t_{CYCH} = (1 – n / 2) × t_{CYC}
t_{CYCL} = (n / 2) × t_{CYC}



(3) Reset Input Ratings

(V_{DD} = 3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

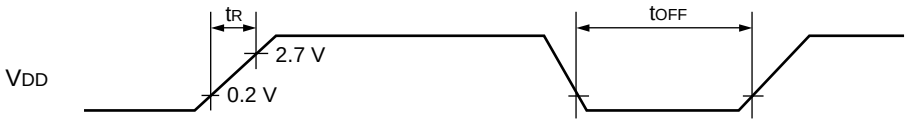
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	5 t_{CP}	—	ns	



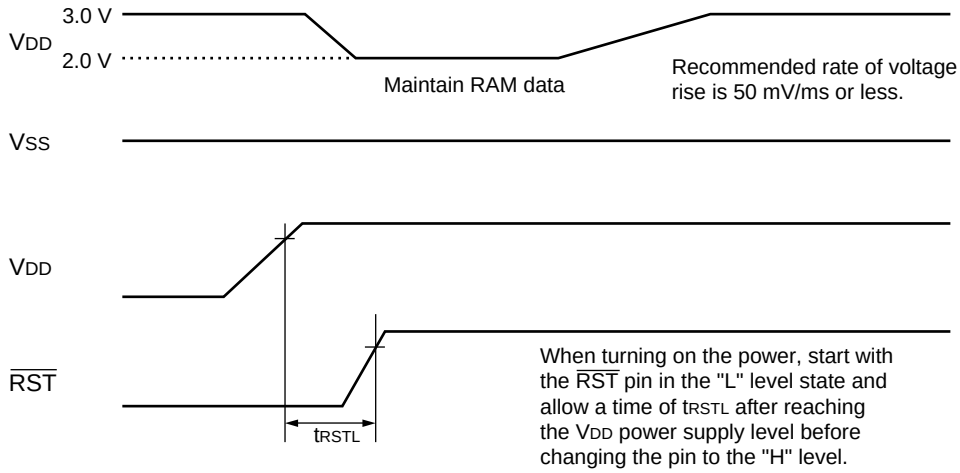
(4) Power-On Reset

(V_{DD} = 3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Paramete	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rise time	t_R	V_{DD}	—	20	ms	
Power supply cutoff time	t_{OFF}		2	—	ms	



Sudden changes in the power supply voltage may cause a power-on reset.
The recommended practice if you wish to change the power supply voltage while the device is operating is to raise the voltage smoothly.

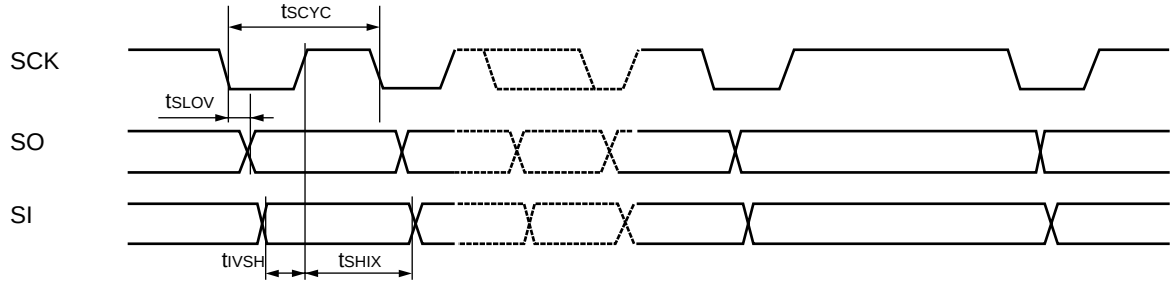


(5) Serial I/O (CH0 to 2)

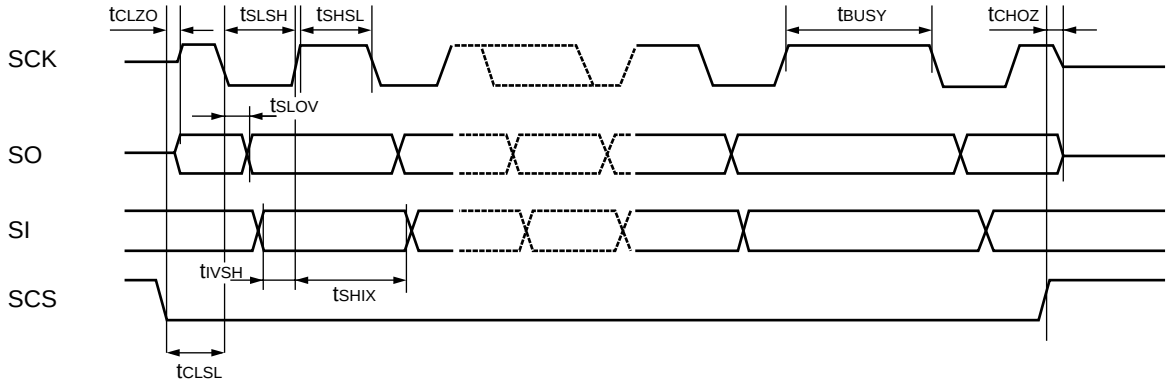
(V_{DD} = +3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter	Sym-bol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock cycle time	t_{SCYC}	Internal clock	8 t_{CPP}	—	ns	
SCK ↓ → SO delay time	t_{SLOV}		–10	50	ns	
Valid SI → SCK ↑	t_{IVSH}		50	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}		50	—	ns	
Serial clock “H” pulse width	t_{SHSL}	External clock	4 t_{CPP} – 10	—	ns	
Serial clock “L” pulse width	t_{SLSH}		4 t_{CPP} – 10	—	ns	
SCK ↓ → SO delay time	t_{SLOV}		0	50	ns	
Valid SI → SCK ↑	t_{IVSH}		50	—	ns	
SCK ↑ → valid SI hold time	t_{SHIX}		50	—	ns	
Serial busy time	t_{BUSY}		—	6 t_{CPP}	ns	
SCS ↓ → SCK, SO delay time	t_{CLZO}		—	50	ns	
SCS ↓ → SCK input mask time	t_{CLSL}		—	3 t_{CPP}	ns	
SCS ↓ → SCK, SO Hi-Z time	t_{CHOZ}	—	50	—	ns	

- Internal shift clock mode



- External shift clock mode

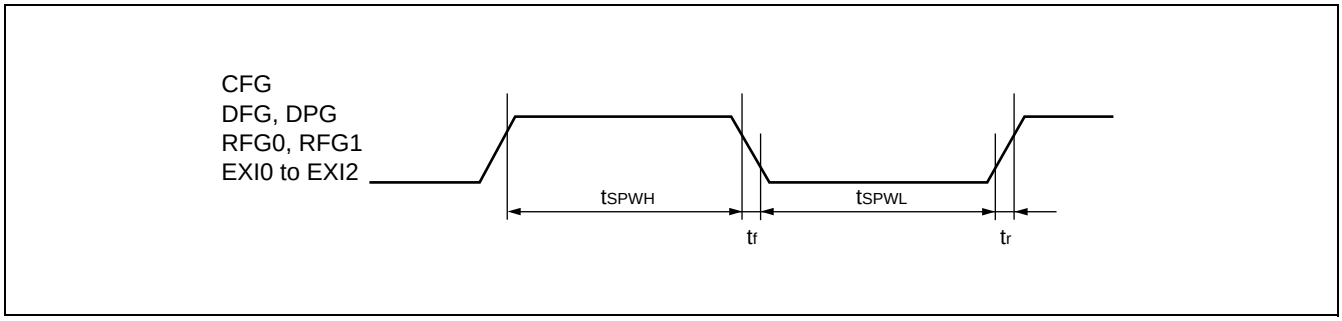


(6) FG Pulse Input

(V_{DD} = 3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Servo input “H” pulse width	t_{SPWH}	CFG, DFG, DPG, RFG0, RFG1, EXI0 to EXI2	t_C + 50	—	ns	
Servo input “L” pulse width	t_{SPWL}		t_C + 50	—	ns	

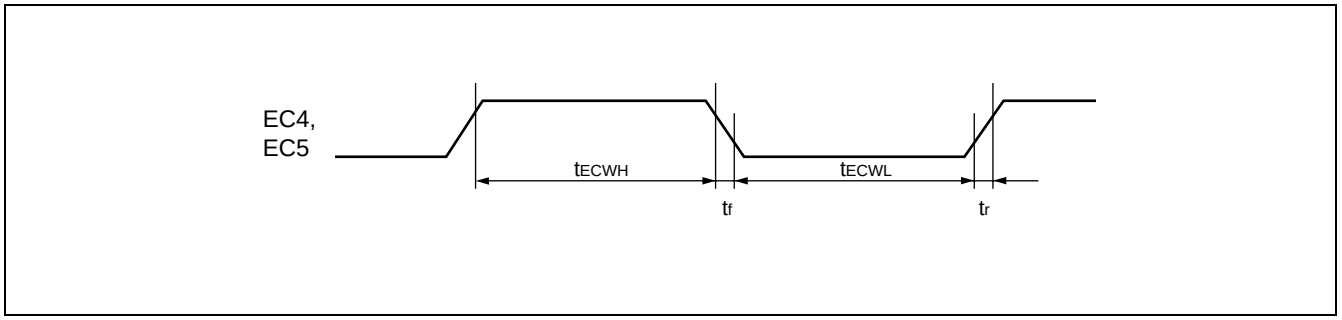
Note : t_C is the clock cycle time of the X0 and X1 pin oscillation.



(7) Timer External Clock Input

(V_{DD} = +3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

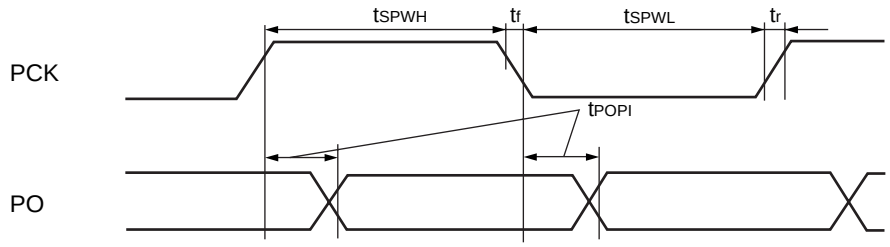
Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Timer 4 input “H” pulse width	t_{ECWH}	EC4	4 t_C + 50	—	ns	
Timer 4 input “L” pulse width	t_{ECWL}		4 t_C + 50	—	ns	
Timer 5 input “H” pulse width	t_{ECWH}	EC5	4 t_{CPP}	—	ns	
Timer 5 input “L” pulse width	t_{ECWL}		4 t_{CPP}	—	ns	



(8) General-Purpose Prescaler

(V_{DD} = 3.0 V ± 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter		Symbol	Pin Name	Value		Unit	Remarks
				Min	Max		
PCK input clock frequency		f_{CP}	PCK	—	12	MHz	
PCK input “H” pulse width		t_{SPWH}		33	—	ns	
PCK input “L” pulse width		t_{SPWL}		33	—	ns	
PCK input	Fall time	t_f	PCK	—	100	ns	
	Rise time	t_r					
PO output delay time		t_{POPI}	PO	—	80	ns	



5. Electrical Characteristics for the A/D Converter

(V_{DD} = 3.0 V + 0.3 V, V_{SS} = AV_{SS} = 0 V, T_A = –20 °C to +70 °C)

Parameter		Symbol	Pin Name	Condition	Value			Unit	Remarks
					Min	Typ	Max		
Resolution		—	—	—	—	—	10	bit	
Conversion time		—	—	—	8.4	—	—	µs	
Total error		—	—	V_{DD} = AV_{DD} = 3.0 V, AV_{RH} = 3.0 V	—	—	±4.0	LSB	
Linearity error		—	—		—	—	±3.5	LSB	
Differential linearity error		—	—		—	—	±2.0	LSB	
Zero transition error		V_{OT}	AN-0 to AN-F	V_{DD} = AV_{DD} = 3.0 V, AV_{RH} = 3.0 V	AV_{SS} – 1.5	AV_{SS} + 0.5	AV_{SS} + 2.5	LSB	
Full-scale transition error		V_{FST}	AN-0 to AN-F		AV_{RH} – 5.5	AV_{RH} – 1.5	AV_{RH} + 0.5	LSB	
Analog input current		I_{AIN}	AN-0 to AN-F	—	—	0.1	10	µA	
Analog input voltage		V_{AIN}	AN-0 to AN-F	—	AV_{SS}	—	AV_{RH}	V	
Reference voltage		AV_{RH}	AV_{RH}	—	—	—	AV_{DD}	V	
Power supply current	During conversion	I_A	AV_{DD}	V_{DD} = AV_{DD} = 3.0 V	—	3.0	—	mA	
	Conversion halted	I_{AH}			—	—	5.0	µA	
Reference voltage supply current	During conversion	I_R	AV_{RH}	V_{DD} = AV_{DD} = 3.0 V, AV_{RH} = 3.0 V	—	100	—	µA	
	Conversion halted	I_{RH}			—	—	10	µA	
Variation between channels		—	AN-0 to AN-F	—	—	—	4	LSB	

Notes : • The relative error increases as $|AV_{RH}|$ becomes smaller.

• Ensure that the output impedance of the external circuit connected to the analog input meets the following condition :

Output impedance of external circuit < 7 kΩ (approx.)

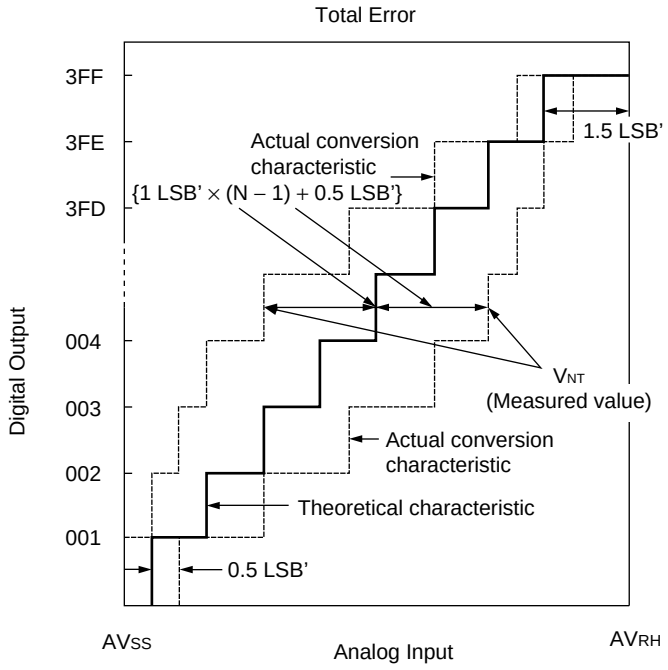
If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short. (Sampling time = 6.4 µs for a 20 MHz machine clock)

6. Flash Memory Erase and Programming performance

Parameter	Condition	Value			Unit	Remarks	
		Min	Typ	Max			
Sector erase time	T_A = +25 °C, V_{CC} = 3.0 V	—	1	15	s	Excludes 00H programming prior erasure	
Chip erase time		—	10	—	s	MB91F191A	Excludes 00H programming prior erasure
		—	12	—		MB91F192	
Half word (16 bit width) programming time		—	16	3,600	µs	Excludes system-level overhead	
Erase/Program cycle	—	10,000	—	—	cycle		
Data holding time	—	100,000	—	—	h		

7. A/D Converter Glossary

- Resolution : The change in analog voltage that can be recognized by the A/D converter.
- Linearity error
  The deviation between the actual conversion characteristics and the line linking the zero transition point ("00 0000 0000_B" ⟷ "00 0000 0001_B") and the full scale transition point ("11 1111 1110_B" ⟷ "11 1111 1111_B") .
- Differential linearity error
  The variation from the ideal input voltage required to change the output code by 1 LSB.
- Total error
  The total error is the difference between the actual value and the theoretical value.
  Includes the zero transition error, full-scale transition error and linearity error.

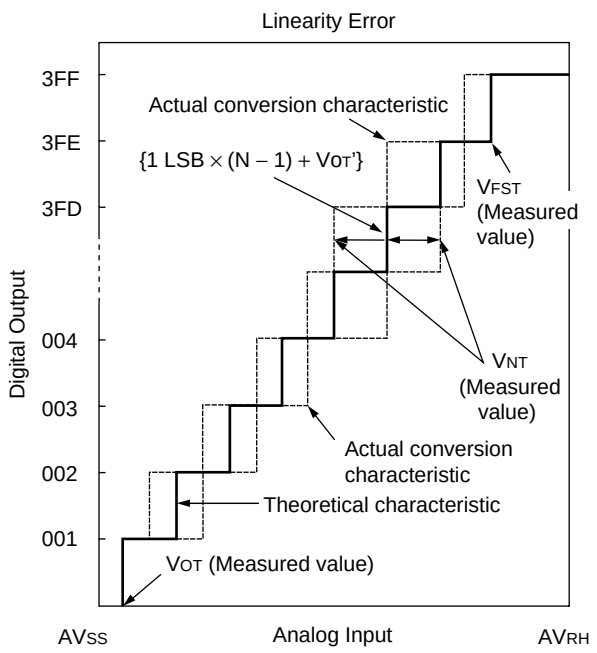


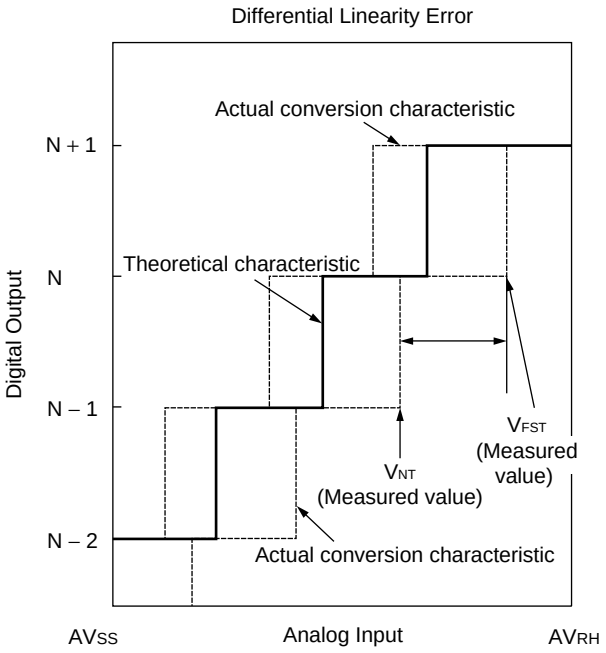
$$1\ \text{LSB'}\ (\text{Theoretical}) = \frac{AV_{RH} - AV_{SS}}{1024}\ [\text{V}]$$

$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}$$

V_{OT}' (Theoretical) $= AV_{SS} + 0.5$ LSB' [V]
V_{FST}' (Theoretical) $= AV_{RH} - 1.5$ LSB' [V]

V_{NT} : Voltage at which digital output changes from (N + 1) to N





$$\text{Linearity error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB'}} \quad [\text{LSB}]$$

$$\text{Differential linearity error for digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB'}} - 1\ \text{LSB} \quad [\text{LSB}]$$

$$V_{OT}\text{' (Theoretical)} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

V_{OT} : Voltage at which digital output changes from $(000)_H$ to $(001)_H$.
V_{FST} : Voltage at which digital output changes from $(3FE)_H$ to $(3FF)_H$.

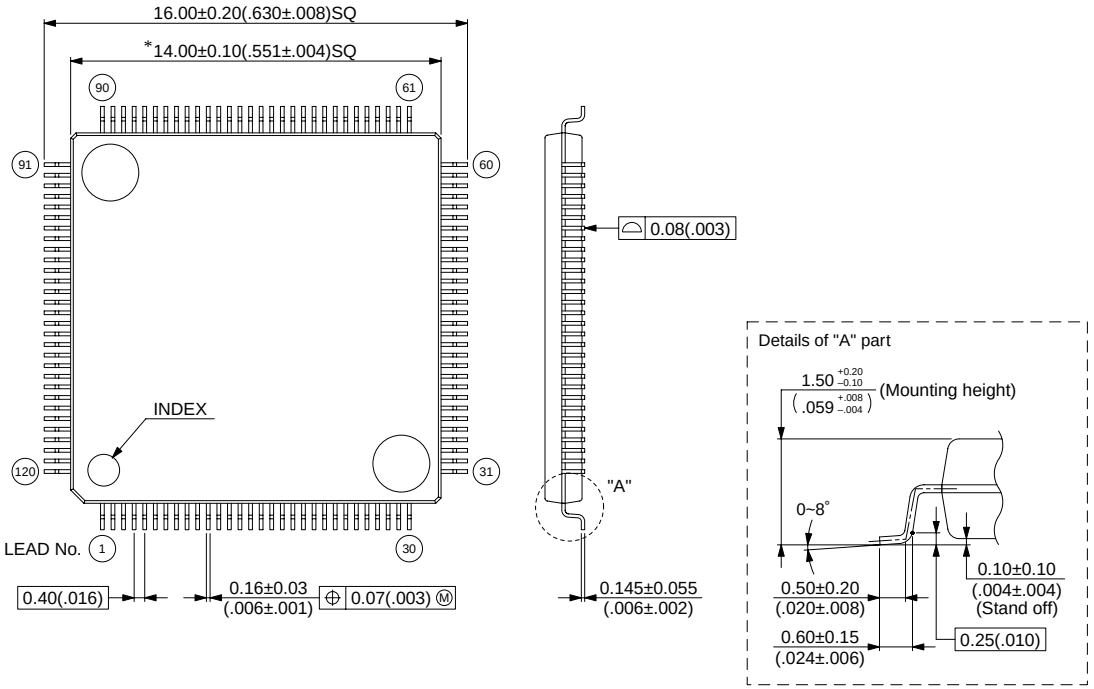
■ ORDERING INFOMATION

Part No.	Package	Remarks
MB91191RPFF MB91192PFF MB91F191APFF MB91F192PFF	Plastic LQFP, 120-pin (FPT-120P-M05)	
MB91192LGA MB91F192LGA	Plastic FLGA, 144-pin (LGA-144P-M02)	

■ PACKAGE DIMENSION

Plastic LQFP, 120-pin
(FPT-120P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

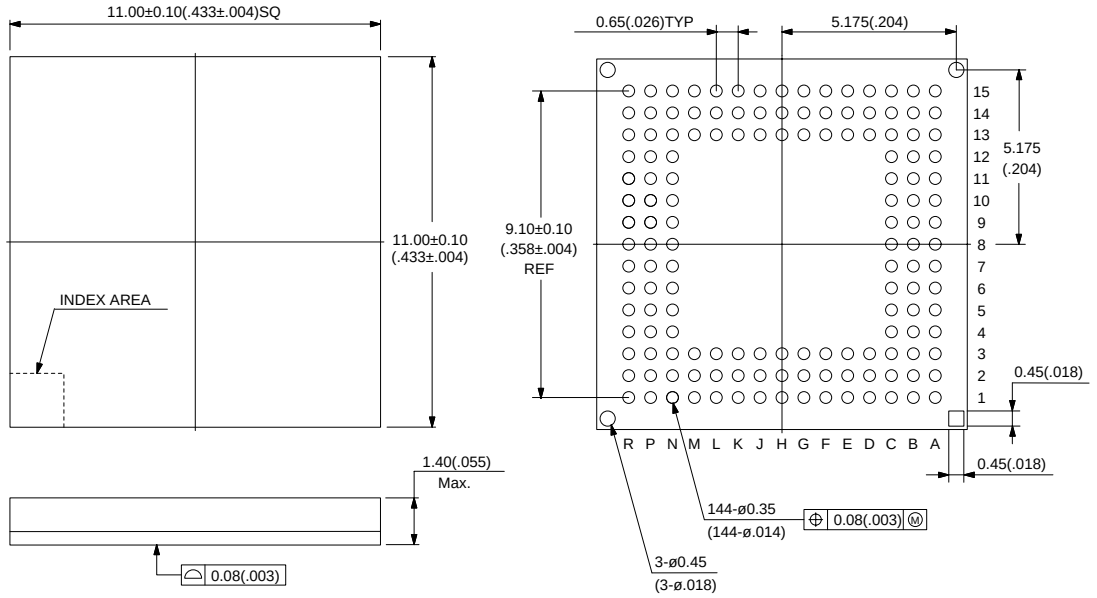


Dimensions in mm (inches).

(Continued)

(Continued)

Plastic FLGA, 144-pin
(LGA-144P-M02)



Dimensions in mm (inches).

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-partyÅfs intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0302