

32-Bit Microcontroller

CMOS

FR30 Series

MB91F127/F128

■ DESCRIPTION

This model, designed on the basis of 32-bit RISC CPU (FR30 series), is a standard single-chip micro controller with built-in I/O resources and bus control functions. The functions are suitable for built-in control that requires high-speed CPU processing.

MB91F127 includes 256 Kbytes built-in flash memory and 14 Kbytes built-in RAM. MB91F128 includes 510 Kbytes built-in flash memory and 14 Kbytes built-in RAM.

The specifications of the devices are best suited for applications requiring high-level CPU processing capabilities, such as navigation system, high-performance FAX, and printer controller.

■ FEATURES

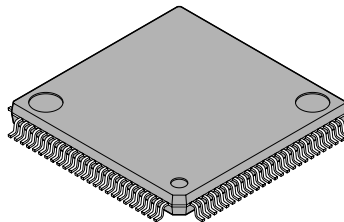
FR-CPU

- 32-bit RISC (FR30), load/store architecture, 5-step pipeline
- Operating frequency : Internal 25 MHz
- General register : 32bit x 16 registers
- 16-bit fixed-length instructions (primitives), 1 instruction/1 cycle
- Instructions of memory-to-memory transfer, bit processing, and barrel shift : Instructions suitable for built-in control

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■ PACKAGE

100 pin, Plastic LQFP



(FPT-100P-M05)

MB91F127/F128

- Function entry/exit instructions, multi load/store instruction for register data : High-level language compatible instructions
- Register interlock functions : Simple description of assembler language
- Branch instructions with delay slot : Reduced overhead on branching process
- Built-in multiplier/ Supporting at instruction level
 - Signed 32-bit multiplying : 5 cycles
 - Signed 16-bit multiplying : 3 cycles
- Interrupt (saving PC and PS) : 6 cycles, 16 priority levels

Bus interface

- Maximum of 25 MHz internal operation rate
- 25-bit address bus (32 MB space)
- 16-bit address output, 8/16-bit data input/output
- Basic bus cycle : 2-clock cycle
- Chip selection outputs specifiable in a minimum of 64 Kbytes steps : 6 outputs
- Automatic wait cycle : Specifiable flexibly from 0 cycle to 7 cycles for each area
- Supporting time-division input/output interface for address/data (for area 1 only)
- Unassigned data/address terminals are available as input/output ports
- Supporting little endian mode (selecting one area from area 1 to area 5)

DMAC (DMA controller)

- 8 channels
- Transfer factor : Interrupt request of built-in resources
- Transfer sequence : Step transfer/Block transfer/Burst transfer/Consecutive transfer
- Transfer data length : Selectable among 8 bits, 16 bits, and 32 bits
- Pausing is allowed by interrupt request

UART

- 3 channels
- Full-duplex double buffer
- Data length : 7 to 9 bits (no parity), 6 to 8 bits (with parity)
- Asynchronous (start-stop synchronization) or CLK synchronous communication is selectable
- Multi processor mode
- Built-in 16-bit timer (U-Timer) used as a baud-rate generator : Generates an arbitrary baud rate
- External clock is available as a transfer clock
- Error detection : parity, frame, and overrun

A/D converter (sequential transducer)

- 8/10-bit resolution, 8 channels
- Sequential comparison and transducer : At 25 MHz, 5.2 μ s
- Built-in sample and hold circuit
- Conversion mode : Selectable among single conversion, scan conversion, and repeat conversion
- Activation : Selectable among software, external trigger, and built-in timer

Reload timer

- 16-bit timer : 3 channels
- Internal clock : 2-clock cycle resolution, selectable among 2/8/32 dividing and external clock

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Other interval timers

- 16-bit timer : 3 channels (U-Timer)
- PPG timer : 4 channels
- 16-bit OCU : 4 channels, ICU : 4 channels, Free-run timer : 1 channel
- Watchdog timer: 1 channel

Flash memory 510 KB

- 510 KB FLASH ROM: Read/Write/Erase is allowed with a same power

Built-in RAM 14 KB

- D-bus RAM 12 KB, C-bus RAM 2 KB

Bit search module

- Position of a first bit that changes between “1” and “0” is searched in one cycle, within an MSB of one word.

Interrupt controller

- External interrupt input : Normal interrupt×6 (INT0 to INT5)
- Internal interrupt factors : UART, DMAC, A/D, Reload timer, UTIMER, delay interrupt, PPG, ICU, and OCU
- Priority levels are programmable (16 levels)

Reset factors

- Power-on reset/watchdog timer/software reset/external reset

Low power consumption mode

- Sleep/stop mode

Clock control

- Built-in PLL circuit, selectable among 1-multiplication, and 2-multiplication
- Gearing function : Operation clock frequencies are freely and independently specifiable for CPU and peripherals.
Gear clocks are selectable among 1/1, 1/2, 1/4, and 1/8 (or among 1/2, 1/4, 1/8, and 1/16).
Upper limit of peripheral operations is 25 MHz.

Others

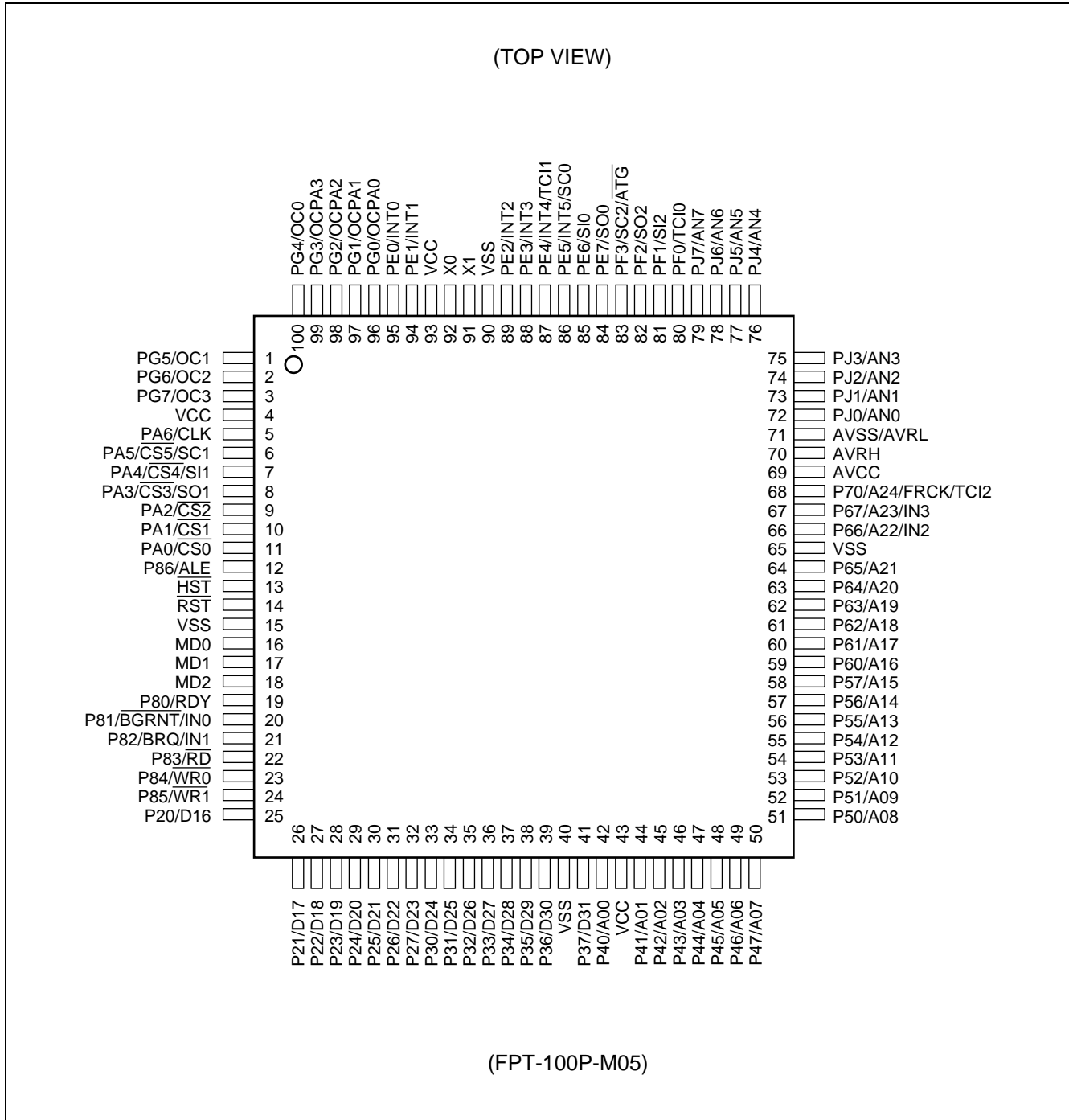
- Package : LQFP-100
- CMOS technology : 0.35 μm
- Power supply voltage : 3.3 V±0.3 V

■ SERIES CONFIGURATION

| Model name | MB91F127 | MB91F128 | MB91FV129 |
|--------------|---------------------|---------------------|--------------------|
| Outline | Quantity production | Quantity production | Evaluation product |
| FLASH memory | 256 KB | 510 KB | 510 KB |
| D-bus RAM | 12 KB | 12 KB | 16 KB |
| C-bus RAM | 2 KB | 2 KB | 2 KB |

MB91F127/F128

PIN ASSIGNMENT



■ PIN DESCRIPTION

Note that the numbers in the table are not pin numbers on a package.

| No. | Pin name | Input/output circuit type | Description |
|--|--|---------------------------|---|
| 1 2 3 4 5 6 7 8 | D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27 | D | Bit 16 through bit 23 of external data bus. The terminals are available as general I/O ports (P20 through P27) when external bus width is specified at 8 bits or in single-chip mode. |
| 9 10 11 12 13 14 15 16 | D24/P30 D25/P31 D26/P32 D27/P33 D28/P34 D29/P35 D30/P36 D31/P37 | D | Bit 24 through bit 31 of external data bus. The terminals are available as general I/O ports (P30 through P37) when the terminals are not used. |
| 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 | A00/P40 A01/P41 A02/P42 A03/P43 A04/P44 A05/P45 A06/P46 A07/P47 A08/P50 A09/P51 A10/P52 A11/P53 A12/P54 A13/P55 A14/P56 A15/P57 | D | Bit 00 through bit 15 of external address bus. The terminals are available as general I/O ports (P40 through P47 and P50 through P57) when the terminals are not used as address buses. |
| 33 34 35 36 37 38 39 40 | A16/P60 A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66/IN2 A23/P67/IN3 | D | Bit 16 through bit 23 of external address bus. The terminals are available as general I/O ports (P60 through P67) when the terminals are not used as address busses. [IN2,IN3]: Input terminals of input capture. This function is active when input capture is operating. |

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| No. | Pin name | Input/output circuit type | Description | | | | | | | | | | | | |
|--|--|---------------------------|---|-------------------------|-------------------------|------------------|------------------|------------|-------------------------|-------------------------|----------------|------------|-------------------------|----------------|----------------|
| 41 | A24/P70/FRCK/TCI2 | D | Bit 24 of external address bus. [P70] A24, FRCK and TCI2 are available as general input ports when they are not used. [FRCK] External clock input of free-run timer. This function is active when external clock input of free-run timer is used. [TCI2] External clock input of timer 2. This function is active when external clock input of timer 2 is used. | | | | | | | | | | | | |
| 42 | RDY/P80 | D | External ready input. Enter "0" when bus cycle under execution does not complete. This terminal is available as general input/output port when it is not used. | | | | | | | | | | | | |
| 43 | $\overline{\text{BGRNT}}$ /P81/IN0 | D | External bus open receive output. This terminal outputs "L" when an external bus is released. This terminal is available as general input/output port when it is not used. [IN0] Input capture input. This function is active when input capture is under input operation. | | | | | | | | | | | | |
| 44 | BRQ/P82/IN1 | D | External bus open request input. Enter "1" when releasing external bus. This terminal is available as general input/output port when it is not used. [IN1] Input capture input. This function is active when input capture is under input operation. | | | | | | | | | | | | |
| 45 | $\overline{\text{RD}}$ /P83 | D | External bus read strobe. This terminal is available as general input/output port when it is not used. | | | | | | | | | | | | |
| 46 | $\overline{\text{WR0}}$ /P84 | D | External bus write strobe. Control signals and data bus byte positions are related as the following : | | | | | | | | | | | | |
| 47 | $\overline{\text{WR1}}$ /P85 | D | <table border="1"> <thead> <tr> <th></th> <th>16-bit bus width</th> <th>8-bit bus width</th> <th>Single chip mode</th> </tr> </thead> <tbody> <tr> <td>D31 to D24</td> <td>$\overline{\text{WR0}}$</td> <td>$\overline{\text{WR0}}$</td> <td>(port allowed)</td> </tr> <tr> <td>D23 to D16</td> <td>$\overline{\text{WR1}}$</td> <td>(port allowed)</td> <td>(port allowed)</td> </tr> </tbody> </table> | | 16-bit bus width | 8-bit bus width | Single chip mode | D31 to D24 | $\overline{\text{WR0}}$ | $\overline{\text{WR0}}$ | (port allowed) | D23 to D16 | $\overline{\text{WR1}}$ | (port allowed) | (port allowed) |
| | | | | 16-bit bus width | 8-bit bus width | Single chip mode | | | | | | | | | |
| | | | D31 to D24 | $\overline{\text{WR0}}$ | $\overline{\text{WR0}}$ | (port allowed) | | | | | | | | | |
| D23 to D16 | $\overline{\text{WR1}}$ | (port allowed) | (port allowed) | | | | | | | | | | | | |
| Note : $\overline{\text{WR1}}$ is set to Hi-z during resetting. For using with 16-bit bus width, use an external pull-up resistor. [P84 or P85] Available as general input/output ports when $\overline{\text{WR0}}$ and $\overline{\text{WR1}}$ are not used. | | | | | | | | | | | | | | | |
| 48 49 50 | $\overline{\text{CS0}}$ /PA0 $\overline{\text{CS1}}$ /PA1 $\overline{\text{CS2}}$ /PA2 | D | Chip select 0 output (Low active) Chip select 1 output (Low active) Chip select 2 output (Low active) [PA0, 1, or 2] Available as general input/output ports when $\overline{\text{CS0}}$, $\overline{\text{CS1}}$ and $\overline{\text{CS2}}$ are not used. | | | | | | | | | | | | |

(Continued)

| No. | Pin name | Input/output circuit type | Description |
|--|--|---------------------------|---|
| 51 52 53 | $\overline{CS3}$ /PA3/SO1 $\overline{CS4}$ /PA4/SI1 $\overline{CS5}$ /PA5/SC1 | D | Chip select 3, 4, 5 output (Low active). [PA3,4,5] Available as general input/output ports when channel 1 of chip select UART is not used. [SO1,SI1,SC1] Data output, data input, and clock terminals of UART1. Active when UART1 operation is allowed. |
| 54 | CLK/PA6 | D | System clock output. Outputs a same clock as the same frequency of external bus operation. [PA6] Available as general input/output ports it is not used. |
| 55 56 57 58 59 60 61 62 | OCPA0/PG0 OCPA1/PG1 OCPA2/PG2 OCPA3/PG3 OC0/PG4 OC1/PG5 OC2/PG6 OC3/PG7 | D | [OCPA0 to 3] PPG timer outputs. The function is active when PPG timer output is allowed. [OC0 to 3] Output comparison output. The function is active when output comparison output is allowed. [PB0-7] Available as general input/output ports it is not used. |
| 63 64 65 | MD0 MD1 MD2 | B | Mode terminals 0 through 2. The terminals specify basic operation mode of MCU. Use the terminals by connecting them directly to VCC or VSS. |
| 66 67 | X0 X1 | A | Clock (oscillation) input. Clock (oscillation) output. |
| 68 | \overline{RST} | C | External reset input. |
| 69 | \overline{HST} | C | Hardware standby input. |
| 70 | P86/ALE | D | [ALE] Address latch signal output. The function is active when ALE output of EPCR is allowed. |
| 71 72 | INT0/PE0 INT1/PE1 INT2/PE2 INT3/PE3 | D | [INT0,1,2,3] External interrupt request inputs. The input is used whenever necessary if external interrupt is allowed. Output of other functions must be suspended if not on purpose. [PE0,1,2,3] General input/output port |
| 75 76 | INT4/PE4/TC11 INT5/PE5/SC0 | D | [INT4,5] External interrupt request inputs. The input is used whenever necessary if concerned external interrupt is allowed. Output of other functions must be suspended if not on purpose. [TC11] External clock input of timer 1. [SC0] Clock input of UART0. [PE4,5] General input/output port |
| 77 | SI0/PE6 | D | [SI0] Data input of UART0. This function is active when data input of UART0 is allowed. [PE6] General input/output port |
| 78 | SO0/PE7 | D | [SO0] Data output of UART0. This function is active when data output of UART0 is allowed. [PE7] General input/output port |

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| No. | Pin name | Input/output circuit type | Description |
|-----------|--|---------------------------|---|
| 79 | PF0/TCI0 | D | [TCI0] External clock input of timer 0. |
| | | | [PF0] General input/output port |
| 80 | SI2/PF1 | D | [SI2] Data input of UART2. This function is active when data input of UART2 is allowed. |
| | | | [PF1] General input/output port |
| 81 | SO2/PF2 | D | [SO2] Data output of UART2. This function is active when data output of UART2 is allowed. |
| | | | [PF2] General input/output port. This function is active when data output of UART2 is disallowed. |
| 82 | SC2/PF3/ $\overline{\text{ATG}}$ | D | [SC2] Clock input of UART2 [$\overline{\text{ATG}}$] External trigger input of A/D converter. The input is used whenever necessary if a function concerned is selected. Output of other functions must be suspended if not on purpose. |
| | | | [PF3] General input/output port |
| 83 to 90 | AN0/PJ0 AN1/PJ1 AN2/PJ2 AN3/PJ3 AN4/PJ4 AN5/PJ5 AN6/PJ6 AN7/PJ7 | E | [AN0 to AN7] Analog input of A/D converter. This function is active when analog input is specified in AIC register. |
| | | | [PJ0 through PJ7] General input/output ports |
| 91 | AVCC | — | VCC power supply for A/D converter |
| 92 | AVRH | — | Reference voltage of A/D converter (high potential side). Be sure to turn on or off this terminal with a potential higher than AVRH applied to VCC. |
| 93 | AVSS/AVRL | — | A/D converter VSS power source and reference voltage (low potential side). |
| 94 to 96 | VCC | — | Power sources of digital circuits. Be sure to connect power source to all terminals when the device is used. |
| 97 to 100 | VSS | — | Ground level of digital circuits. |

Note : Most of the above terminals multiplex inputs and outputs of I/O ports and resources, as indicated as “XXXX/PXX”. If the outputs of ports and resources conflict with each other on the terminals, resources take preferences.

■ INPUT/OUTPUT CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|--|
| A | | <ul style="list-style-type: none"> • For 25 MHz system • Oscillation feedback register : Approx. 1MΩ • Standby control is available. |
| B | | <ul style="list-style-type: none"> • CMOS level input • High-voltage control is available for FLASH test. |
| C | | <ul style="list-style-type: none"> • CMOS level hysteresis input • Standby control is not available. |
| D | | <ul style="list-style-type: none"> • CMOS level output • CMOS level hysteresis input • Standby control is available |
| E | | <ul style="list-style-type: none"> • Standby control is available • CMOS level output • CMOS level hysteresis input • Analog input |

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■ HANDLING DEVICES

1. Preventing latch up

On a CMOS IC, latch up may occur when a voltage higher than VCC or a voltage lower than VSS is applied to input terminal or output terminal, or when a voltage exceeding rated level is applied across VCC and VSS. Latch up causes drastic increase of power source current, which may result in destruction of the element by heat. Take extra care not to exceed maximum rating in use. Also, take extra care so that analog terminal does not exceed digital power source.

2. Treatment of unused input terminals

Leaving unused terminals open may cause malfunction. Apply pull-up or pull-down treatment on unused terminals.

3. External reset input

Complete resetting of internal system requires inputting "L" level signal to $\overline{\text{RST}}$ terminal for a minimum of 5 machine cycles.

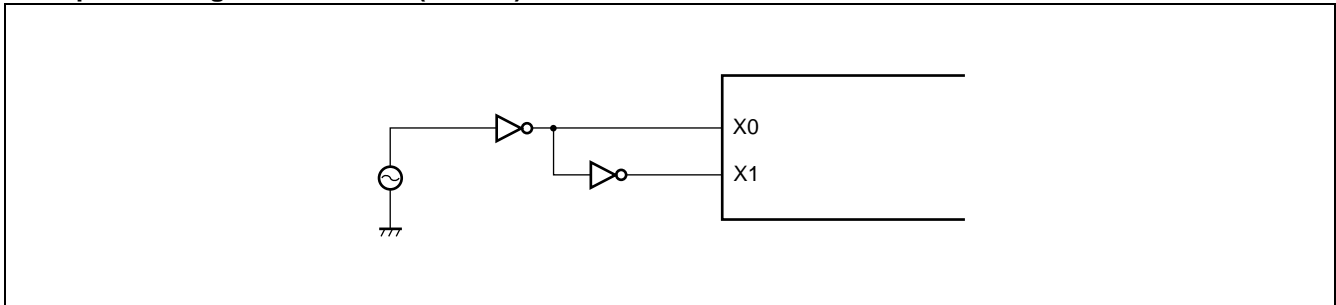
4. Notes on using external clock

When using an external clock, supply a clock signal to X0 terminal and supply its antiphase clock to X1 terminal simultaneously. In this case, do not use STOP mode (oscillation stop mode). (Because X1 terminal halts with "H" output under STOP status.)

Under a 12.5 MHz frequency, the device operates with a clock supplied to X0 terminal only.

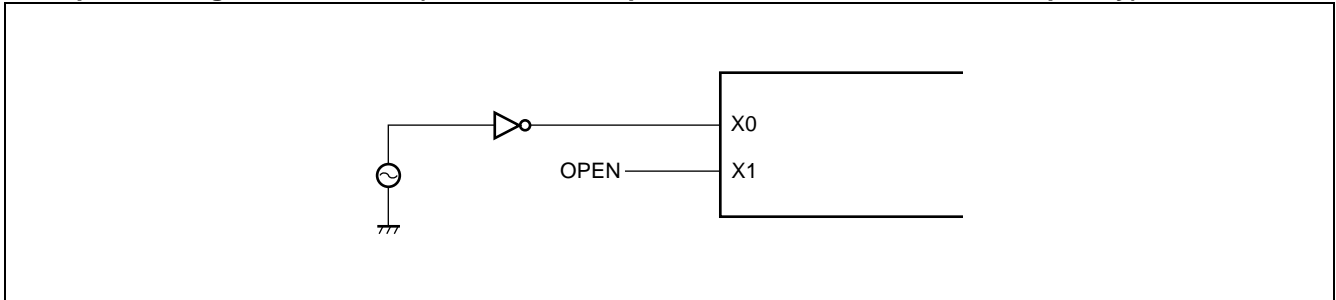
Figures show examples of using an external clock.

Example of using external clock (normal)



Note : STOP mode (oscillation stop mode) is not available.

Example of using external clock (allowed under operation at 12.5 MHz or lower frequency)



5. Connecting power supply terminals (VCC, VSS)

If two or more VCC, VSS terminals are used, the terminals to be placed under the same potentials are connected with each other internally for preventing malfunctions such as latch up. However, for reducing unwanted radiation, preventing malfunctions of strobe signals and observing total power and current ratings, be sure to connect all of these terminals to power supply and ground externally.

Connecting power supply to VCC - VSS in impedance as low as possible is desirable.

6. Crystal oscillator circuit

Noises around X0 and X1 terminals causes malfunction of the device. Design printed wiring so that X0, X1, and crystal oscillator (or ceramic oscillator), and bypass capacitor to the ground are aligned as close as possible one another. Also the wiring of those elements should not cross with other wiring if possible. Printed wiring with ground wires around X0 and X1 terminals ensures more stable operations. Such designing is strongly recommended.

7. Treating NC terminals

Be sure to leave NC terminals open.

8. Mode terminals (MD0 through MD2)

Do not connect the mode terminals directly to VCC or VSS.

For preventing malfunctions caused by noises, make printed traces between the mode terminals and VCC or VSS as short as possible, and connect the elements in lower impedance.

9. Turning power on

Be sure to turn on the power of the device with $\overline{\text{RST}}$ terminal placed under "L" level. Ensure a period at a minimum of 5 cycles of internal operation clock before placing the terminal under "H" level.

10. Terminal status upon turning on power

Status upon turning on the power is indefinite. Upon turning on the power, oscillation starts and the circuit is initialized.

11. Oscillation input upon turning on power

Upon turning on the power, be sure to input a clock signal until oscillation stabilizing wait status is released.

12. Initializing power-on reset

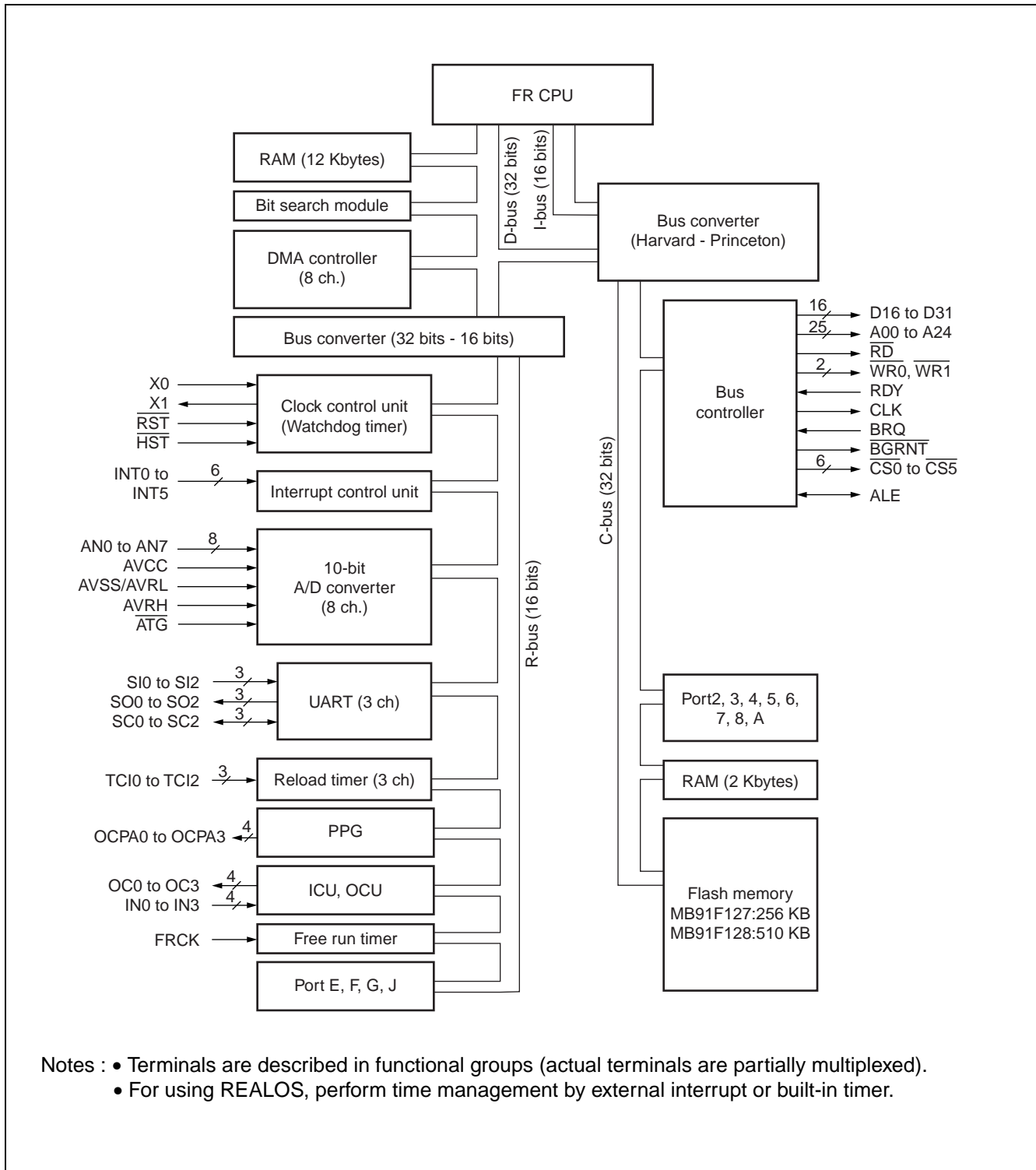
The device includes some built-in registers that are initialized only with power-on reset operation. For initializing the registers, perform power-on reset by turning on the power again.

13. Recovery from Sleep/Stop status

For recovering from Sleep/Stop status initiated by a program in C-Bus RAM, reset the device instead of recovering by an interrupt process.

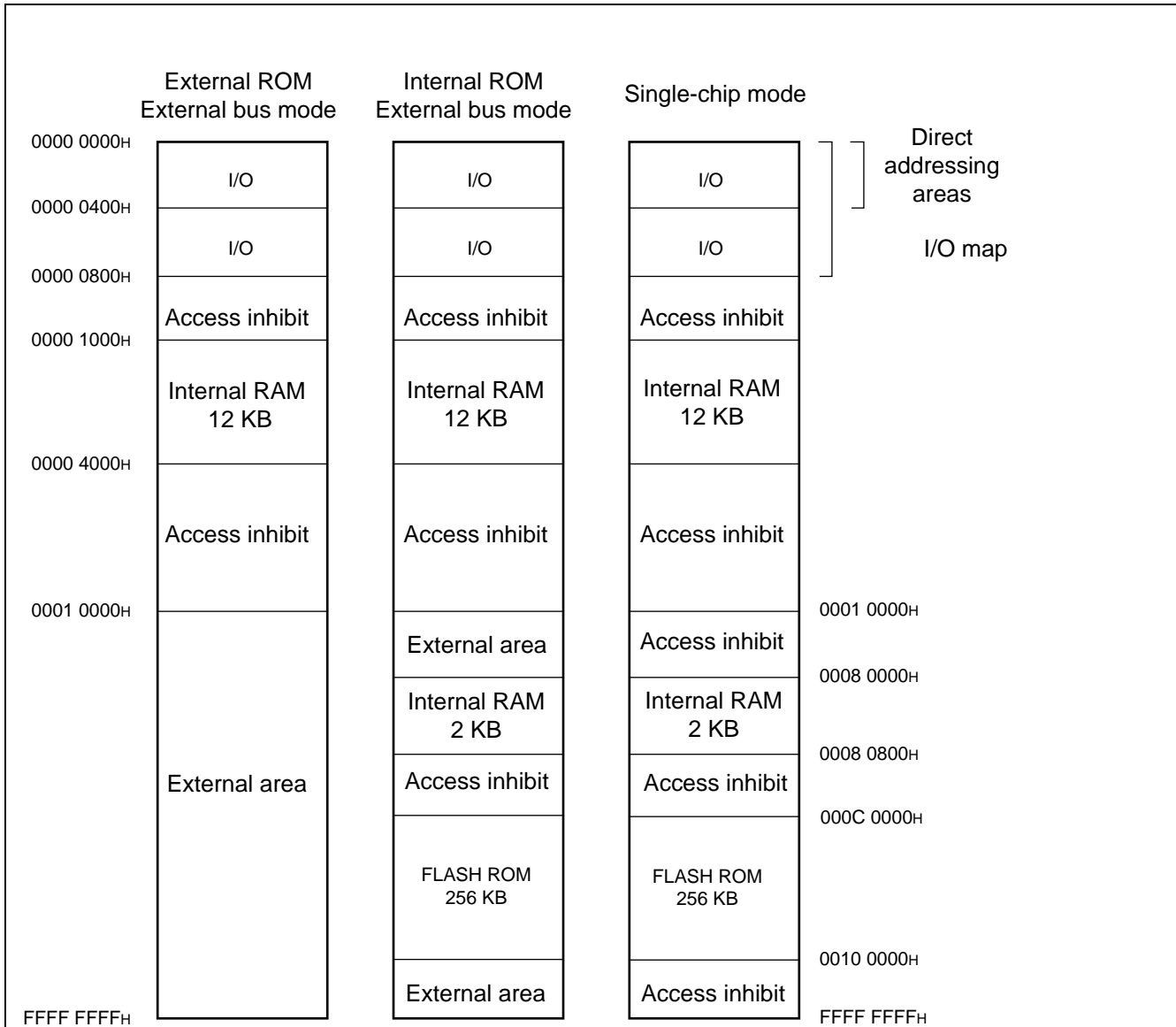
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■ BLOCK DIAGRAM



■ CPU CORE MEMORY SPACE

• MB91F127



Note : External area is not accessible in single-chip mode. When accessing to external areas, select the internal ROM external bus mode in mode register.

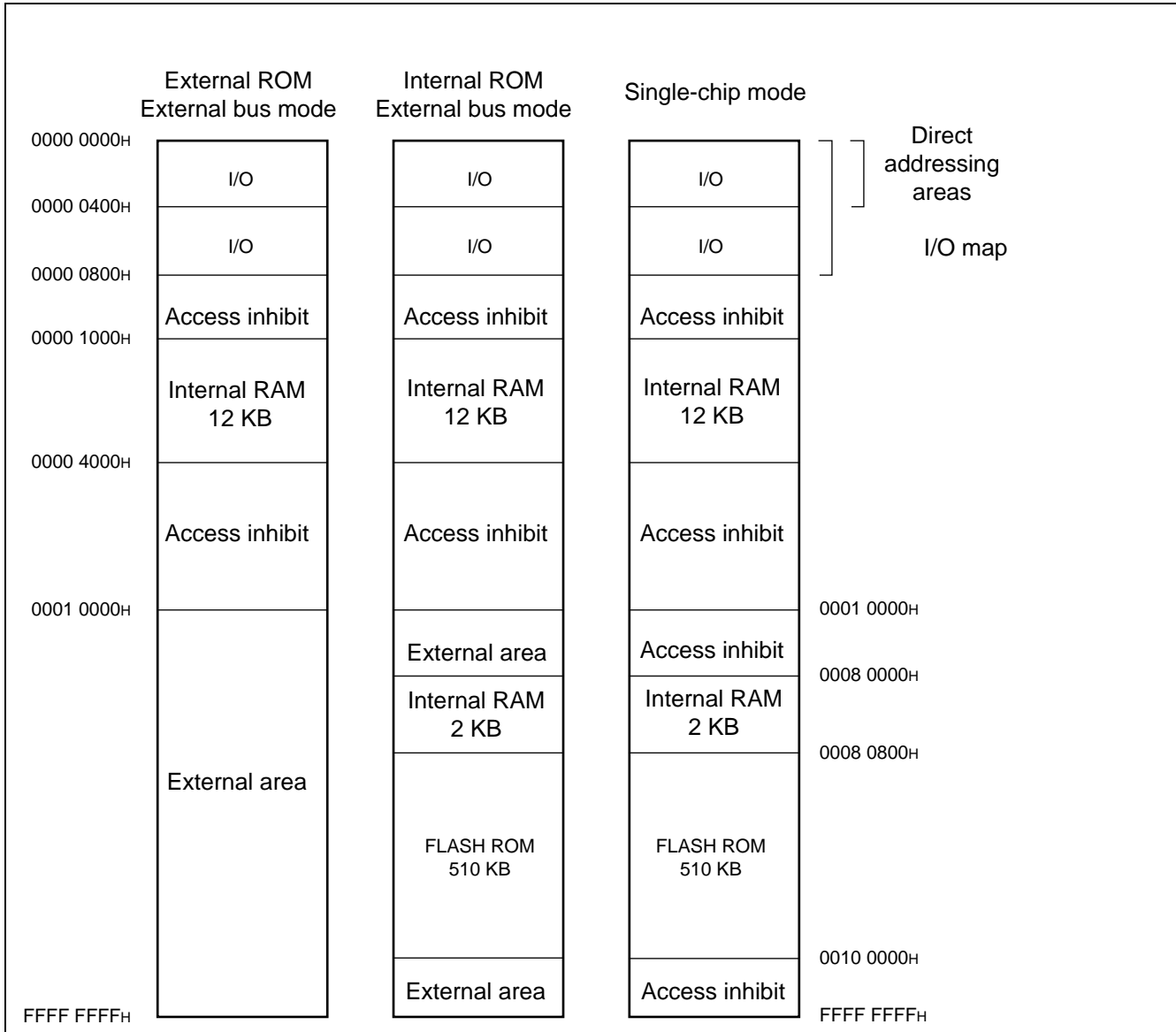
Direct addressing areas

The areas described below are used for I/O processes. The areas, referred to as “direct addressing areas,” allow specifying an operand address directly by an instruction. The direct addressing areas varies as the following, depending on size of the data to be accessed.

- Byte-data access : 0 to 0FF_H
- Half-word data access : 0 to 1FF_H
- Word-data access : 0 to 3FF_H

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• MB91F128



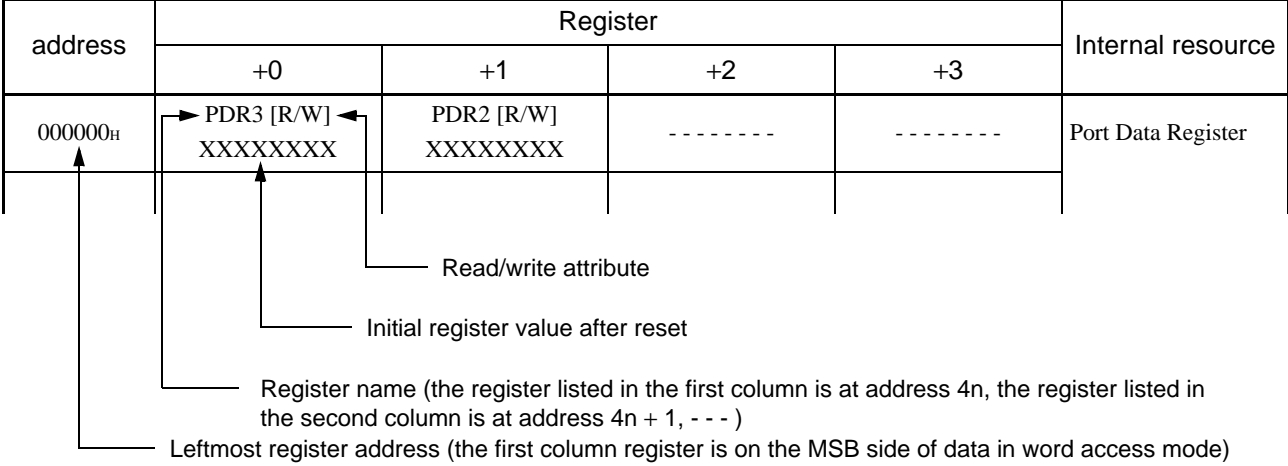
Note : External area is not accessible in single-chip mode. When accessing to external areas, select the internal ROM external bus mode in mode register.

Direct addressing areas

The areas described below are used for I/O processes. The areas, referred to as “direct addressing areas,” allow specifying an operand address directly by an instruction. The direct addressing areas varies as the following, depending on size of the data to be accessed.

- Byte-data access : 0 to 0FF_H
- Half-word data access : 0 to 1FF_H
- Word-data access : 0 to 3FF_H

■ LEGEND OF I/O MAP



Note : Register bit values indicate initial values as shown below :

- “1” : Initial value “1”
- “0” : Initial value “0”
- “X” : Initial value “X”
- “-” : Register does not exist physically in this position.

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■ I/O MAP

| Address | Register | | | | Internal resource |
|---------------------|--------------------------------|------------------------|-----------------------------------|---------------------------|---|
| | +0 | +1 | +2 | +3 | |
| 000000 _H | PDR3 [R/W] XXXXXXXX | PDR2 [R/W] XXXXXXXX | — | — | Port data Register |
| 000004 _H | PDR7 [R/W] -----X | PDR6 [R/W] XXXXXXXX | PDR5 [R/W] XXXXXXXX | PDR4 [R/W] XXXXXXXX | |
| 000008 _H | — | PDRA [R/W] XXXXXXXX | — | PDR8[R/W] --XXXXXX | |
| 00000C _H | — | | | | |
| 000010 _H | — | — | PDRE [R/W] XXXXXXXX | PDRF [R/W] XXXXXXXX | |
| 000014 _H | PDRG [R/W] XXXXXXXX | — | — | PDRJ [R/W] XXXXXXXX | |
| 000018 _H | — | — | — | — | Reserved |
| 00001C _H | SSR [R/W] 00001- 00 | SIDR [R/W] XXXXXXXX | SCR [R/W] 00000100 | SMR [R/W] 00 -- 0 - 00 | UART0 |
| 000020 _H | SSR [R/W] 00001- 00 | SIDR [R/W] XXXXXXXX | SCR [R/W] 00000100 | SMR [R/W] 00 -- 0 - 00 | UART1 |
| 000024 _H | SSR [R/W] 00001- 00 | SIDR [R/W] XXXXXXXX | SCR [R/W] 00000100 | SMR [R/W] 00 -- 0 - 00 | UART2 |
| 000028 _H | TMRLR [W] XXXXXXXX XXXXXXXX | | TMR [W] XXXXXXXX XXXXXXXX | | Reload Timer 0 |
| 00002C _H | — | | TMCSR [R/W] ---- 0000 00000000 | | |
| 000030 _H | TMRLR [W] XXXXXXXX XXXXXXXX | | TMR [W] XXXXXXXX XXXXXXXX | | Reload Timer 1 |
| 000034 _H | — | | TMCSR [R/W] ---- 0000 00000000 | | |
| 000038 _H | — | | — | | Reserved |
| 00003C _H | TMRLR [W] XXXXXXXX XXXXXXXX | | TMR [W] XXXXXXXX XXXXXXXX | | Reload Timer 2 |
| 000040 _H | — | | TMCSR [R/W] ---- 0000 00000000 | | |
| 000044 _H | IPCP1[R] XXXXXXXX XXXXXXXX | | IPCP0[R] XXXXXXXX XXXXXXXX | | 16 bit ICU |
| 000048 _H | IPCP3[R] XXXXXXXX XXXXXXXX | | IPCP2[R] XXXXXXXX XXXXXXXX | | |
| 00004C _H | — | ICS23[R/W] 00000000 | — | ICS01[R/W] 00000000 | |
| 000050 _H | ADCR [W] 00101-XX XXXXXXXX | | ADCS [R/W] 00000000 00000000 | | A/D converter (Serially com- pared) |

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| Address | Register | | | | Internal resource |
|---------------------|--------------------------------------|------------------------|------------------------------------|---------------------------|----------------------------|
| | +0 | +1 | +2 | +3 | |
| 000054 _H | OCCP1[R/W] XXXXXXXX XXXXXXXX | | OCCP0[R/W] XXXXXXXX XXXXXXXX | | 16 bit OCU |
| 000058 _H | OCCP3[R/W] XXXXXXXX XXXXXXXX | | OCCP2[R/W] XXXXXXXX XXXXXXXX | | |
| 00005C _H | — | | — | | Reserved |
| 000060 _H | — | | — | | |
| 000064 _H | OCS2, 3[R/W] XXX00000 0000XX00 | | OCS0, 1[R/W] XXX00000 0000XX00 | | 16 bit OCU |
| 000068 _H | — | | — | | Reserved |
| 00006C _H | TCDT [R/W] 00000000 00000000 | | TCCS [R/W] 0 - - - - - 00000000 | | Free run timer |
| 000070 _H | — | | — | | Reserved |
| 000074 _H | — | | — | | Reserved |
| 000078 _H | UTM/UTIMR [R/W] 00000000 00000000 | | — | UTIMC[R/W] 0 - - 00001 | U-Timer0 |
| 00007C _H | UTM/UTIMR [R/W] 00000000 00000000 | | — | UTIMC[R/W] 0 - - 00001 | U-Timer1 |
| 000080 _H | UTM/UTIMR [R/W] 00000000 00000000 | | — | UTIMC[R/W] 0 - - 00001 | U-Timer2 |
| 000084 _H | — | | — | | Reserved |
| 000088 _H | — | | — | | |
| 00008C _H | — | | — | | Reserved |
| 000090 _H | — | | — | | |
| 000094 _H | EIRR [R/W] 00000000 | ENIR [R/W] 00000000 | — | | External interrupt/ NMI |
| 000098 _H | EHVR [R/W] - - - - 0000 | ELVR [R/W] 00000000 | — | | |

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| Address | Register | | | | Internal resource |
|---------------------|---------------------------------|---------------------|--------------------------------|------------------------|-------------------------|
| | +0 | +1 | +2 | +3 | |
| 00009C _H | — | | | | Reserved |
| 0000A0 _H | — | | | | |
| 0000A4 _H | — | | | | |
| 0000A8 _H | — | | | | |
| 0000AC _H | — | | | | |
| 0000B0 _H | — | | | | |
| 0000B4 _H | — | | | | |
| 0000B8 _H | — | | | | |
| 0000BC _H | — | | | | |
| 0000C0 _H | — | | | | |
| 0000C4 _H | — | | | | |
| 0000C8 _H | — | | | | |
| 0000CC _H | — | | | | |
| 0000D0 _H | — | — | DDRE [W] 00000000 | DDRF [W] 00000000 | Port direction register |
| 0000D4 _H | — | AIC3[W] 11111111 | — | — | A/D converter |
| 0000D8 _H | DDRG [W] 00000000 | — | — | DDRJ [W] 00000000 | Port direction register |
| 0000DC _H | GCN1 [R/W] 00110010 00010000 | | ----- | GCN2[R/W] 00000000 | PPG ctl |
| 0000E0 _H | PTMR0 [R] 11111111 11111111 | | PCSR0 [W] XXXXXXXX XXXXXXXX | | PPG0 |
| 0000E4 _H | PDUT0 [W] XXXXXXXX XXXXXXXX | | PCNH0[R/W] 0000000 - | PCNL0[R/W] 00000000 | |
| 0000E8 _H | PTMR1 [R] 11111111 11111111 | | PCSR1 [W] XXXXXXXX XXXXXXXX | | PPG1 |
| 0000EC _H | PDUT1 [W] XXXXXXXX XXXXXXXX | | PCNH1[R/W] 0000000 - | PCNL1[R/W] 00000000 | |
| 0000F0 _H | PTMR2 [R] 11111111 11111111 | | PCSR2 [W] XXXXXXXX XXXXXXXX | | PPG2 |
| 0000F4 _H | PDUT2 [W] XXXXXXXX XXXXXXXX | | PCNH2[R/W] 0000000 - | PCNL2[R/W] 00000000 | |
| 0000F8 _H | PTMR3 [R] 11111111 11111111 | | PCSR3 [W] XXXXXXXX XXXXXXXX | | PPG3 |
| 0000FC _H | PDUT3 [W] XXXXXXXX XXXXXXXX | | PCNH3[R/W] 0000000 - | PCNL3[R/W] 00000000 | |

(Continued)

| Address | Register | | | | Internal resource |
|--|--|----|----|----|-------------------|
| | +0 | +1 | +2 | +3 | |
| 000100 _H to 0001FC _H | — | | | | Reserved |
| 000200 _H | DPDP [R/W] ----- -0000000 | | | | DMAC |
| 000204 _H | DACSR [R/W] 00000000 00000000 00000000 00000000 | | | | |
| 000208 _H | DATCR [R/W] ----- --XX0000 --XX0000 --XX0000 | | | | |
| 00020C _H | — | | | | |
| 000210 _H to 0002FC _H | — | | | | Reserved |
| 000300 _H to 0003EC _H | — | | | | Reserved |
| 0003F0 _H | BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | Bit search module |
| 0003F4 _H | BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0003F8 _H | BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |
| 0003FC _H | BSRR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX | | | | |

(Continued)

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| Address | Register | | | | Internal resource |
|--|----------------------------------|------------------------|-------------------------|------------------------|---------------------------|
| | +0 | +1 | +2 | +3 | |
| 000400 _H | ICR00 [R/W] ---11111 | ICR01[R/W] ---11111 | ICR02[R/W] ---11111 | ICR03[R/W] ---11111 | Interrupt controller |
| 000404 _H | ICR04[R/W] ---11111 | ICR05[R/W] ---11111 | ICR06[R/W] ---11111 | ICR07[R/W] ---11111 | |
| 000408 _H | ICR08 [R/W] ---11111 | ICR09[R/W] ---11111 | ICR10[R/W] ---11111 | ICR11[R/W] ---11111 | |
| 00040C _H | ICR12[R/W] ---11111 | ICR13[R/W] ---11111 | ICR14[R/W] ---11111 | ICR15[R/W] ---11111 | |
| 000410 _H | ICR16[R/W] ---11111 | ICR17[R/W] ---11111 | ICR18[R/W] ---11111 | ICR19[R/W] ---11111 | |
| 000414 _H | ICR20[R/W] ---11111 | ICR21[R/W] ---11111 | ICR22[R/W] ---11111 | ICR23[R/W] ---11111 | |
| 000418 _H | ICR24 [R/W] ---11111 | ICR25[R/W] ---11111 | ICR26[R/W] ---11111 | ICR27[R/W] ---11111 | |
| 00041C _H | ICR28[R/W] ---11111 | ICR29[R/W] ---11111 | ICR30[R/W] ---11111 | ICR31[R/W] ---11111 | |
| 000420 _H | ICR32[R/W] ---11111 | ICR33[R/W] ---11111 | ICR34[R/W] ---11111 | ICR35[R/W] ---11111 | |
| 000424 _H | ICR36[R/W] ---11111 | ICR37[R/W] ---11111 | ICR38[R/W] ---11111 | ICR39[R/W] ---11111 | |
| 000428 _H | ICR40[R/W] ---11111 | ICR41[R/W] ---11111 | ICR42[R/W] ---11111 | ICR43[R/W] ---11111 | |
| 00042C _H | ICR44[R/W] ---11111 | ICR45[R/W] ---11111 | ICR46[R/W] ---11111 | ICR47[R/W] ---11111 | |
| 000430 _H | DICR [R/W] -----0 | HRCL [R/W] ---11111 | — | — | Delay interrupt |
| 000434 _H to 00047C _H | — | | | | Reserved |
| 000480 _H | RSRR/WTCR [R/W] 1XXXX - 00 | STCR [R/W] 000111-- | PDDR [R/W] ---- 0000 | CTBR [W] XXXXXXXX | Clock controller block |
| 000484 _H | GCR [R/W] 110011 - 1 | WPR [W] XXXXXXXX | — | — | |
| 000488 _H | PTCR [R/W] 00 -- 0 --- | — | | | PLL controller block |
| 00048C _H to 0005FC _H | — | | | | Reserved |

(Continued)

(Continued)

| Address | Register | | | | Internal resource |
|--|----------------------------------|------------------------|----------------------------------|------------------------|--------------------------------------|
| | +0 | +1 | +2 | +3 | |
| 000600 _H | DDR3 [W] 00000000 | DDR2 [W] 00000000 | — | — | Data direction register |
| 000604 _H | DDR7 [W] -----0 | DDR6 [W] 00000000 | DDR5 [W] 00000000 | DDR4 [W] 00000000 | |
| 000608 _H | — | DDRA [W] -0000000 | — | DDR8 [W] --000000 | |
| 00060C _H | ASR1 [W] 00000000 00000001 | | AMR1 [W] 00000000 00000000 | | External bus interface |
| 000610 _H | ASR2 [W] 00000000 00000010 | | AMR2 [W] 00000000 00000000 | | |
| 000614 _H | ASR3 [W] 00000000 00000011 | | AMR3 [W] 00000000 00000000 | | |
| 000618 _H | ASR4 [W] 00000000 00000100 | | AMR4 [W] 00000000 00000000 | | |
| 00061C _H | ASR5 [W] 00000000 00000101 | | AMR5 [W] 00000000 00000000 | | |
| 000620 _H | AMD0 [R/W] ---XX111 | AMD1 [R/W] 0--00000 | AMD32[R/W] 00000000 | AMD4 [R/W] 0--00000 | |
| 000624 _H | AMD5[R/W] 0--00000 | DSCR [W] 00000000 | RFCR [R/W] --XXXXXX 00---000 | | |
| 000628 _H | EPCR0 [W] --1-1100 -1111111 | | EPCR1 [W] -----1 11111111 | | |
| 00062C _H | DMCR4 [R/W] 00000000 0000000- | | DMCR5 [R/W] 00000000 0000000- | | |
| 000630 _H to 0007BC _H | — | | | | |
| 0007C0 _H | FSTR [R/W] 000XXXX0 | — | — | — | Flash memory |
| 0007C4 _H to 0007F8 _H | — | | | | Reserved |
| 0007FC _H | — | — | LER [W] -----000 | MODR [W] XXXXXXXX | Little endian register mode register |

Note : Do not issue RMW instructions to a register with write-only bit.

RMW instructions (RMW : Read modify write)

AND Rj, @Ri OR Rj, @Ri EOR Rj, @Ri

ANDH Rj, @Ri ORH Rj, @Ri EORH Rj, @Ri

ANDB Rj, @Ri ORB Rj, @Ri EORB Rj, @Ri

BANDL #u4, @Ri BORL #u4, @Ri BEORL #u4, @Ri

BANDH #u4, @Ri BORH #u4, @Ri BEORH #u4, @Ri

Data in "Reserved" or "-" area is indefinite.

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■ INTERRUPT CAUSES, INTERRUPT VECTORS AND INTERRUPT CONTROL REGISTER ALLOCATIONS

| Interrupt causes | Interrupt number | | Interrupt level | | TBR default Address*2 |
|---------------------------------|------------------|-------------|-------------------------------|------------------|-----------------------|
| | Decimal | Hexadecimal | Register*1 | Offset | |
| Reset | 0 | 00 | — | 3FC _H | 000FFFFC _H |
| Reserved by system | 1 | 01 | — | 3F8 _H | 000FFFF8 _H |
| Reserved by system | 2 | 02 | — | 3F4 _H | 000FFFF4 _H |
| Reserved by system | 3 | 03 | — | 3F0 _H | 000FFFF0 _H |
| Reserved by system | 4 | 04 | — | 3EC _H | 000FFFE _C |
| Reserved by system | 5 | 05 | — | 3E8 _H | 000FFFE8 _H |
| Reserved by system | 6 | 06 | — | 3E4 _H | 000FFFE4 _H |
| Reserved by system | 7 | 07 | — | 3E0 _H | 000FFFE0 _H |
| Reserved by system | 8 | 08 | — | 3DC _H | 000FFFD _C |
| Reserved by system | 9 | 09 | — | 3D8 _H | 000FFFD8 _H |
| Reserved by system | 10 | 0A | — | 3D4 _H | 000FFFD4 _H |
| Reserved by system | 11 | 0B | — | 3D0 _H | 000FFFD0 _H |
| Reserved by system | 12 | 0C | — | 3CC _H | 000FFFCC _H |
| Reserved by system | 13 | 0D | — | 3C8 _H | 000FFFC8 _H |
| Undefined instruction exception | 14 | 0E | — | 3C4 _H | 000FFFC4 _H |
| NMI request | 15 | 0F | 15 (F _H) fixed | 3C0 _H | 000FFFC0 _H |
| External interrupt 0 | 16 | 10 | ICR00 | 3BC _H | 000FFFBC _H |
| External interrupt 1 | 17 | 11 | ICR01 | 3B8 _H | 000FFF8 _H |
| External interrupt 2 | 18 | 12 | ICR02 | 3B4 _H | 000FFF4 _H |
| External interrupt 3 | 19 | 13 | ICR03 | 3B0 _H | 000FFF0 _H |
| UART 0 reception complete | 20 | 14 | ICR04 | 3AC _H | 000FFFA _C |
| UART 1 reception complete | 21 | 15 | ICR05 | 3A8 _H | 000FFFA8 _H |
| UART 2 reception complete | 22 | 16 | ICR06 | 3A4 _H | 000FFFA4 _H |
| UART 0 transmission complete | 23 | 17 | ICR07 | 3A0 _H | 000FFFA0 _H |
| UART 1 transmission complete | 24 | 18 | ICR08 | 39C _H | 000FFF9C _H |
| UART 2 transmission complete | 25 | 19 | ICR09 | 398 _H | 000FFF98 _H |

(Continued)

| Interrupt causes | Interrupt number | | Interrupt level | | TBR default Address*2 |
|-----------------------|------------------|-------------|-----------------|------------------|-----------------------|
| | Decimal | Hexadecimal | Register*1 | Offset | |
| DMAC 0 (end, error) | 26 | 1A | ICR10 | 394 _H | 000FFF94 _H |
| DMAC 1 (end, erro) | 27 | 1B | ICR11 | 390 _H | 000FFF90 _H |
| DMAC 2 (end, erro) | 28 | 1C | ICR12 | 38C _H | 000FFF8C _H |
| DMAC 3 (end, erro) | 29 | 1D | ICR13 | 388 _H | 000FFF88 _H |
| DMAC 4 (end, erro) | 30 | 1E | ICR14 | 384 _H | 000FFF84 _H |
| DMAC 5 (end, erro) | 31 | 1F | ICR15 | 380 _H | 000FFF80 _H |
| DMAC 6 (end, erro) | 32 | 20 | ICR16 | 37C _H | 000FFF7C _H |
| DMAC 7 (end, erro) | 33 | 21 | ICR17 | 378 _H | 000FFF78 _H |
| A/D (sequential type) | 34 | 22 | ICR18 | 374 _H | 000FFF74 _H |
| Reload timer 0 | 35 | 23 | ICR19 | 370 _H | 000FFF70 _H |
| Reload timer 1 | 36 | 24 | ICR20 | 36C _H | 000FFF6C _H |
| Reload timer 2 | 37 | 25 | ICR21 | 368 _H | 000FFF68 _H |
| External interrupt 4 | 38 | 26 | ICR22 | 364 _H | 000FFF64 _H |
| External interrupt 5 | 39 | 27 | ICR23 | 360 _H | 000FFF60 _H |
| Reserved by system | 40 | 28 | ICR24 | 35C _H | 000FFF5C _H |
| Reserved by system | 41 | 29 | ICR25 | 358 _H | 000FFF58 _H |
| U-TIMER 0 | 42 | 2A | ICR26 | 354 _H | 000FFF54 _H |
| U-TIMER 1 | 43 | 2B | ICR27 | 350 _H | 000FFF50 _H |
| U-TIMER 2 | 44 | 2C | ICR28 | 34C _H | 000FFF4C _H |
| FLASH memory | 45 | 2D | ICR29 | 348 _H | 000FFF48 _H |
| Reserved by system | 46 | 2E | ICR30 | 344 _H | 000FFF44 _H |
| Reserved by system | 47 | 2F | ICR31 | 340 _H | 000FFF40 _H |
| PPG0 | 48 | 30 | ICR32 | 33C _H | 000FFF3C _H |
| PPG1 | 49 | 31 | ICR33 | 338 _H | 000FFF38 _H |
| PPG2 | 50 | 32 | ICR34 | 334 _H | 000FFF34 _H |
| PPG3 | 51 | 33 | ICR35 | 330 _H | 000FFF30 _H |
| ICU0 (capture) | 52 | 34 | ICR36 | 32C _H | 000FFF2C _H |
| ICU1 (capture) | 53 | 35 | ICR37 | 328 _H | 000FFF28 _H |
| ICU2 (capture) | 54 | 36 | ICR38 | 324 _H | 000FFF24 _H |
| ICU3 (capture) | 55 | 37 | ICR39 | 320 _H | 000FFF20 _H |

(Continued)

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(Continued)

| Interrupt causes | Interrupt number | | Interrupt level | | TBR default Address*2 |
|---|------------------|----------------|-----------------|--|---|
| | Decimal | Hexadecimal | Register*1 | Offset | |
| OCU0 (match) | 56 | 38 | ICR40 | 31C _H | 000FFF1C _H |
| OCU1 (match) | 57 | 39 | ICR41 | 318 _H | 000FFF18 _H |
| OCU2 (match) | 58 | 3A | ICR42 | 314 _H | 000FFF14 _H |
| OCU3 (match) | 59 | 3B | ICR43 | 310 _H | 000FFF10 _H |
| Reserved by system | 60 | 3C | ICR44 | 30C _H | 000FFF0C _H |
| 16 bit free-run timer | 61 | 3D | ICR45 | 308 _H | 000FFF08 _H |
| Reserved by system | 62 | 3E | ICR46 | 304 _H | 000FFF04 _H |
| Delay interrupt cause bit | 63 | 3F | ICR47 | 300 _H | 000FFF00 _H |
| Reserved by system (used by REALOS) *3 | 64 | 40 | — | 2FC _H | 000FFEFC _H |
| Reserved by system (used by REALOS) *3 | 65 | 41 | — | 2F8 _H | 000FFE8 _H |
| Used by INT | 66 to 255 | 42 to FF | — | 2F4 _H to 000 _H | 000FEF4 _H to 000FFC00 _H |

*1 : ICR specifies interrupt levels for interrupt requests, using the registers in interrupt controller.
ICR is provided for each interrupt request.

*2 : TBR is a register that indicates a head address of the vector table for EIT.
An address that is found by adding offset values defined by TBR and EIT cause, is a vector address.

*3 : If REALOS/FR is used, 0x40 and 0x41 interrupts are used for system code.

Information : An 1 Kbyte area starting with an address indicated by TBR is the vector area for EIT. Size of the area for one vector is 4 byte. Relation between a vector number and a vector address is as follows:

$$\begin{aligned} \text{vctadr} &= \text{TBR} + \text{vctofs} \\ &= \text{TBR} + (3\text{FC}_{\text{H}} - 4 \times \text{vct}) \end{aligned}$$

Vctadr Vector address, vctofs: Vector offset, vct: Vector number

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|----------------------|----------------|-----------------|------|---------|
| | | Min | Max | | |
| Power supply voltage | V_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | |
| Analog supply voltage | AV_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | *1 |
| Analog reference voltage | $AVRH$ | $V_{SS} - 0.3$ | $V_{SS} + 4.0$ | V | *1 |
| Input voltage | V_I | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| Analog input voltage | V_{IA} | $V_{SS} - 0.3$ | $AV_{CC} + 0.3$ | V | |
| Output voltage | V_O | $V_{SS} - 0.3$ | $V_{CC} + 0.3$ | V | |
| Maximum clamp current | I_{CLAMP} | -2.0 | +2.0 | mA | *5 |
| Total maximum clamp current | $\Sigma I_{CLAMP} $ | — | 20 | mA | *5 |
| “L” level maximum output current | I_{OL} | — | 10 | mA | *2 |
| “L” level average output current | I_{OLAV} | — | 4 | mA | *3 |
| “L” level maximum total output current | ΣI_{OL} | — | 100 | mA | |
| “L” level average total output current | ΣI_{OLAV} | — | 50 | mA | *4 |
| “H” level maximum output current | I_{OH} | — | -10 | mA | *2 |
| “H” level average output current | I_{OHAV} | — | -4 | mA | *3 |
| “H” level maximum total output current | ΣI_{OH} | — | -50 | mA | |
| “H” level average total output current | ΣI_{OHAV} | — | -20 | mA | *4 |
| Power consumption | P_d | — | 500 | mW | |
| Operating temperature | T_A | -30 | +70 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

*1 : Care must be taken that AV_{CC} , $AVRH$ do not exceed $V_{CC} + 0.3\text{ V}$. Also, care must be taken that $AVRH$ do not exceed AV_{CC} .

*2 : Maximum output current defines a peak value of a specific terminal.

*3 : Average output current defines a mean value of current flow within a period of 100 ms in a specific terminal.

*4 : Average total output current defines a mean value of current flow within a period of 100 ms in all terminals.

*5 : • Applicable to pins : D16 to D31, A00 to A24, RDY, \overline{BGRNT} , BRQ, \overline{RD} , $\overline{WR0}$, $\overline{WR1}$, $\overline{CS0}$ to $\overline{CS5}$, CLK, OCPA0 to OCPA3, OC0 to OC3, ALE, INT0 to INT5, SI0, SI2, SO0, SO2, TCI0, SC2

- Use within recommended operating conditions.

- Use at DC voltage (current) .

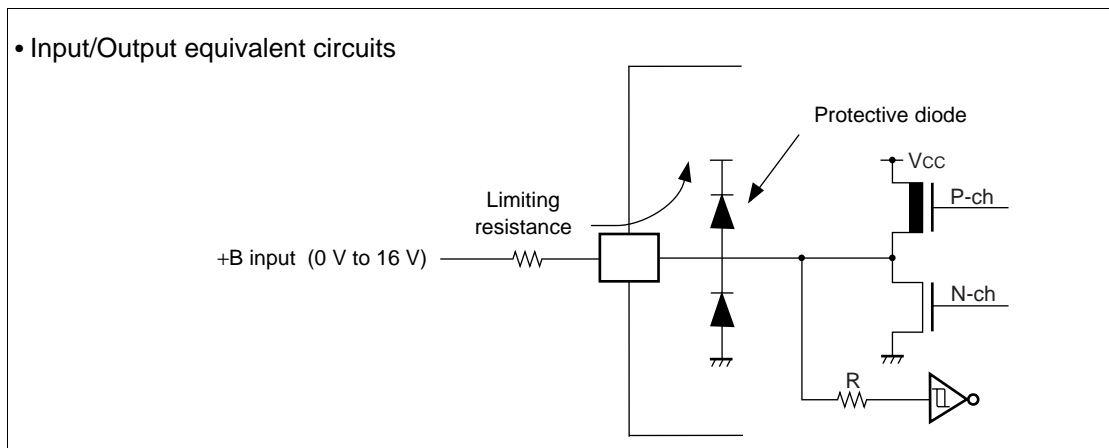
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

(Continued)

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(Continued)

- The value of the limiting resistance should be set so that when the signal is applied the input current to the microcontroller pins does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the input pin open.
- Sample recommended circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = AV_{SS} = 0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|--------------------------|-----------|----------------|----------------|------|--|
| | | Min | Max | | |
| Power supply | V_{CC} | 3.0 | 3.6 | V | Normal operation |
| | | 2.0 | 3.6 | | Retain RAM data under "stop" condition |
| Analog supply voltage | AV_{CC} | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V | |
| Analog reference voltage | AV_{RH} | AV_{SS} | AV_{CC} | V | |
| Operating temperature | T_A | -30 | +70 | °C | |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

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3. DC Characteristics

($AV_{CC} = V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $AV_{SS} = V_{SS} = 0 \text{ V}$, $T_A = -30 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|--------------------------|-----------|---------------------------------------|---|---------------------|-----|---------------------|---------------|---------------|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | V_{IHS} | Hysteresis input terminal | — | $0.8 \times V_{CC}$ | — | $V_{CC} + 0.3$ | V | * |
| "L" level input voltage | V_{ILS} | Hysteresis input terminal | — | $V_{SS} - 0.3$ | — | $0.2 \times V_{CC}$ | V | * |
| "H" level output voltage | V_{OH} | Port2 to PortJ | $V_{CC} = 3.3 \text{ V}$ $I_{OH} = -4.0 \text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| "L" level output voltage | V_{OL} | Port2 to PortJ | $V_{CC} = 3.3 \text{ V}$ $I_{OL} = 4.0 \text{ mA}$ | — | — | 0.4 | V | |
| Input leak current | I_{LI} | Port2 to PortJ | $V_{CC} = 3.6 \text{ V}$ $V_{SS} < V_I < V_{CC}$ | — | — | ± 5 | μA | |
| Power supply current | I_{CC} | VCC | 25 MHz $V_{CC} = 3.3 \text{ V}$ | — | 75 | 100 | mA | |
| | I_{CC} | | 25 MHz $V_{CC} = 3.3 \text{ V}$ | — | 85 | 120 | mA | FLASH writing |
| | I_{CCS} | | 25 MHz $V_{CC} = 3.3 \text{ V}$ | — | 60 | 85 | mA | Sleeping |
| | I_{CCH} | | $T_A = 25 \text{ }^\circ\text{C}$ $V_{CC} = 3.3 \text{ V}$ | — | 10 | 150 | μA | Stopping |
| Input capacity | C_{IN} | Other than AVCC, AVSS, AVRH, VCC, VSS | — | — | 10 | — | pF | |

* : Refer to "■ INPUT/OUTPUT CIRCUIT TYPE".

4. AC Characteristics

(1) Clock Timing Ratings

(V_{CC} = 3.3 V ± 0.3 V, AV_{SS} = V_{SS} = 0 V, T_A = -30 °C to +70 °C)

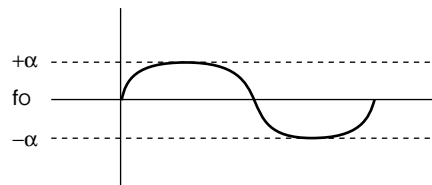
| Parameter | Symbol | Condition | Value | | Unit | Remarks | |
|--|------------------------------------|-------------------|----------------|---------|------|---|----|
| | | | Min | Max | | | |
| Clock frequency (High speed, automatic oscillation) | f _c | — | 10 | 25 | MHz | Self oscillation allowable range | |
| Clock frequency (High speed, PLL used) | | | 10 | 25 | MHz | PLL-use allowable area for self oscillation and external clock input *1 | |
| Clock frequency (High speed, 1/2 division input) | | | 10 | 25 | MHz | External clock input allowable range | |
| Clock cycle time | | | t _c | 40 | 100 | ns | |
| Frequency regulation (when locked) | | | Δf | — | 10 | % | *2 |
| Input clock pulse width | P _{WH} , P _{WL} | — | 9.5 | — | ns | | |
| Input clock rise and fall time | t _{CR} t _{CF} | — | — | 8 | ns | (t _{CR} + t _{CF}) | |
| Internal operation clock frequency | CPU system | f _{CP} | 0.625 *3 | 25 | MHz | | |
| | Peripheral system | f _{CPP} | 0.625 *3 | 25 | MHz | | |
| Internal operation clock cycle time | CPU system | t _{CP} | 40 | 1600 *3 | ns | | |
| | Peripheral system | t _{LCPP} | 40 | 1600 *3 | ns | | |

*1 : Although PLL allows selection among x1 and x2 multiplication modes, the selection is limited by oscillation frequency as follows:

Specifying "x2 multiplication" is not allowed if oscillation frequency exceeds 12.5 MHz.

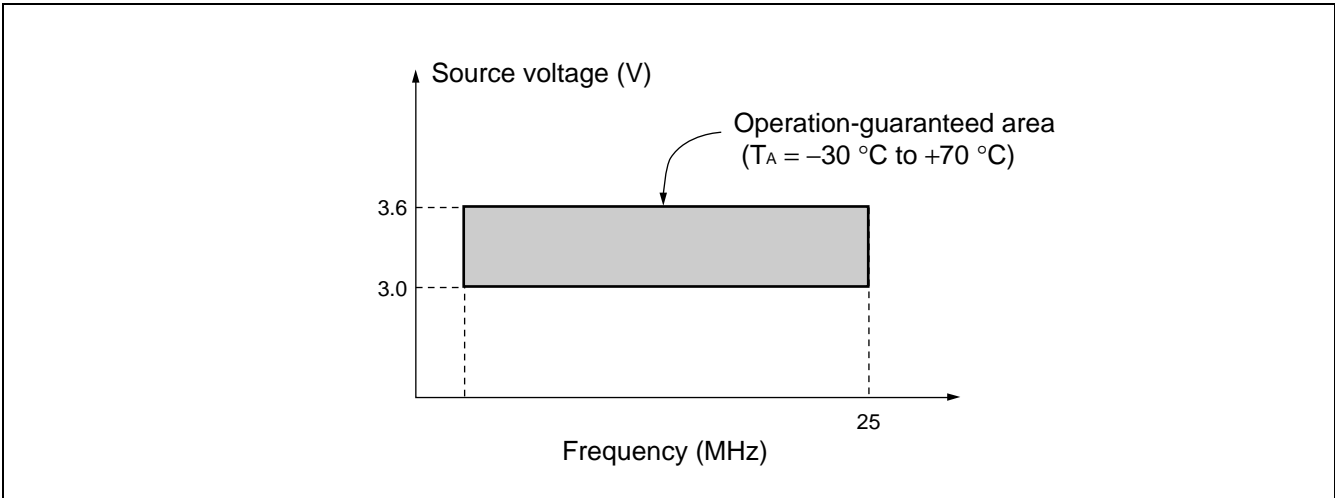
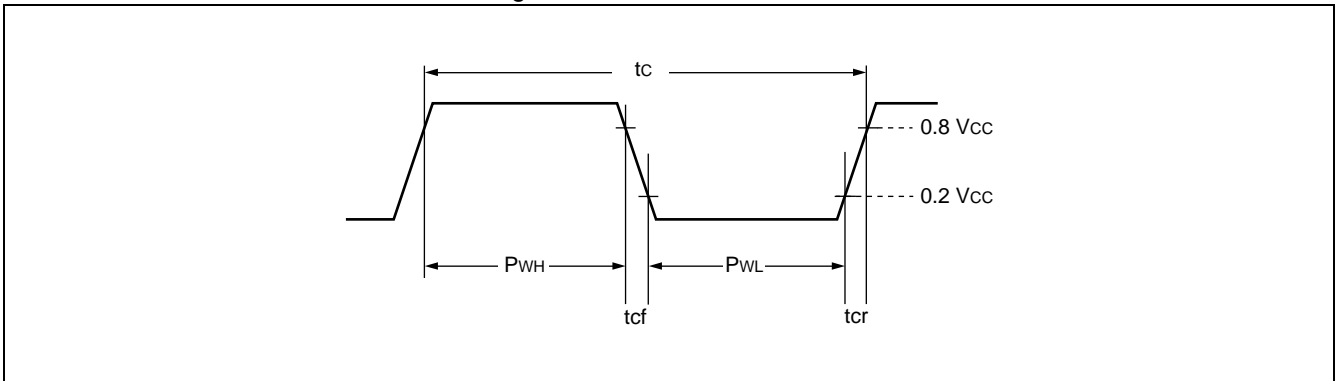
*2 : Frequency regulation indicates a maximum fluctuation from a specified center frequency under locked frequency multiplication.

$$\Delta f = \frac{|\alpha|}{f_0} \times 100 (\%)$$



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*3 : This is a value in the case where 10 MHz signal, a minimum value of clock frequency, is input to X0 and where 1/2-division in oscillation circuit and 1/8-gear are used.



(2) Clock Output Timing

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|-----------------------------------|------------|----------|-----------|---------------------------|---------------------------|------|---------|
| | | | | Min | Max | | |
| Cycle time | t_{CYC} | CLK | — | t_{CP} | — | ns | *1 |
| CLK \uparrow → CLK \downarrow | t_{CHCL} | CLK | | $1/2 \times t_{CYC} - 10$ | $1/2 \times t_{CYC} + 10$ | ns | *2 |
| CLK \downarrow → CLK \uparrow | t_{CLCH} | CLK | | $1/2 \times t_{CYC} - 10$ | $1/2 \times t_{CYC} + 10$ | ns | *3 |

*1 : t_{CYC} is a frequency of 1 clock cycle indicating gear cycle.

*2 : The values indicate specifications where x1 gear cycle is used.

If gear cycle of 1/2, 1/4, or 1/8 is specified, calculate in the formula below by substituting 1/2, 1/4, or 1/8 into n.

$$\text{Min : } (1 - n / 2) \times t_{CYC} - 10$$

$$\text{Max : } (1 - n / 2) \times t_{CYC} + 10$$

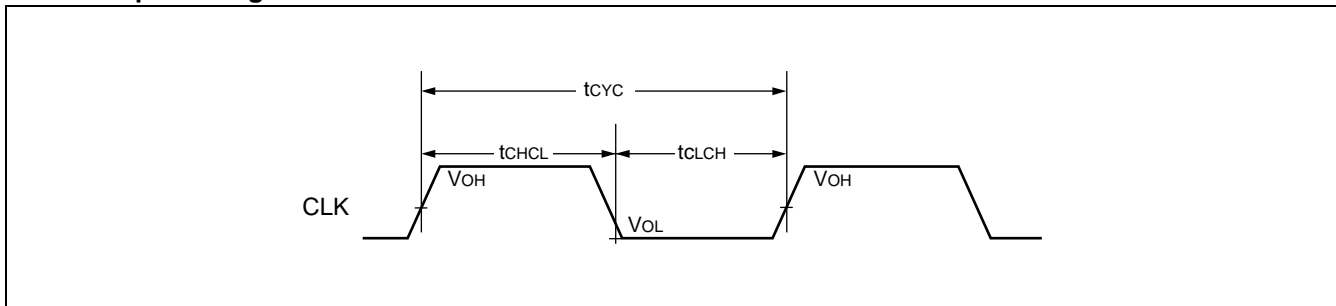
*3 : The values indicate specifications where x1 gear cycle is used.

If gear cycle of 1/2, 1/4, or 1/8 is specified, calculate in the formula below by substituting 1/2, 1/4, or 1/8 into n.

$$\text{Min : } n / 2 \times t_{CYC} - 10$$

$$\text{Max : } n / 2 \times t_{CYC} + 10$$

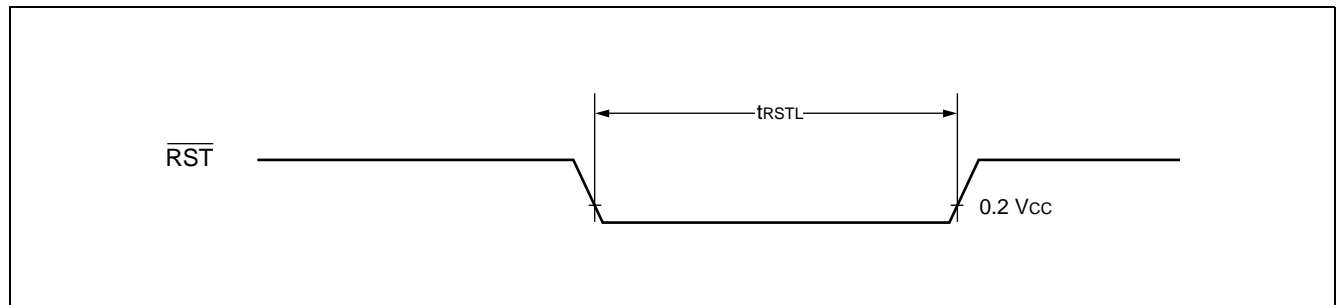
Clock output timing



(3) Reset Input Ratings

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|------------------|------------|-------------------------|-----------|-------------------|-----|------|---------|
| | | | | Min | Max | | |
| Reset input time | t_{RSTL} | $\overline{\text{RST}}$ | — | $t_{CP} \times 5$ | — | ns | |

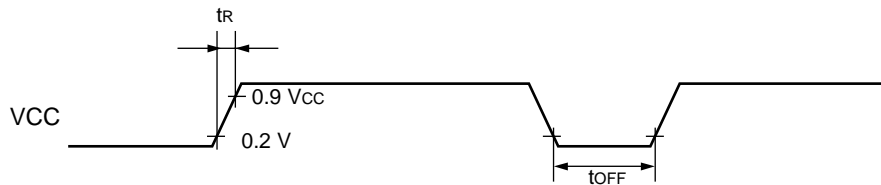


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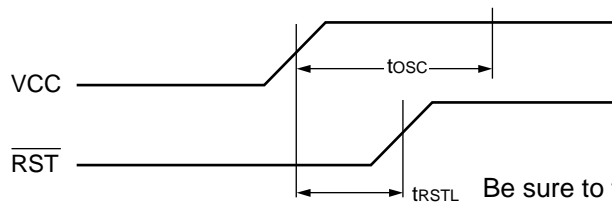
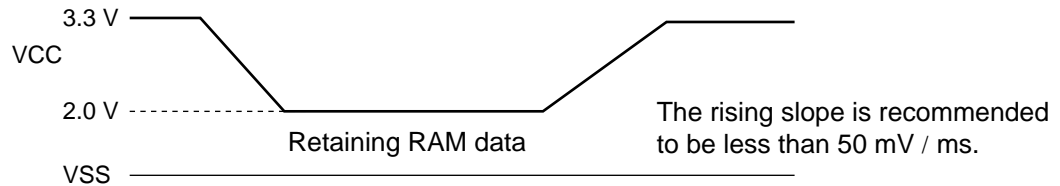
(4) Power-on Reset

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|-----------------------------------|-----------|----------|-------------------------|---|-----|------|---|
| | | | | Min | Max | | |
| Power supply rise time | t_R | VCC | $V_{CC} = 3.3\text{ V}$ | — | 20 | ms | $V_{CC} < 0.2\text{ V}$ before turning on power |
| Power supply shut off time | t_{OFF} | VCC | — | 2 | — | ms | |
| Oscillation stabilizing wait time | t_{OSC} | — | — | $2 \times t_c \times 2^{21} + 100\text{ }\mu\text{s}$ | — | ns | |



A sudden change of supply voltage may activate the power-on reset function. It is recommended that power voltage should be changed smoothly with less fluctuation of voltages.



Be sure to turn on the power while keeping $\overline{\text{RST}}$ terminal at L level first. When the power becomes V_{CC} level, rise the voltage to H level after a period of t_{RSTL} .

(5) Normal Bus Access Read/Write Operation

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

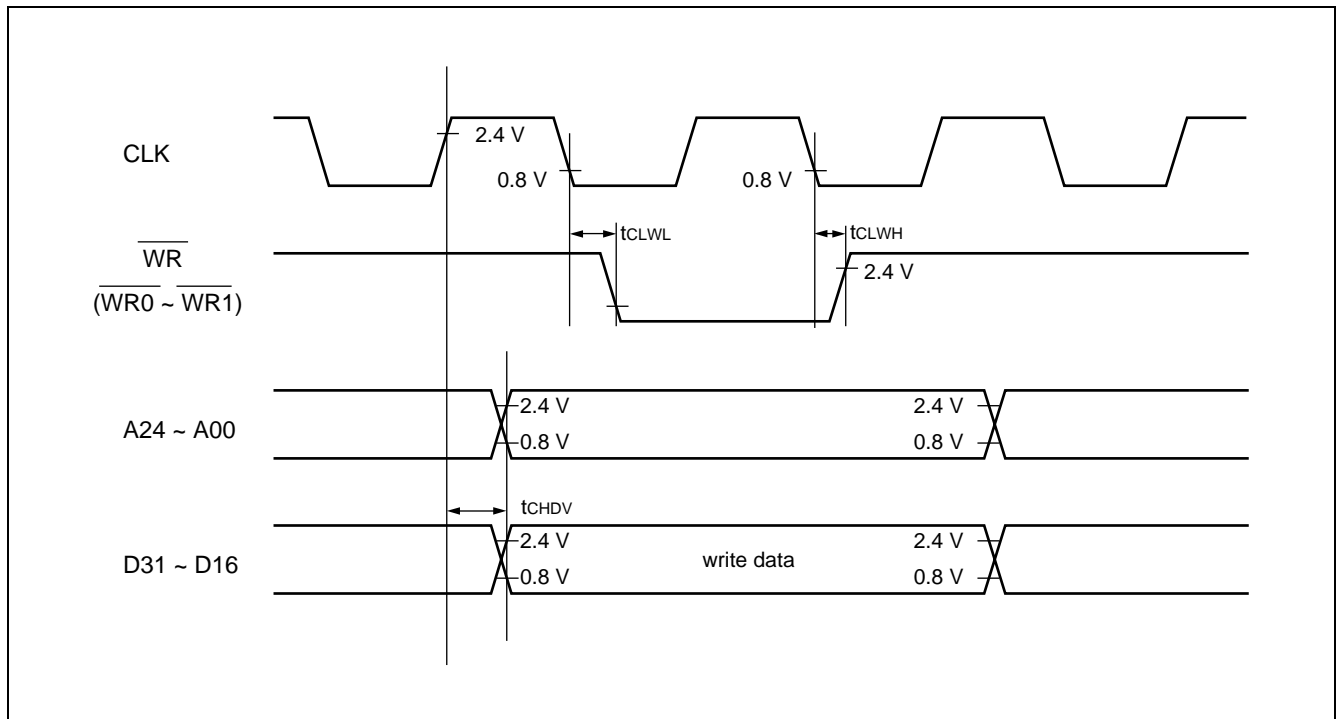
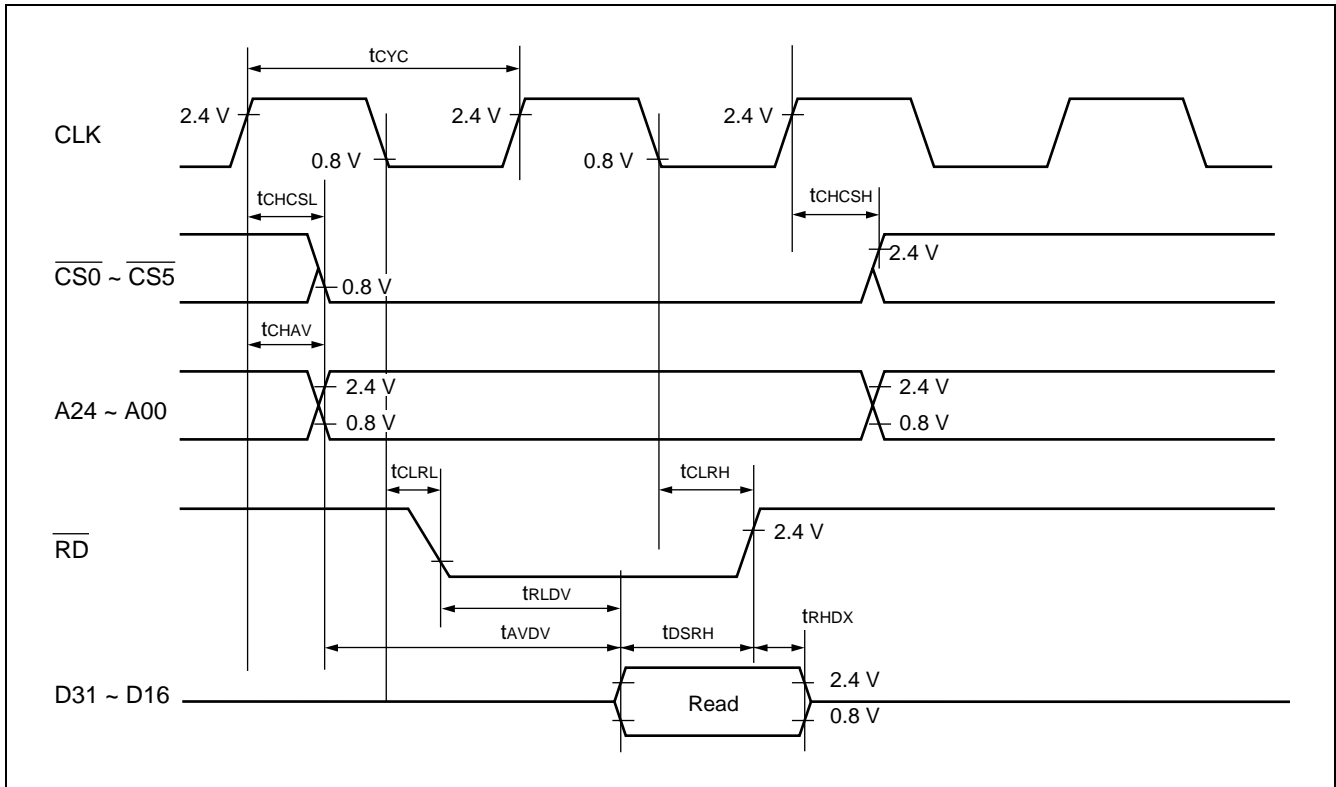
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|-------------|---------------------------------------|-----------|-------|---------------------------|------|----------|
| | | | | Min | Max | | |
| CS0 to CS5 delay time | t_{CHCSL} | CLK | — | — | 15 | ns | |
| CS0 to CS5 delay time | t_{CHCSH} | $\overline{CS0}$ to $\overline{CS5}$ | | — | 15 | ns | |
| Address delay time | t_{CHAV} | CLK A24 to A00 | | — | 15 | ns | |
| Data delay time | t_{CHDV} | CLK D31 to D16 | | — | 15 | ns | |
| \overline{RD} delay time | t_{CLRRL} | CLK RD | | — | 15 | ns | |
| \overline{RD} delay time | t_{CLRHL} | | | — | 15 | ns | |
| $\overline{WR0}, \overline{1}$ delay time | t_{CLWL} | CLK $\overline{WR0}, \overline{1}$ | | — | 15 | ns | |
| $\overline{WR0}, \overline{1}$ delay time | t_{CLWH} | | | — | 15 | ns | |
| Valid address→ Valid data input time | t_{AVDV} | A24 to A00 D31 to D16 | | — | $3/2 \times t_{cyc} - 25$ | ns | *1 *2 |
| $\overline{RD}\downarrow\rightarrow$ Valid data input time | t_{RLDV} | \overline{RD} D31 to D16 | | — | $t_{cyc} - 25$ | ns | *1 |
| Data setup → $\overline{RD}\uparrow$ Time | t_{DSRH} | | | 25 | — | ns | |
| $\overline{RD}\uparrow\rightarrow$ Data hold time | t_{RHDX} | | | 0 | — | ns | |

*1 : If the bus is expanded by automatic wait insertion or RDY input, add time ($t_{cyc} \times$ the number of expanded cycles) to the rated value.

*2 : The ratings are based on conditions with “gear cycle $\times 1$ ”. If gear cycle of 1/2, 1/4, or 1/8 is specified, calculate in the formula below by substituting 1/2, 1/4, or 1/8 into n.

Formula : $(2 - n / 2) \times t_{cyc} - 25$

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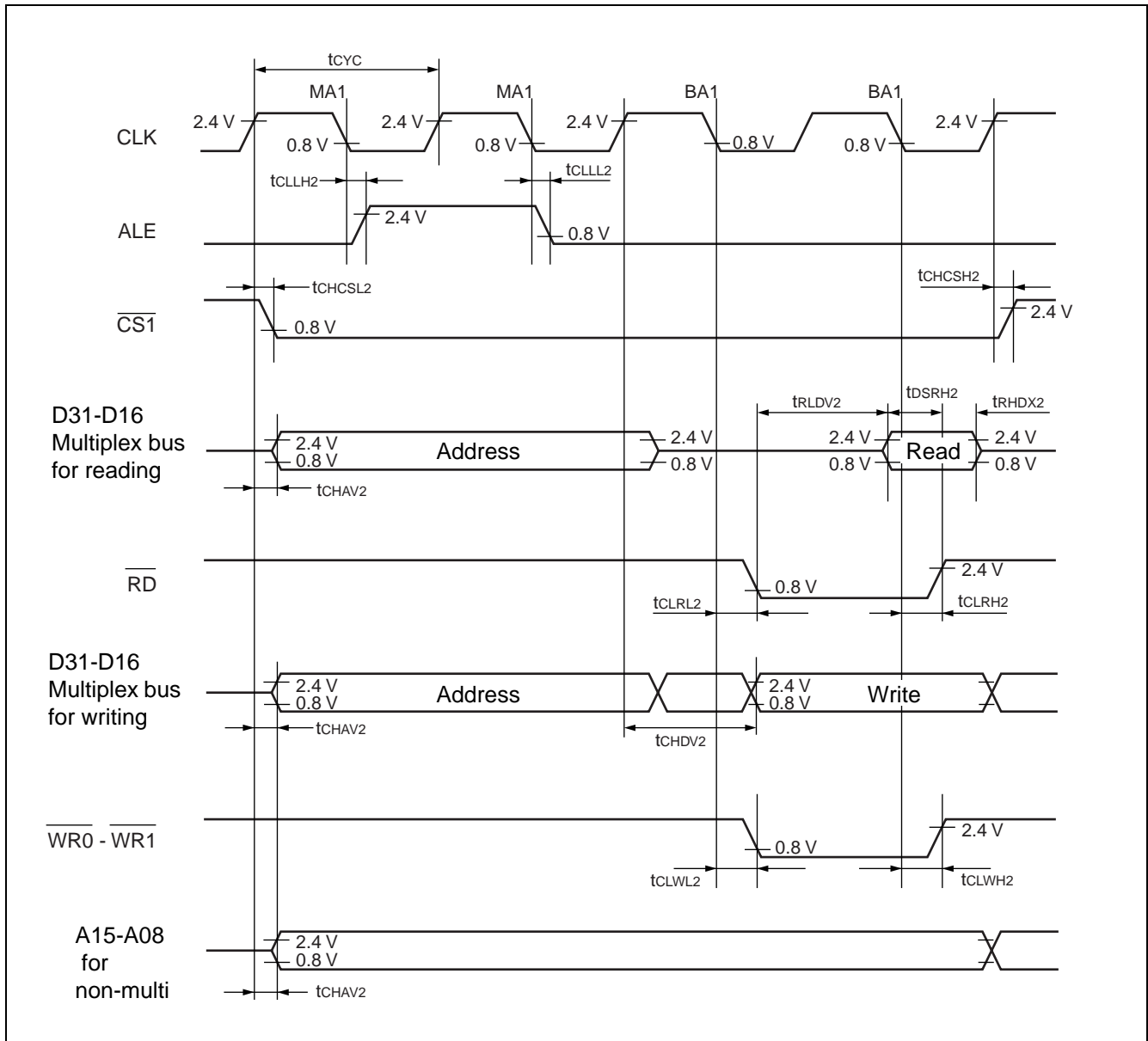
(6) Timeshared Bus Access Read/Write Operations

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--|--------------|--|-----------|-------|----------------|------|---------|
| | | | | Min | Max | | |
| ALE delay time | t_{CLLH2} | CLK | — | — | 10 | — | |
| ALE delay time | t_{CLL2} | ALE | | — | 10 | — | |
| $\overline{\text{CS1}}$ delay time | t_{CHCSL2} | CLK | | — | 15 | — | |
| $\overline{\text{CS1}}$ delay time | t_{CHCSH2} | $\overline{\text{CS1}}$ | | — | 15 | ns | |
| Address delay time | t_{CHAV2} | CLK | | — | 15 | ns | |
| Data delay time | t_{CHDV2} | D31 to D16 | | — | 15 | ns | |
| $\overline{\text{RD}}$ delay time | t_{CLRL2} | CLK | | — | 10 | ns | |
| $\overline{\text{RD}}$ delay time | t_{CLRH2} | $\overline{\text{RD}}$ | | — | 10 | ns | |
| $\overline{\text{WR0}}, \overline{1}$ delay time | t_{CLWL2} | CLK | | — | 10 | ns | |
| $\overline{\text{WR0}}, \overline{1}$ pulse width | t_{CLWH2} | $\overline{\text{WR0}}$ $\overline{\text{WR1}}$ | | — | 10 | ns | |
| $\overline{\text{RD}}\downarrow\rightarrow$ Valid data input time | t_{RLDV2} | $\overline{\text{RD}}$ D31 to D16 | | — | $t_{cyc} - 25$ | — | * |
| Data setup $\rightarrow\overline{\text{RD}}\uparrow$ time | t_{DSRH2} | | | 25 | — | ns | |
| $\overline{\text{RD}}\uparrow\rightarrow$ Data hold time | t_{RHDX2} | | | 0 | — | ns | |

* : If the bus is expanded by automatic wait insertion or RDY input, add time ($t_{cyc} \times$ the number of expanded cycles) to the rated value.

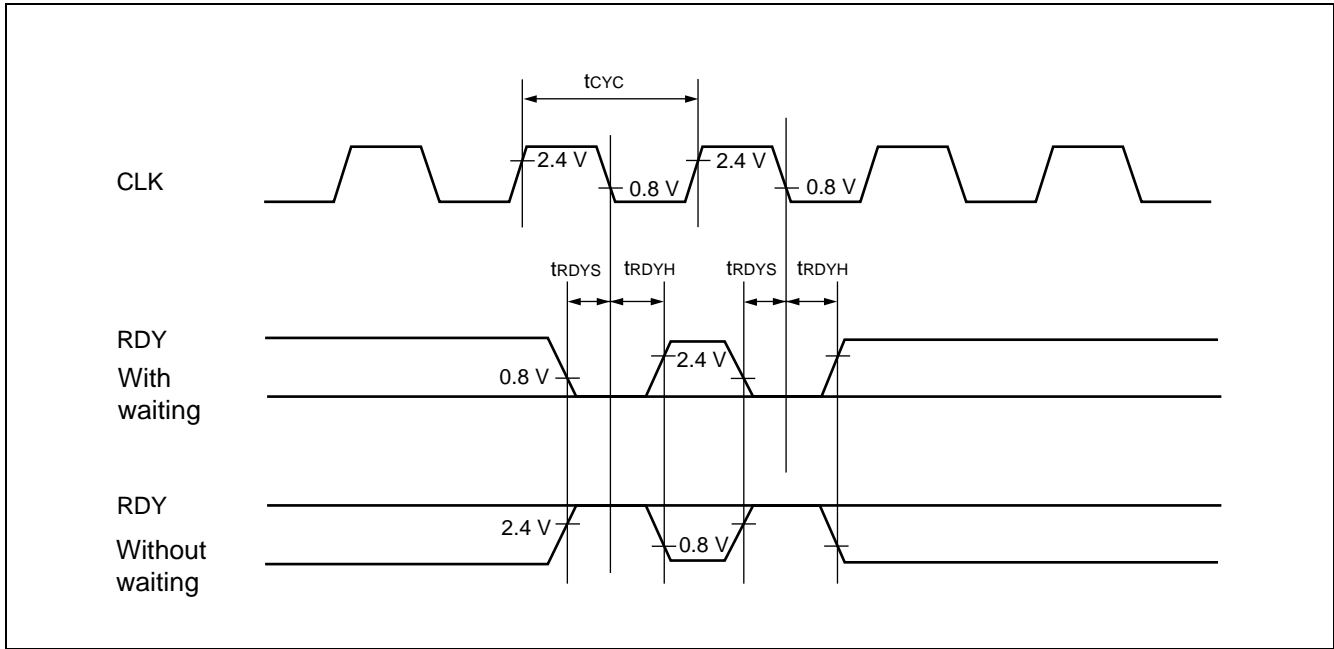
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(7) Ready Input Timing

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $AV_{SS} = V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|-------------------------|------------|------------|-----------|-------|-----|------|---------|
| | | | | Min | Max | | |
| RDY setup time RCLK↓ | t_{RDYS} | RDY CLK | — | 15 | — | ns | |
| CLK↓→ RDY hold time | t_{RDYH} | CLK RDY | | 0 | — | ns | |



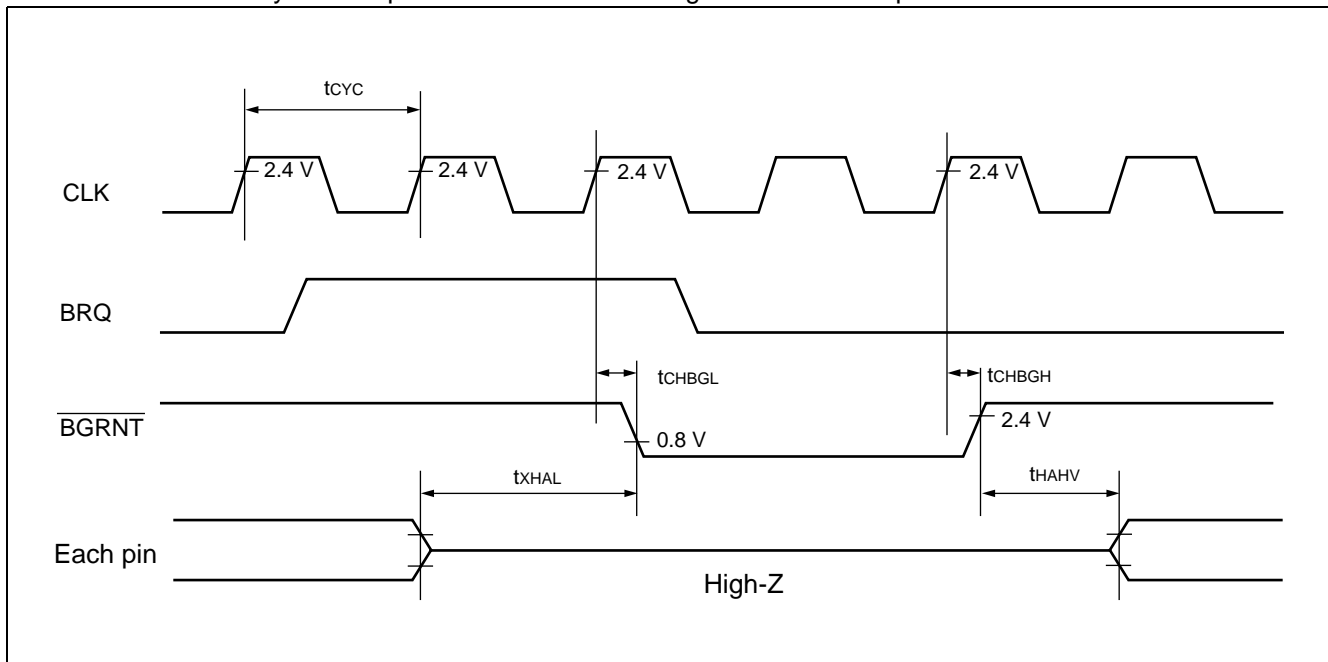
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(8) Hold Timing

($V_{CC} = 3.0\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|-----------------------------------|-------------|--------------|-----------|----------------|----------------|------|---------|
| | | | | Min | Max | | |
| BGRNT delay time | t_{CHBGL} | CLK BGRNT | — | — | 10 | ns | |
| BGRNT delay time | t_{CHBGH} | | | — | 10 | ns | |
| Terminal floating →BGRNT↓ time | t_{XHAL} | BGRNT | | $t_{CYC} - 10$ | $t_{CYC} + 10$ | ns | |
| BGRNT↑ →Terminal valid time | t_{HAHV} | | | $t_{CYC} - 10$ | $t_{CYC} + 10$ | ns | |

Note : More than one cycle is required for BGRNT to change after BRQ is input.



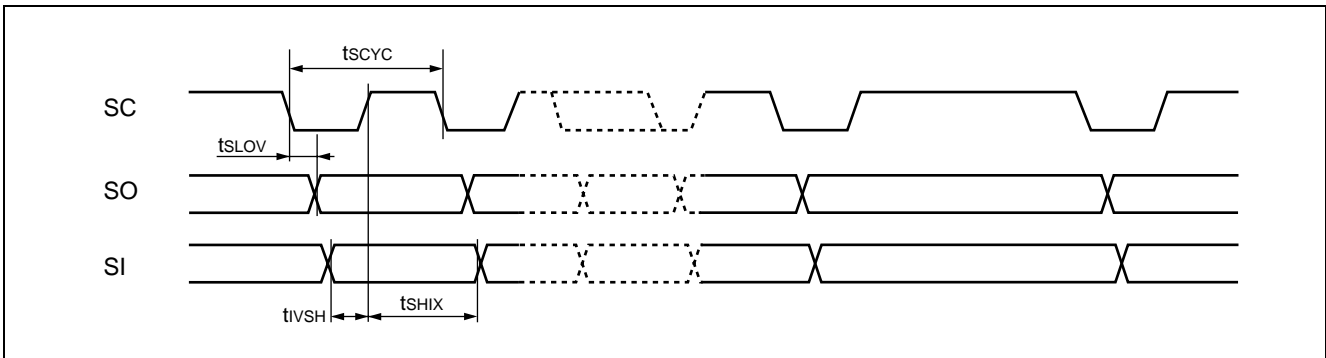
(9) UART Timing

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

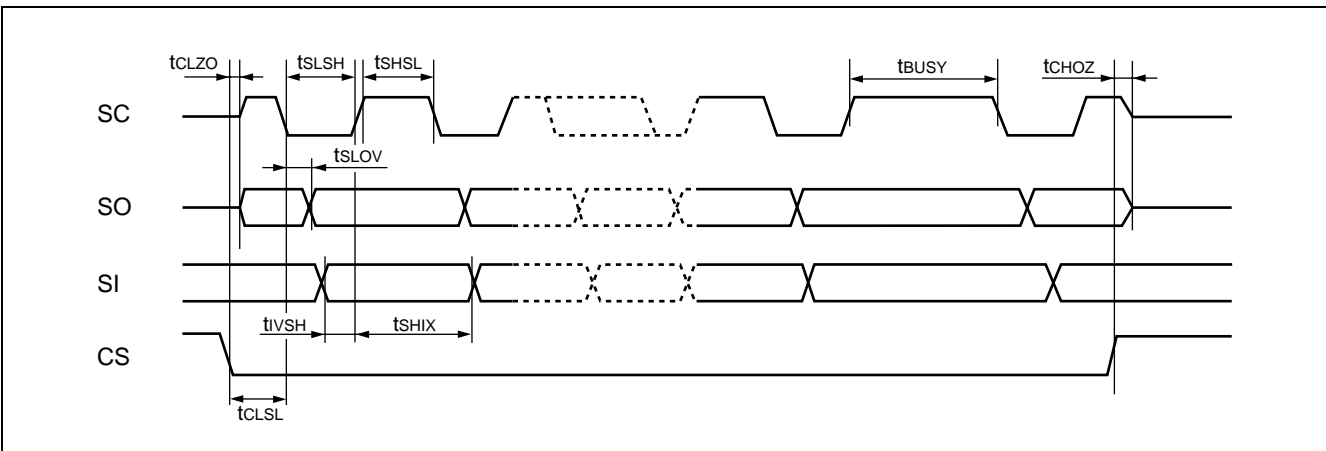
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|--------------------------------------|------------|----------|---------------------------|---------------------|----------------|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | — | Internal shift clock mode | $8 t_{CYCP}^*$ | — | ns | |
| SC \downarrow → SO delay time | t_{SLOV} | — | | -10 | +50 | ns | |
| Valid SI → SC \uparrow | t_{IVSH} | — | | 50 | — | ns | |
| SC \uparrow → Valid SI hold time | t_{SHIX} | — | | 50 | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | — | External shift clock mode | $4 t_{CYCP}^* - 10$ | — | ns | |
| Serial clock "L" pulse width | t_{LSLH} | — | | $4 t_{CYCP}^* - 10$ | — | ns | |
| SC \downarrow → SO delay time | t_{SLOV} | — | | 0 | 50 | ns | |
| Valid SI → SC \uparrow | t_{IVSH} | — | | 50 | — | ns | |
| SC \uparrow → Valid SI hold time | t_{SHIX} | — | | 50 | — | ns | |
| Serial busy time | t_{BUSY} | — | | — | $6 t_{CYCP}^*$ | ns | |
| CS \downarrow → SC, SO delay time | t_{CLZO} | — | | — | 50 | ns | |
| CS \downarrow → SC input mask time | t_{CLSL} | — | | — | $3 t_{CYCP}^*$ | ns | |
| SC \uparrow → SC, SO Hi-z time | t_{CHOZ} | — | — | 50 | ns | | |

* : t_{CYCP} is a cycle time of peripheral system clock.

Internal shift clock mode



External shift clock mode



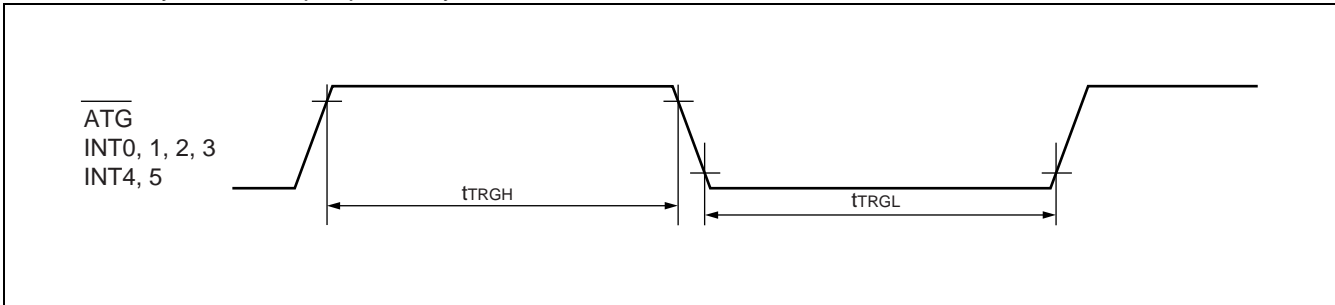
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(10) Trigger Input Timing

($V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -30\text{ }^\circ\text{C}$ to $+70\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|-------------------|--------------------------|--|-----------|----------------|-----|------|---------|
| | | | | Min | Max | | |
| Input pulse width | t_{TRGH} t_{TRGL} | \overline{ATG} , INT0, 1, 2, 3 INT4, 5 | — | $5 t_{CYCP}^*$ | — | ns | |

* : t_{CYCP} is a cycle time of peripheral system clock.



(11) A/D Converter Block Electrical Characteristics

($V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $AV_{SS} = V_{SS} = 0 \text{ V}$, $T_A = -30 \text{ }^\circ\text{C}$ to $+70 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|----------------------------------|-----------|------------|-----------------------------|-----------------------------|-----------------------------|---------------|---------|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | 10 | BIT | |
| Total error | — | — | — | — | ± 4.0 | LSB | |
| Linearity error | — | — | — | — | ± 3.5 | LSB | |
| Differential linearity error | — | — | — | — | ± 2.0 | LSB | |
| Zero transition voltage | V_{0t} | AN0 to AN7 | $AV_{SS} - 1.5 \text{ LSB}$ | $AV_{SS} + 0.5 \text{ LSB}$ | $AV_{SS} + 2.5 \text{ LSB}$ | mV | |
| Full-scale transition voltage | V_{FST} | AN0 to AN7 | $AVRH - 5.5 \text{ LSB}$ | $AVRH - 1.5 \text{ LSB}$ | $AVRH + 0.5 \text{ LSB}$ | mV | |
| Conversion time | — | — | 5.3 | — | — | μs | |
| Analog input current | I_{AIN} | AN0 to AN7 | — | 0.1 | 10 | μA | |
| Analog input voltage | V_{AIN} | AN0 to AN7 | AV_{SS} | — | $AVRH$ | V | |
| Reference voltage | — | $AVRH$ | AV_{SS} | — | AV_{CC} | V | |
| Power supply current | I_A | $AVCC$ | — | 3.0 | 5.0 | mA | |
| | I_{AH} | | — | — | 5.0 | μA | |
| Reference voltage supply current | I_R | $AVRH$ | — | 100 | 150 | μA | |
| | I_{RH} | | — | — | 10 | μA | |
| Variation among channels | — | AN0 to AN7 | — | — | 4 | LSB | |

Notes : • Relatively, the errors increase as $|AVRH|$ value becomes smaller.

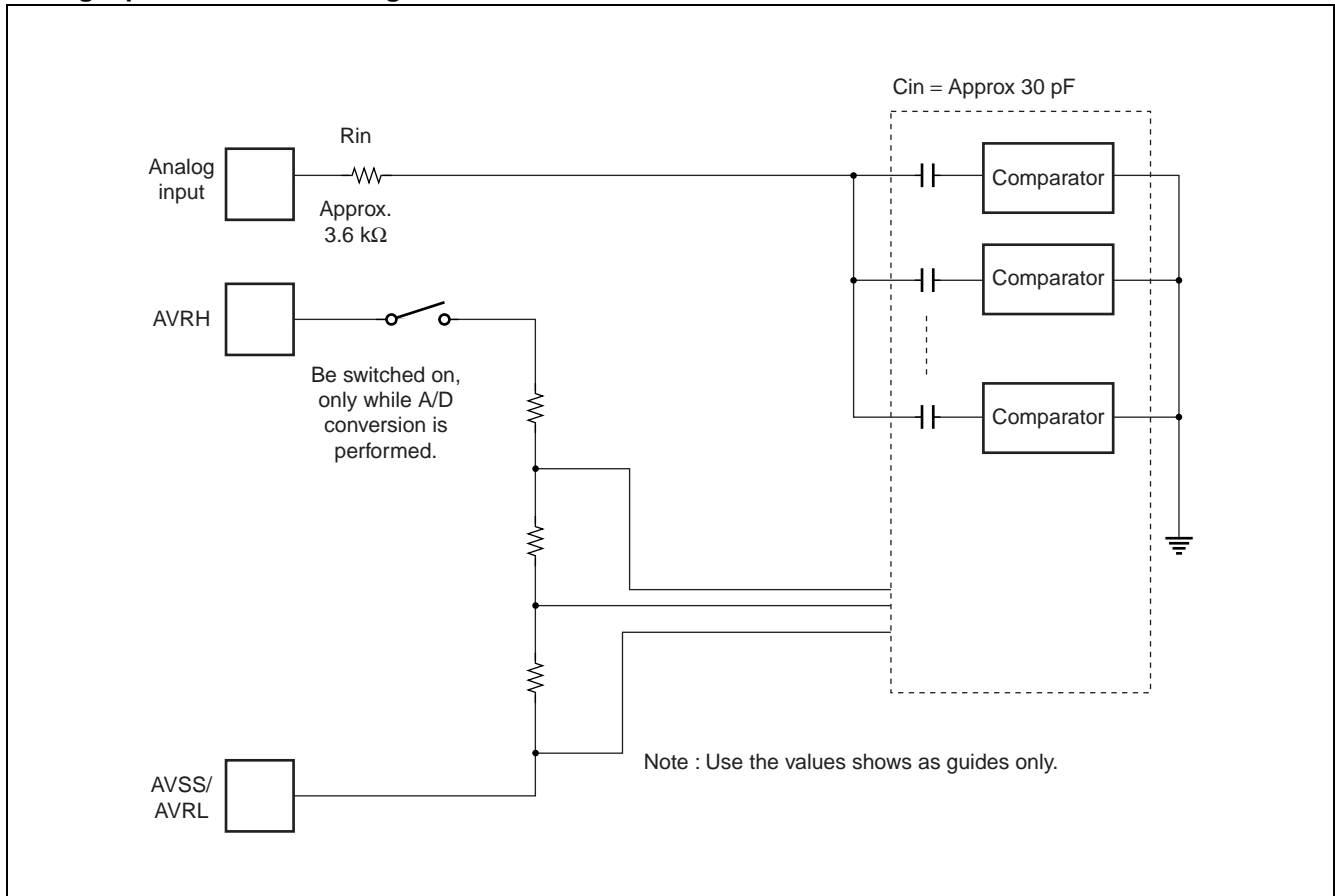
- Define an output impedance of external circuit analog input under the following conditions :

Output impedance of external circuit $\leq 2 \text{ (k}\Omega\text{)}$

If an output impedance of external circuit is exceedingly high, sampling time for analog voltage may run short.

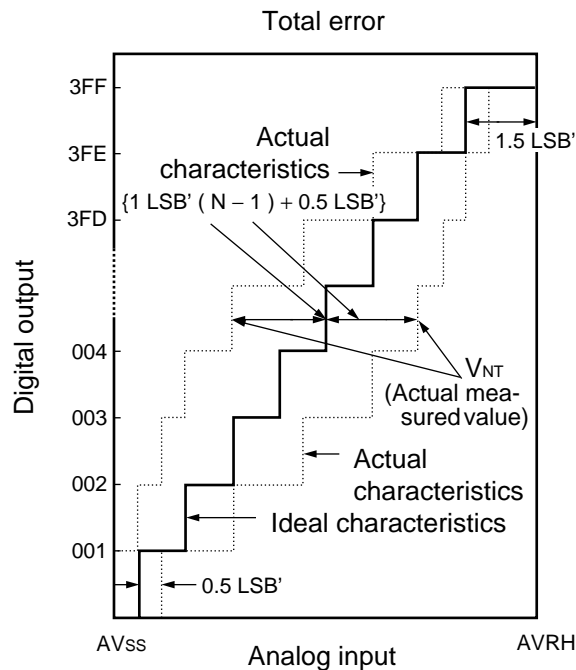
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Analog input circuit model diagram



5. A/D Converter Block Electrical Characteristics

- Resolution
Analog variations recognized by an A/D converter.
- Linearity error
Deviation of actual conversion characteristics from an ideal line, which is across zero-transition point (“00 0000 0000” \leftrightarrow “00 0000 0001”) and full-scale transition point (“11 1111 1110” \leftrightarrow “11 1111 1111”)
- Differential linearity error
Deviation from ideal value of input voltage, which is required for changing output code by 1 LSB.
- Total error
Difference between actual value and ideal value. The error includes zero-transition error, full-scale transition error, and linearity error.



$$1 \text{ LSB}' (\text{Ideal value}) = \frac{AVRH - AVSS}{1024} \text{ [V]}$$

$$\text{Total error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + 0.5 \text{ LSB}'\}}{1 \text{ LSB}'}$$

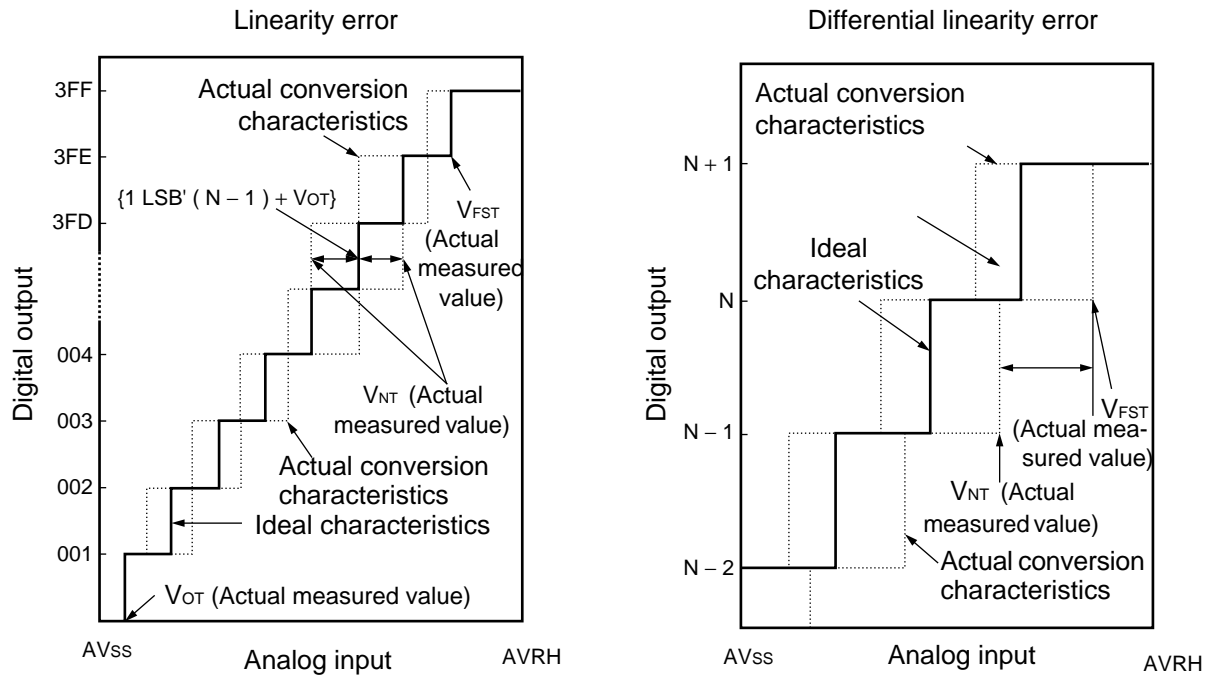
V_{NT} : Transition voltage for digital output to change from (N+1) to N.

$$V_{OT}' (\text{Ideal value}) = AVSS + 0.5 \text{ LSB}' \text{ [V]}$$

$$V_{FST}' (\text{Ideal value}) = AVRH - 1.5 \text{ LSB}' \text{ [V]}$$

(Continued)

(Continued)



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB}' \times (N - 1) + V_{OT}\}}{1 \text{ LSB}'} \quad [\text{LSB}]$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}'} - 1 \quad [\text{LSB}]$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \quad [\text{V}]$$

V_{OT} : Transition voltage for digital output to change from (000)_H to (001)_H.

V_{FST} : Transition voltage for digital output to change from (3FE)_H to (3FF)_H.

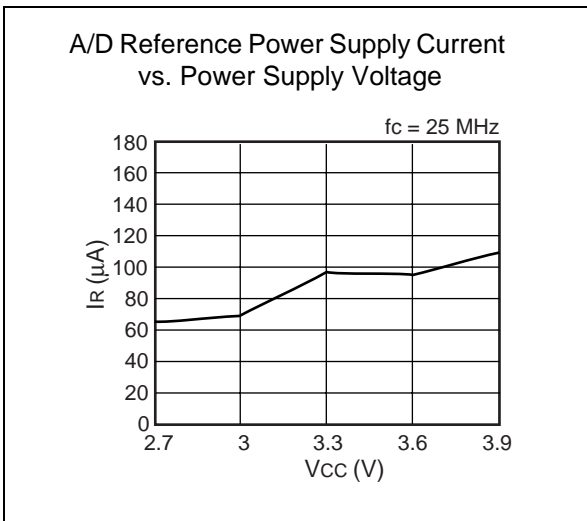
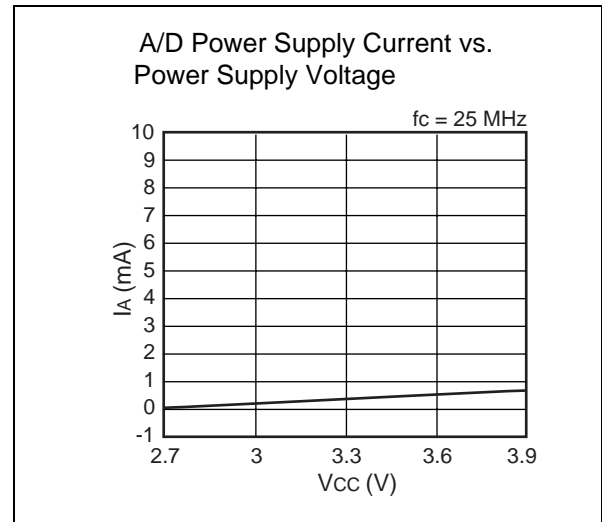
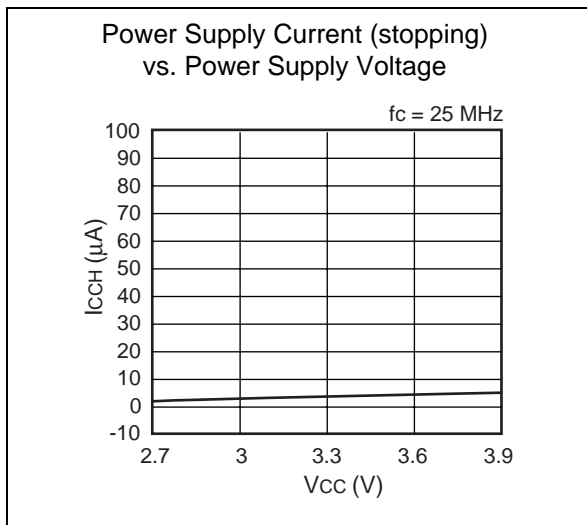
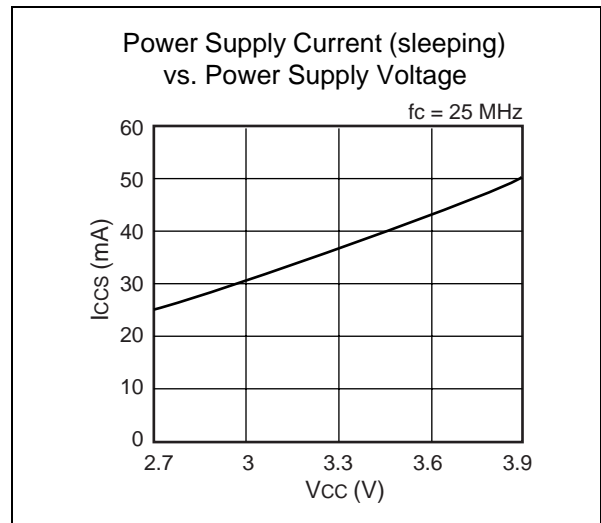
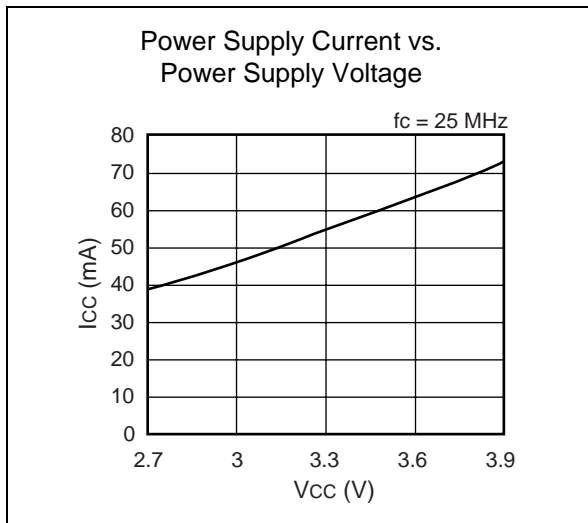
■ FLASH MEMORY WRITE/ERASE CHARACTERISTICS

| Parameter | Condition | Value | | | Unit | Remarks |
|---------------------------------------|--|-------|---------|------|---------------|--|
| | | Min | Typ | Max | | |
| Sector erase time | $T_A = +25\text{ }^\circ\text{C}$, $V_{CC} = 3.3\text{ V}$ | — | 1 | 15 | s | Not including time for internal writing before deletion. |
| Chip erase time | | — | 4 | — | s | Not including time for internal writing before deletion. |
| Half byte (16 bit width) writing time | | — | 16 | 3600 | μs | Not including system-level overhead time. |
| Write/erase cycle | — | — | 10,000 | — | cycle | |
| Data holding time | — | — | 100,000 | — | h | |

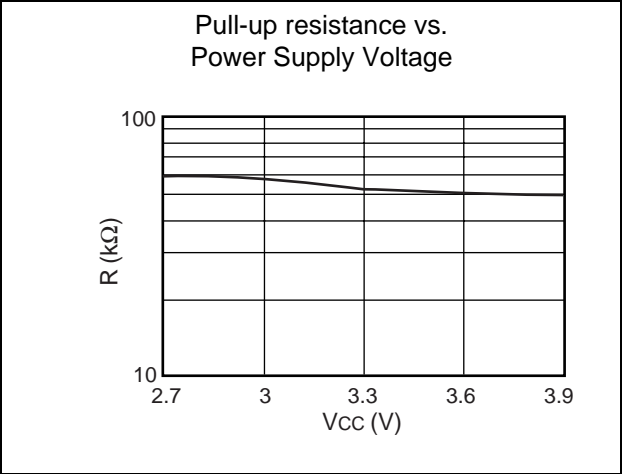
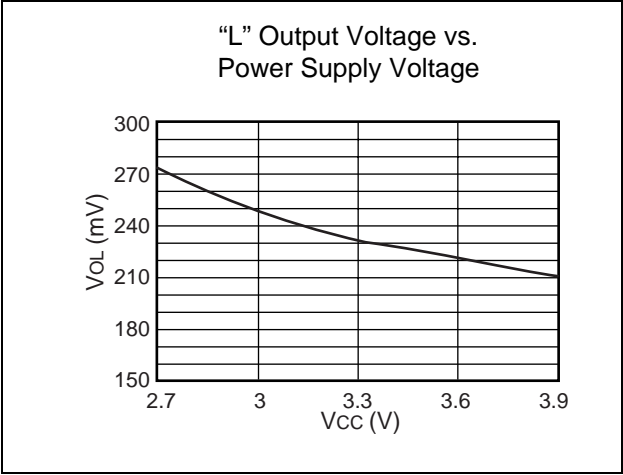
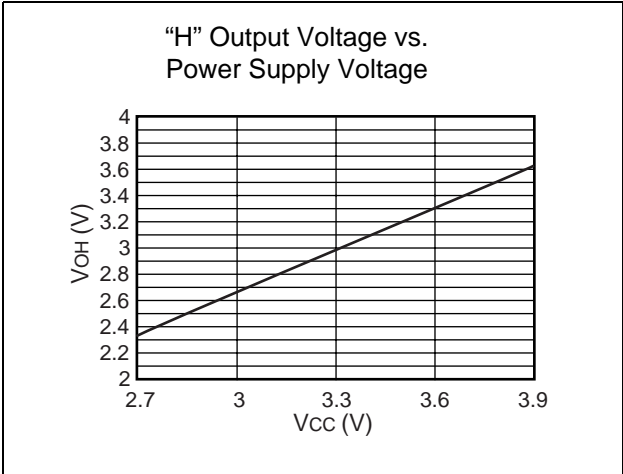
MB91F127/F128

■ EXAMPLE CHARACTERISTICS

- Power Supply Current



- Output Voltage



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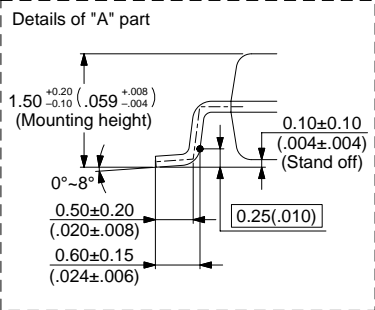
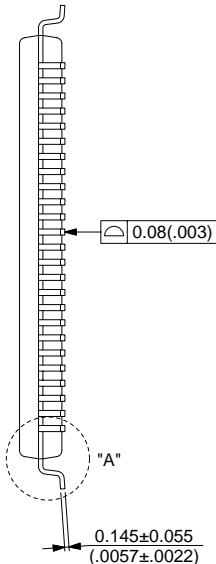
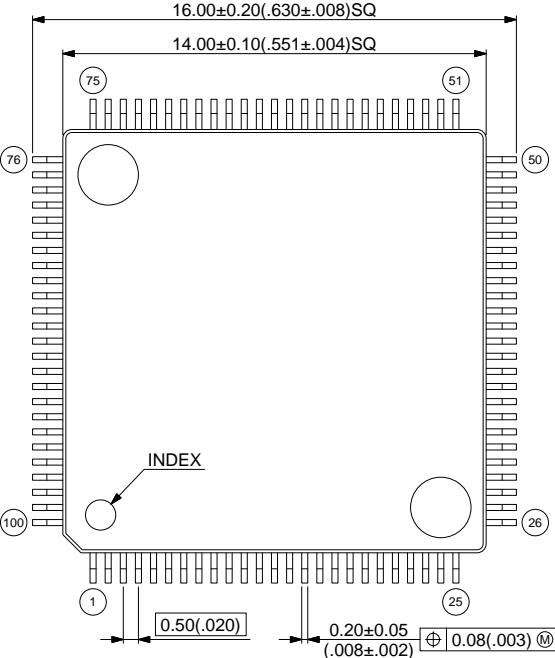
■ ORDERING INFORMATION

| Part number | Package | Remarks |
|-------------|--|---------|
| MB91F127PFV | 100-pin plastic LQFP (FPT-100P-M05) | |
| MB91F128PFV | 100-pin plastic LQFP (FPT-100P-M05) | |

■ PACKAGE DIMENSIONS

100-pin plastic LQFP
(FPT-100P-M05)

*Pins width and pins thickness include plating thickness.



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Dimensions in mm (inches)

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