

MC14060B

14-Bit Binary Counter and Oscillator

The MC14060B is a 14-stage binary ripple counter with an on-chip oscillator buffer. The oscillator configuration allows design of either RC or crystal oscillator circuits. Also included on the chip is a reset function which places all outputs into the zero state and disables the oscillator. A negative transition on Clock will advance the counter to the next state. Schmitt trigger action on the input line permits very slow input rise and fall times. Applications include time delay circuits, counter controls, and frequency dividing circuits.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

- Fully Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Buffered Outputs Available from Stages 4 Through 10 and 12 Through 14
- Common Reset Line
- Pin-for-Pin Replacement for CD4060B
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in} , V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V_{DD} +0.5	V
I_{in} , I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	$^{\circ}C$
T_{stg}	Storage Temperature Range	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (8 Second Soldering)	260	$^{\circ}C$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/ $^{\circ}C$ from 65 $^{\circ}C$ To 125 $^{\circ}C$.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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MARKING DIAGRAMS



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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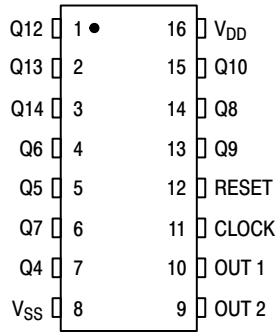


Table 1. Truth Table

Clock	Reset	Output State
	L	No Change
	L	Advance to Next State
H	H	All Outputs are Low

X = Don't Care

Figure 1. Pin Assignment

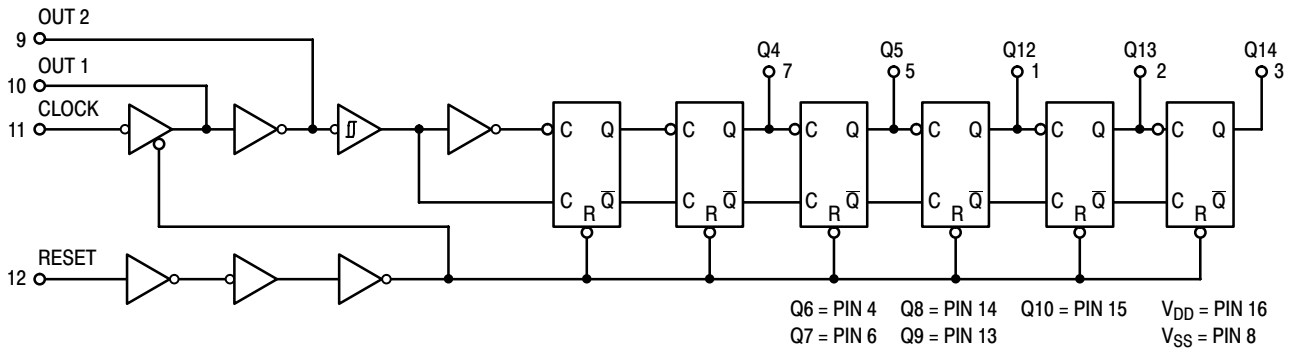


Figure 2. Logic Diagram

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Symbol	Characteristic	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
V _{OL}	Output Voltage V _{in} = V _{DD} or 0 "0" Level	5.0	–	0.05	–	0	0.05	–	0.05	V
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
V _{OH}	V _{in} = 0 or V _{DD} "1" Level	5.0	4.95	–	4.95	5.0	–	4.95	–	V
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
V _{IL}	Input Voltage (V _O = 4.5 or 0.5 V) (V _O = 9.0 or 1.0 V) (V _O = 13.5 or 1.5 V) "0" Level	5.0	–	1.5	–	2.25	1.5	–	1.5	V
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
V _{IH}	(V _O = 0.5 or 4.5 V) (V _O = 1.0 or 9.0 V) (V _O = 1.5 or 13.5 V) "1" Level	5.0	3.5	–	3.5	2.75	–	3.5	–	V
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11.0	–	11.0	8.25	–	11.0	–	
V _{IL}	Input Voltage (V _O = 4.5 Vdc) (V _O = 9.0 Vdc) (V _O = 13.5 Vdc) "0" Level (For Input 11 and Output 10)	5.0	–	1.0	–	2.25	1.0	–	1.0	Vdc
		10	–	2.0	–	4.50	2.0	–	2.0	
		15	–	2.5	–	6.75	2.5	–	2.5	
V _{IH}	(V _O = 0.5 Vdc) (V _O = 1.0 Vdc) (V _O = 1.5 Vdc) "1" Level	5.0	4.0	–	4.0	2.75	–	4.0	–	Vdc
		10	8.0	–	8.0	5.50	–	8.0	–	
		15	12.5	–	12.5	8.25	–	12.5	–	
I _{OH}	Output Drive Current (V _{OH} = 2.5 V) (V _{OH} = 4.6 V) (V _{OH} = 9.5 V) (V _{OH} = 13.5 V) (Except Source Pins 9 and 10)	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mA
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
I _{OL}	(V _{OL} = 0.4 V) (V _{OL} = 0.5 V) (V _{OL} = 1.5 V) Sink	5.0	0.64	–	0.51	0.88	–	0.36	–	mA
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
I _{in}	Input Current	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μA
C _{in}	Input Capacitance (V _{in} = 0)	–	–	–	–	5.0	7.5	–	–	pF
I _{DD}	Quiescent Current (Per Package)	5.0	–	5.0	–	0.005	5.0	–	150	μA
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
I _T	Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	5.0 10 15	I _T = (0.25 μA/kHz) f + I _{DD} I _T = (0.54 μA/kHz) f + I _{DD} I _T = (0.85 μA/kHz) f + I _{DD}							μA

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L – 50) Vfk
where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Symbol	Characteristic	V _{DD} Vdc	Min	Typ (Note 5)	Max	Unit
t _{TLH}	Output Rise Time (Counter Outputs)	5.0	–	40	200	ns
		10	–	25	100	
		15	–	20	80	
t _{THL}	Output Fall Time (Counter Outputs)	5.0	–	50	200	ns
		10	–	30	100	
		15	–	20	80	
t _{PLH} t _{PHL}	Propagation Delay Time Clock to Q4 Clock to Q14	5.0	–	415	740	ns
		10	–	175	300	
		15	–	125	200	
		5.0	–	1.5	2.7	μs
		10	–	0.7	1.3	
		15	–	0.4	1.0	
t _{WH}	Clock Pulse Width	5.0	100	65	–	ns
		10	40	30	–	
		15	30	20	–	
f _φ	Clock Pulse Frequency	5.0	–	5	3.5	MHz
		10	–	14	8	
		15	–	17	12	
t _{TLH} t _{THL}	Clock Rise and Fall Time	5.0	No Limit			ns
		10				
		15				
t _w	Reset Pulse Width	5.0	120	40	–	ns
		10	60	15	–	
		15	40	10	–	
t _{PHL}	Propagation Delay Time Reset to On	5.0	–	170	350	ns
		10	–	80	160	
		15	–	60	100	

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

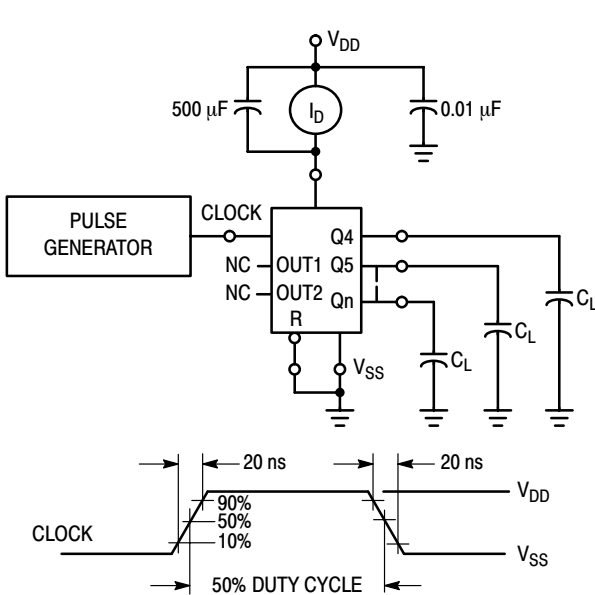


Figure 1. Power Dissipation Test Circuit and Waveform

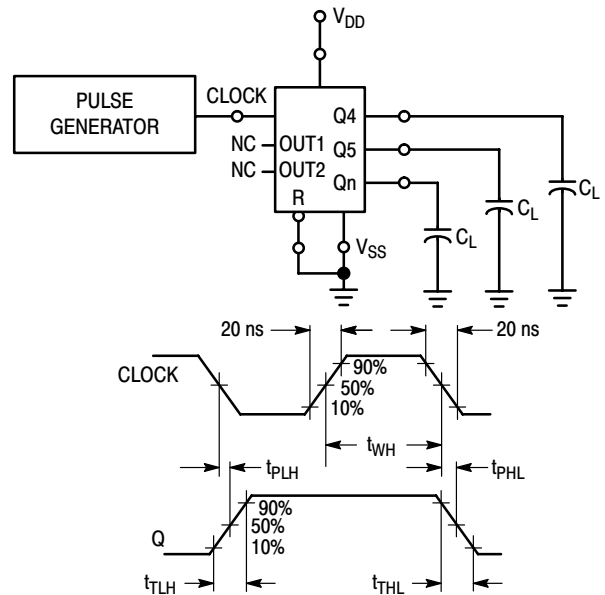
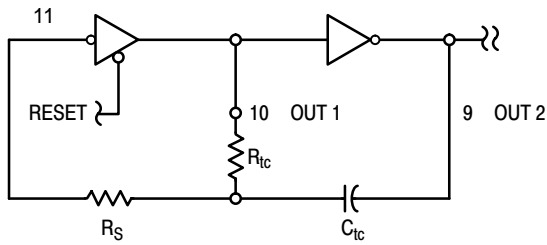


Figure 2. Switching Time Test Circuit and Waveforms

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$$f \approx \frac{1}{2.3R_{tc}C_{tc}}$$

if $1 \text{ kHz} \leq f \leq 100 \text{ kHz}$
and $2R_{tc} < R_S < 10R_{tc}$
(f in Hz, R in ohms, C in farads)

The formula may vary for other frequencies. Recommended maximum value for the resistors in $1 \text{ M}\Omega$.

Figure 3. Oscillator Circuit Using RC Configuration

TYPICAL RC OSCILLATOR CHARACTERISTICS

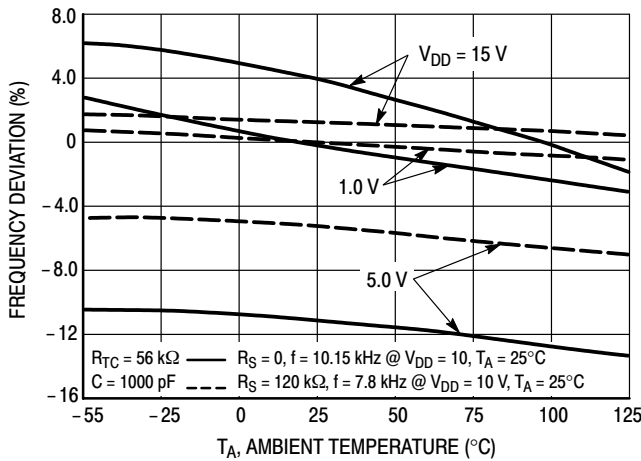


Figure 4. RC Oscillator Stability

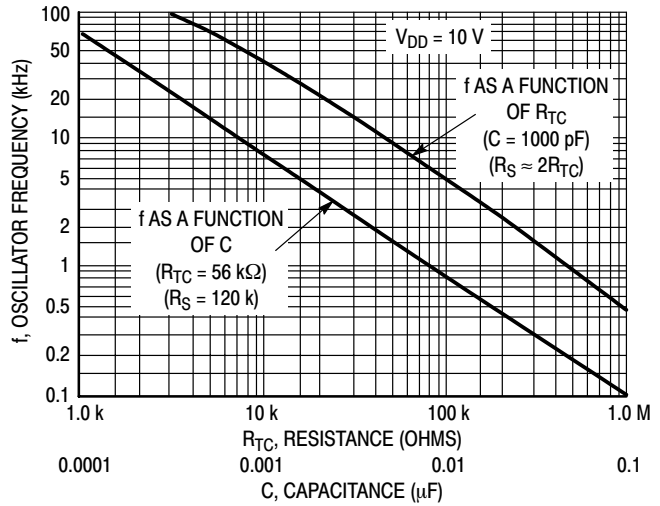


Figure 5. RC Oscillator Frequency as a Function of R_{TC} and C

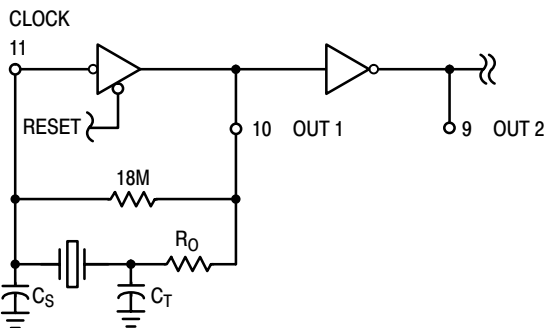


Figure 6. Typical Crystal Oscillator Circuit

Table 2. Typical Data for Crystal Oscillator Circuit

Characteristic	500 kHz Circuit	32 kHz Circuit	Unit
Crystal Characteristics			
Resonant Frequency	500	32	kHz
Equivalent Resistance, R_S	1.0	6.2	k Ω
External Resistor/Capacitor Values			
R_0	47	750	k Ω
C_T	82	82	pF
C_S	20	20	pF
Frequency Stability			
Frequency Changes as a Function of V_{DD} ($T_A = 25^\circ\text{C}$)			
V_{DD} Change from 5.0 V to 10 V	+6.0	+2.0	ppm
V_{DD} Change from 10 V to 15 V	+2.0	+2.0	ppm
Frequency Change as a Function of Temperature ($V_{DD} = 10 \text{ V}$)			
T_A Change from -55°C to $+25^\circ\text{C}$ Complete Oscillator (Note 6)	+100	+120	ppm
T_A Change from $+25^\circ\text{C}$ to $+125^\circ\text{C}$ Complete Oscillator (Note 6)	-160	-560	ppm

6. Complete oscillator includes crystal, capacitors, and resistors.

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ORDERING INFORMATION

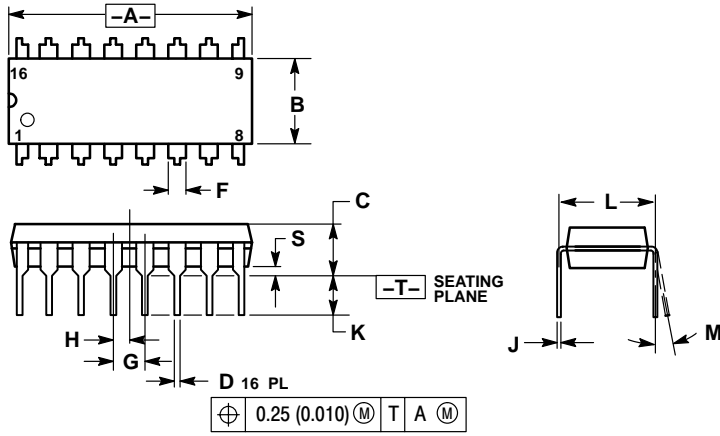
Device	Package	Shipping†
MC14060BCP	PDIP-16	500 Units / Rail
MC14060BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14060BD	SOIC-16	48 Units / Rail
MC14060BDR2	SOIC-16	2500 / Tape & Reel
MC14060BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC14060BFEL	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel
MC14060BDTR2	TSSOP-16 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

PDIP-16 P SUFFIX CASE 648-08 ISSUE T

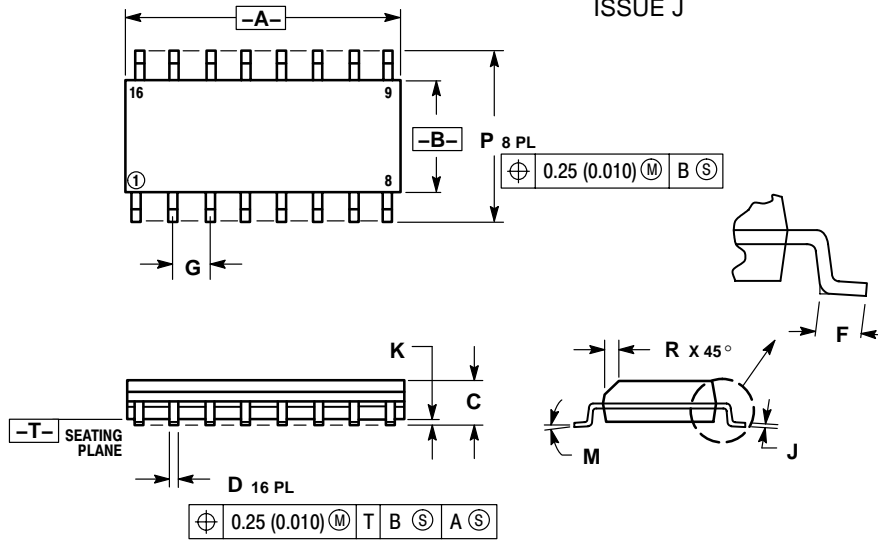


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16 D SUFFIX PLASTIC SOIC PACKAGE CASE 751B-05 ISSUE J



NOTES:

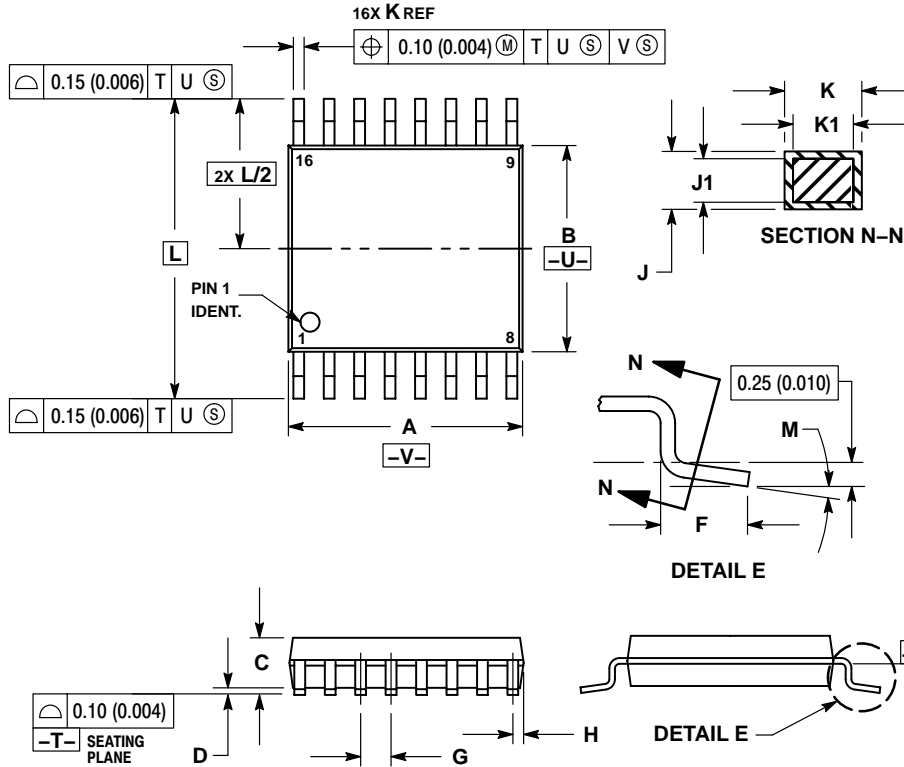
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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PACKAGE DIMENSIONS

TSSOP-16
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948F-01
ISSUE O



NOTES:

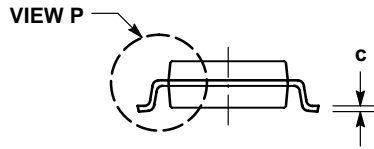
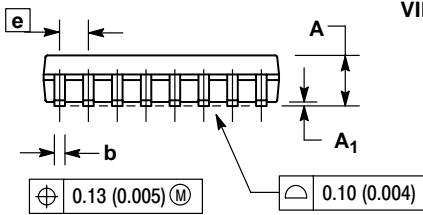
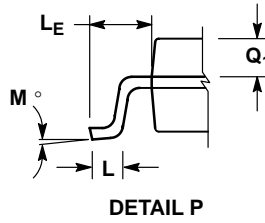
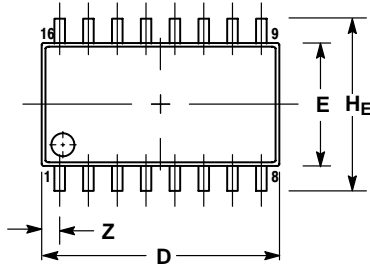
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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PACKAGE DIMENSIONS

SOEIAJ-16
F SUFFIX
PLASTIC EIAJ SOIC PACKAGE
CASE 966-01
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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