



# 4-BIT PARALLEL ACCESS SHIFT REGISTER

The functional characteristics of the MC74F195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting, and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

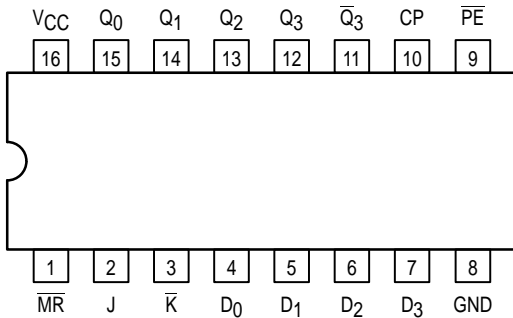
The MC74F195 operates in two primary modes, shift right ( $Q_0$ - $Q_1$ ) and parallel load, which are controlled by the state of the Parallel Enable ( $\overline{PE}$ ) input. Serial data enters the first flip-flop ( $Q_0$ ) via the J and  $\overline{K}$  inputs when the  $\overline{PE}$  input is HIGH, and is shifted 1 bit in the direction  $Q_0$ - $Q_1$ - $Q_2$ - $Q_3$  following each LOW-to-HIGH clock transition. The J and  $\overline{K}$  inputs provide the flexibility of the JK type input is made for special applications, and by tying the two pins together the simple D-type input is made for general applications. The device appears as four common clocked D flip-flops when the  $\overline{PE}$  input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs ( $D_0$ - $D_3$ ) is transferred to the respective  $Q_0$ - $Q_3$  outputs. Shift left operation ( $Q_3$ - $Q_2$ ) can be achieved by tying the  $Q_n$  outputs to the  $D_{n-1}$  inputs and holding the  $\overline{PE}$  input LOW.

All parallel and serial data transfers are synchronous, occurring after each LOW-to-HIGH clock transition. The MC74F195 utilizes edge-triggering; therefore, there is no restriction on the activity of the J,  $\overline{K}$ ,  $D_n$ , and  $\overline{PE}$  inputs for logic operation, other than the setup and hold time requirements.

A LOW on the asynchronous Master Reset ( $\overline{MR}$ ) input sets all Q outputs LOW, independent of any other input condition.

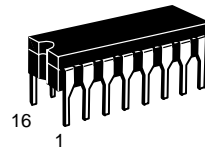
- Shift Right and Parallel Load Capability
- J- $\overline{K}$  (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset

### CONNECTION DIAGRAM DIP

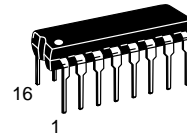


## MC74F195

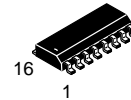
### 4-BIT PARALLEL ACCESS SHIFT REGISTER FAST™ SCHOTTKY TTL



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

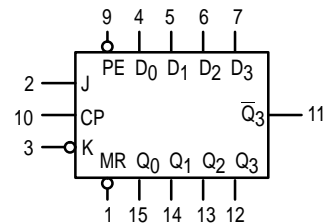


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

|           |         |
|-----------|---------|
| MC74FXXXJ | Ceramic |
| MC74FXXXN | Plastic |
| MC74FXXXD | SOIC    |

### LOGIC SYMBOL



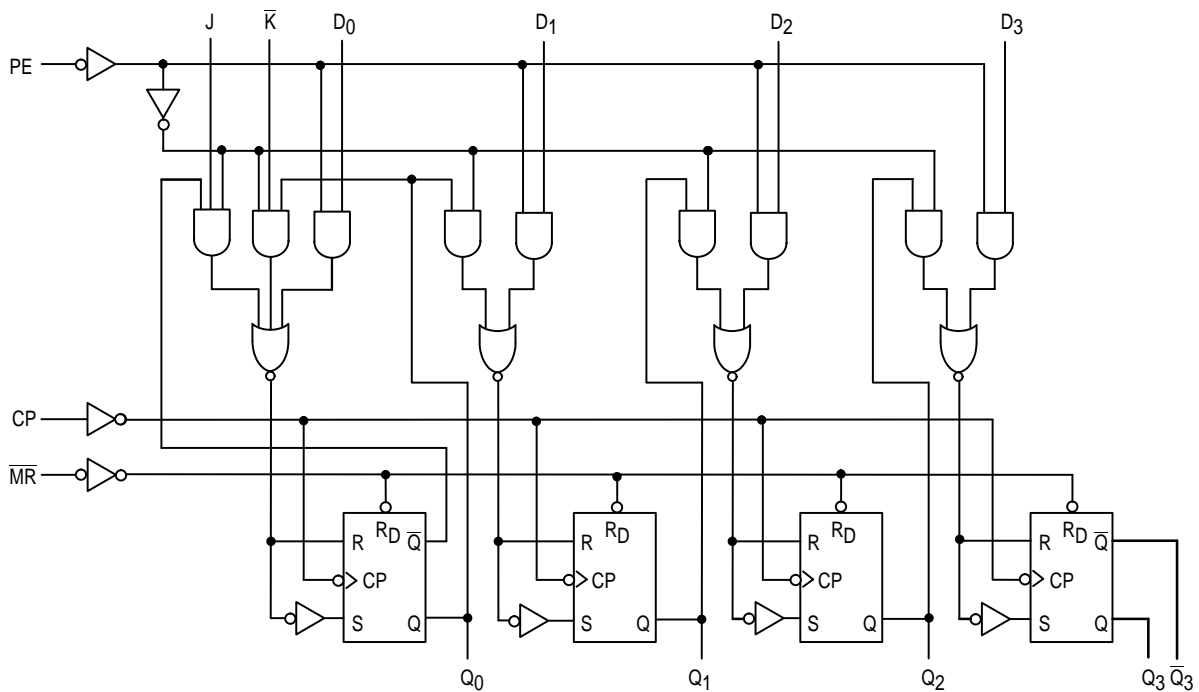
$V_{CC}$  = PIN 16  
GND = PIN 8

# MC74F195

## GUARANTEED OPERATING RANGES

| Symbol          | Parameter                           |    | Min | Typ | Max  | Unit |
|-----------------|-------------------------------------|----|-----|-----|------|------|
| V <sub>CC</sub> | Supply Voltage                      | 74 | 4.5 | 5.0 | 5.5  | V    |
| T <sub>A</sub>  | Operating Ambient Temperature Range | 74 | 0   | 25  | 70   | °C   |
| I <sub>OH</sub> | Output Current — High               | 74 |     |     | -1.0 | mA   |
| I <sub>OL</sub> | Output Current — Low                | 74 |     |     | 20   | mA   |

## LOGIC DIAGRAM



## FUNCTION TABLE

| Operating Modes           | Inputs          |    |                 |   |                |                | Outputs          |                |                |                |                  |
|---------------------------|-----------------|----|-----------------|---|----------------|----------------|------------------|----------------|----------------|----------------|------------------|
|                           | $\overline{MR}$ | CP | $\overline{PE}$ | J | $\overline{K}$ | D <sub>n</sub> | Q <sub>0</sub>   | Q <sub>1</sub> | Q <sub>2</sub> | Q <sub>3</sub> | $\overline{Q}_3$ |
| Asynchronous Reset        | L               | X  | X               | X | X              | X              | L                | L              | L              | L              | H                |
| Shift, Set First Stage    | H               | ↑  | h               | h | h              | X              | H                | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | $\overline{q}_2$ |
| Shift, Reset First Stage  | H               | ↑  | h               | l | l              | X              | L                | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | $\overline{q}_2$ |
| Shift, Toggle First Stage | H               | ↑  | h               | h | l              | X              | $\overline{q}_0$ | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | $\overline{q}_2$ |
| Shift, Retain First Stage | H               | ↑  | h               | l | h              | X              | q <sub>0</sub>   | q <sub>0</sub> | q <sub>1</sub> | q <sub>2</sub> | $\overline{q}_2$ |
| Parallel Load             | H               | ↑  | l               | X | X              | d <sub>n</sub> | d <sub>0</sub>   | d <sub>1</sub> | d <sub>2</sub> | d <sub>3</sub> | $\overline{d}_3$ |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

d<sub>n</sub> (q<sub>n</sub>) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

↑ = LOW-to-HIGH clock transition

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## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter                             | Limits |     |      | Unit | Test Conditions               |                          |
|-----------------|---------------------------------------|--------|-----|------|------|-------------------------------|--------------------------|
|                 |                                       | Min    | Typ | Max  |      |                               |                          |
| V <sub>IH</sub> | Input HIGH Voltage                    | 2.0    |     |      | V    | Guaranteed Input HIGH Voltage |                          |
| V <sub>IL</sub> | Input LOW Voltage                     |        |     | 0.8  | V    | Guaranteed Input LOW Voltage  |                          |
| V <sub>IK</sub> | Input Clamp Diode Voltage             |        |     | -1.2 | V    | I <sub>IN</sub> = -18 mA      | V <sub>CC</sub> = MIN    |
| V <sub>OH</sub> | Output HIGH Voltage                   | 74     | 2.5 |      | V    | I <sub>OH</sub> = -1.0 mA     | V <sub>CC</sub> = 4.5 V  |
|                 |                                       | 74     | 2.7 |      | V    |                               | V <sub>CC</sub> = 4.75 V |
| V <sub>OL</sub> | Output LOW Voltage                    |        |     | 0.5  | V    | I <sub>OL</sub> = 20 mA       | V <sub>CC</sub> = 4.5 V  |
| I <sub>IH</sub> | Input HIGH Current                    |        |     | 20   | μA   | V <sub>IN</sub> = 2.7 V       | V <sub>CC</sub> = MAX    |
|                 |                                       |        |     | 100  |      | V <sub>IN</sub> = 7.0 V       |                          |
| I <sub>IL</sub> | Input LOW Current                     |        |     | -0.6 | mA   | V <sub>CC</sub> = MAX         |                          |
| I <sub>OS</sub> | Output Short Circuit Current (Note 2) | -60    |     | -150 | mA   | V <sub>OUT</sub> = 0 V        | V <sub>CC</sub> = MAX    |
| I <sub>CC</sub> | Power Supply Current                  |        |     | 38   | mA   | V <sub>CC</sub> = MAX         |                          |

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS

| Symbol           | Parameter                    | 54/74F   |      | 74F  |     | Unit |
|------------------|------------------------------|--|------|--|-----|------|
|                  |                              | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0 V<br>C <sub>L</sub> = 50 pF |      | T <sub>A</sub> = 0°C to +70°C<br>V <sub>CC</sub> = 5.0 V ± 10%<br>C <sub>L</sub> = 50 pF |     |      |
|                  |                              | Min  | Max  | Min  | Max |      |
| f <sub>max</sub> |                              | 105  |      | 90   |     | MHz  |
| t <sub>PLH</sub> | Propagation Delay            | 2.5  | 7.0  | 2.5  | 8.0 | ns   |
| t <sub>PHL</sub> | CP to Q/Q̄                   | 2.5  | 8.0  | 2.5  | 9.0 |      |
| t <sub>PHL</sub> | Propagation Delay, MR̄ to Q  | 3.0  | 10   | 3.0  | 11  | ns   |
| t <sub>PLH</sub> | Propagation Delay, MR̄ to Q̄ | 3.0  | 10.5 | 3.0  | 11  | ns   |

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## AC OPERATING REQUIREMENTS

| Symbol             | Parameter                                     | 74F  |     | 74F   |     | Unit |
|--------------------|---|--|-----|---|-----|------|
|                    |   | T <sub>A</sub> = + 25°C<br>V <sub>CC</sub> = + 5.0 V<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = 0°C to + 70°C<br>V <sub>CC</sub> = 5.0 V ± 10%<br>C <sub>L</sub> = 50 pF |     |      |
|                    |   | Min  | Max | Min   | Max |      |
| t <sub>S</sub> (H) | Setup Time, HIGH or LOW J, K, D to CP         | 4.0  |     | 4.0   |     | ns   |
| t <sub>S</sub> (L) |   | 4.0  |     | 4.0   |     |      |
| t <sub>H</sub> (H) | Hold Time, HIGH or LOW J, K, D to CP          | 0  |     | 1.0   |     | ns   |
| t <sub>H</sub> (L) |   | 0  |     | 1.0   |     |      |
| t <sub>S</sub> (H) | Setup Time, HIGH or LOW $\overline{PE}$ to CP | 8.0  |     | 9.0   |     | ns   |
| t <sub>S</sub> (L) |   | 8.0  |     | 9.0   |     |      |
| t <sub>H</sub> (H) | Hold Time, HIGH or LOW $\overline{PE}$ to CP  | 0  |     | 0   |     | ns   |
| t <sub>H</sub> (L) |   | 0  |     | 0   |     |      |
| t <sub>w</sub> (H) | CP Pulse Width, HIGH                          | 5.0  |     | 5.5   |     | ns   |
| t <sub>w</sub> (L) | $\overline{MR}$ Pulse Width, LOW              | 5.0  |     | 5.0   |     | ns   |
| t <sub>rec</sub>   | Recovery Time, $\overline{MR}$ to CP          | 7.0  |     | 8.0   |     | ns   |