# **Dual Low-Voltage CMOS 2-to-4 Decoder/Demultiplexer**

# With 5V-Tolerant Inputs

The MC74LCX139 is a high performance, 2–to–4 decoder/demultiplexer operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A VI specification of 5.5 V allows MC74LCX139 inputs to be safely driven from 5 V devices. The MC74LCX139 is suitable for memory address decoding and other TTL level bus oriented applications.

The MC74LCX139 high–speed 2–to–4 decoder/demultiplexer accepts two binary weighted inputs (A0, A1) and, when enabled, provides four mutually exclusive active–LOW outputs. The LCX139 features an active low Enable input. All outputs will be HIGH unless En is LOW. The LCX139 can be used as an 8–output demultiplexer by using one of the active–LOW Enable inputs as the data input and the other Enable input as a strobe. The Enable inputs which are not used must be permanently tied to ground.

Current drive capability is 24 mA at the outputs.

#### **Features**

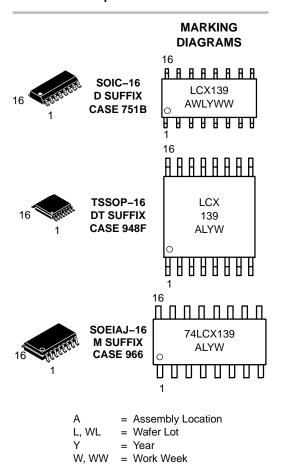
- Designed for 2.3 to 3.6 V V<sub>CC</sub> Operation
- 5 V Tolerant Inputs Interface Capability With 5 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V

Machine Model >200 V

• Pb-Free Packages are Available\*



http://onsemi.com



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

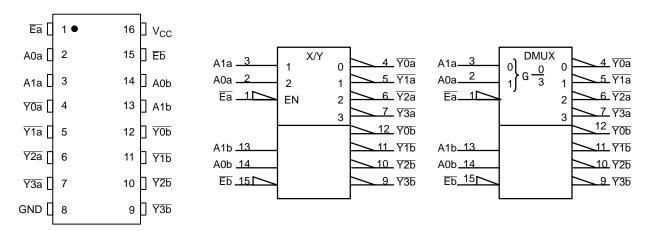


Figure 1. Pin Assignment

Figure 2. IEC Logic Diagram

#### **PIN NAMES**

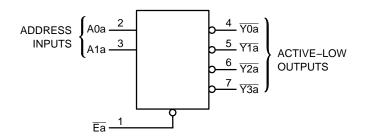
Pins	Function
A0n–A1n	Address Inputs
En	Enable Inputs
<del></del> <del>Y</del> 0n− <del>Y</del> 3n	Outputs

#### **TRUTH TABLE**

Inputs				Out	puts	
Ē	A1	A0	<u>Y0</u>	<u>Y1</u>	<u>Y2</u>	<u>Y3</u>
Н	Х	Χ	Н	Н	Н	Н
L	L	L	L	Н	Н	н
L	L	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	н
L	Н	Н	Н	Н	Н	L

H = High Voltage Level; L = Low Voltage Level;

Z = High Impedance State



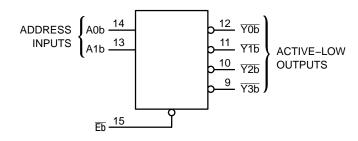


Figure 3. Logic Diagram

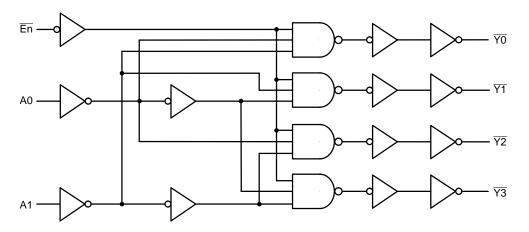


Figure 4. Expanded Logic Diagram (1/2 of Device)

#### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
VI	DC Input Voltage	$-0.5 \le V_1 \le +7.0$		V
Vo	DC Output Voltage	$-0.5 \le V_{O} \le V_{CC} + 0.5$	Output in HIGH or LOW State. (Note 1)	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
Io	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. I<sub>O</sub> absolute maximum rating must be observed.

#### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Pa	rameter	Min	Тур	Max	Unit
V <sub>CC</sub>	Supply Voltage	Operating Data Retention Only	2.0 1.5	2.3 to 3.3	3.6 3.6	V
VI	Input Voltage		0		5.5	V
Vo	Output Voltage	(HIGH or LOW State)	0		V <sub>CC</sub>	V
I <sub>OH</sub>	HIGH Level Output Current	$V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			-24 -12 -8	mA
I <sub>OL</sub>	LOW Level Output Current	$V_{CC} = 3.0 \text{ V} - 3.6 \text{ V}$ $V_{CC} = 2.7 \text{ V} - 3.0 \text{ V}$ $V_{CC} = 2.3 \text{ V} - 2.7 \text{ V}$			+24 +12 +8	mA
T <sub>A</sub>	Operating Free–Air Temperature		-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V	<sub>IN</sub> from 0.8 V to 2.0 V, V <sub>CC</sub> = 3.0 V	0		10	ns/V

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74LCX138D	SOIC-16	48 Units / Rail
MC74LCX138DR2	SOIC-16	2500 Tape & Reel
MC74LCX138DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DT	TSSOP-16*	96 Units / Rail
MC74LCX138DTR2	TSSOP-16*	2500 Tape & Reel
MC74LCX138M	SOEIAJ-16	48 Units / Rail
MC74LCX138MEL	SOEIAJ-16	2000 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

<sup>\*</sup>This package is inherently Pb-Free.

#### DC ELECTRICAL CHARACTERISTICS

	Characteristic		$T_A = -40^{\circ}C$ to $+85^{\circ}C$		
Symbol		Condition	Min	Max	Unit
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V	1.7		V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V	2.0		1
$V_{IL}$	LOW Level Input Voltage (Note 2)	2.3 V ≤ V <sub>CC</sub> ≤ 2.7 V		0.7	V
		2.7 V ≤ V <sub>CC</sub> ≤ 3.6 V		0.8	1
V <sub>OH</sub>	HIGH Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OL} = 100 \mu\text{A}$	V <sub>CC</sub> – 0.2		V
		$V_{CC} = 2.3 \text{ V}; I_{OH} = -8 \text{ mA}$	1.7		1
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -12 mA	2.2		1
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -18 mA	2.4		1
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -24 mA	2.2		1
V <sub>OL</sub>	LOW Level Output Voltage	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; \text{I}_{OL} = 100 \mu\text{A}$		0.2	V
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = 8 mA		0.7	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 12 mA		0.4	1
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA		0.4	1
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 24 mA		0.55	1
I <sub>I</sub>	Input Leakage Current	$2.3 \text{ V} \le \text{V}_{CC} \le 3.6 \text{ V}; 0 \text{ V} \le \text{V}_{I} \le 5.5 \text{ V}$		±5	μΑ
I <sub>CC</sub>	Quiescent Supply Current	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_I = \text{GND or } V_{CC}$		10	μΑ
		$2.3 \le V_{CC} \le 3.6 \text{ V}; 3.6 \le V_{I} \text{ or } V_{O} \le 5.5 \text{ V}$		±10	1
$\Delta I_{CC}$	Increase in I <sub>CC</sub> per Input	$2.3 \le V_{CC} \le 3.6 \text{ V}; V_{IH} = V_{CC} - 0.6 \text{ V}$		500	μΑ

<sup>2.</sup> These values of V<sub>I</sub> are used to test DC electrical characteristics only.

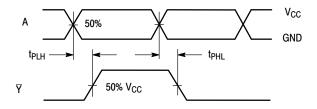
### AC CHARACTERISTICS $t_R = t_F = 2.5 \text{ ns}; C_L = 50 \text{ pF}; R_L = 500 \ \Omega$

			Limits					
			T <sub>A</sub> = -40°C to +85°C					1
		V <sub>CC</sub> = 3.0 V to 3.6 V V <sub>CC</sub> = 2		2.7 V	V <sub>CC</sub> = 2.3	V to 2.7 V	1	
		C <sub>L</sub> = 50 pF		30pF	1			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub>	Propagation Delay	0.8	6.2	1.0	7.3	0.8	9.3	ns
t <sub>PHL</sub>	A to Y	8.0	6.2	1.0	7.3	8.0	9.3	ns
t <sub>PLH</sub>	Propagation Delay	0.8	4.7	1.0	5.2	0.8	7.2	ns
t <sub>PHL</sub>	E to Y	8.0	4.7	1.0	5.2	8.0	7.2	ns
toshl	Output-to-Output Skew (Note 3)		1.0					ns
toslh			1.0					ns

<sup>3.</sup> Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

#### **CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	$V_{CC} = 3.3 \text{ V}, V_{I} = 0 \text{ V or } V_{CC}$	7	pF
C <sub>OUT</sub>	Output Capacitance	$V_{CC} = 3.3 \text{ V}, V_I = 0 \text{ V or } V_{CC}$	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, $V_{CC}$ = 3.3 V, $V_{I}$ = 0 V or $V_{CC}$	25	pF



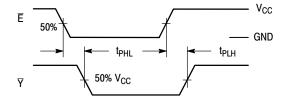
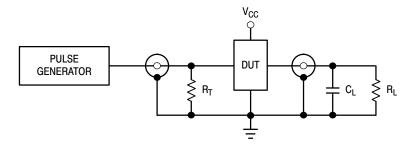


Figure 5. Waveform 1 Prop Delays

Figure 6. Waveform 2 Output Enable

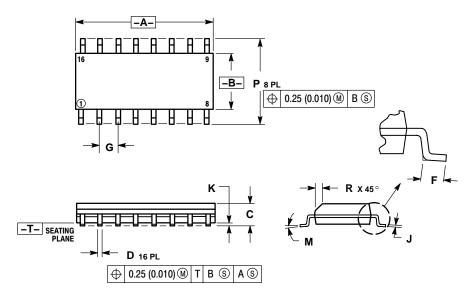


 $C_L$  = 50 pF or equivalent (Includes jig and probe capacitance)  $R_L$  =  $R_1$  = 500  $\Omega$  or equivalent  $R_T$  =  $Z_{OUT}$  of pulse generator (typically 50  $\Omega)$ 

Figure 7. Test Circuit

#### PACKAGE DIMENSIONS

#### SOIC-16 **D SUFFIX** CASE 751B-05 **ISSUE J**



- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 114.5M, 1982.

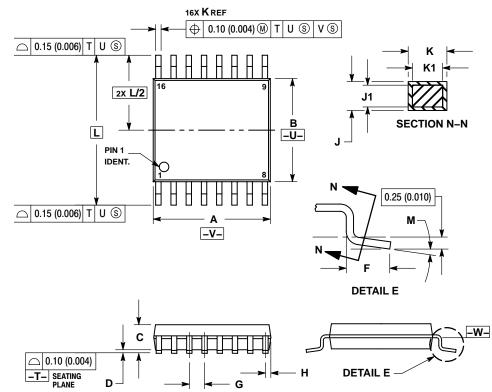
  CONTROLLING DIMENSION: MILLIMETER.

  DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

  MAXIMUM MOLD PROTRUSION 0.15 (0.006) DED 9:10
- PER SIDE.
  DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.127 (0.005) TOTAL
  IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

#### TSSOP-16 **DT SUFFIX** CASE 948F-01 **ISSUE O**



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH.
  PROTRUSIONS OR GATE BURRS. MOLD FLASH
  OR GATE BURRS SHALL NOT EXCEED 0.15
- (0.006) PER SIDE.

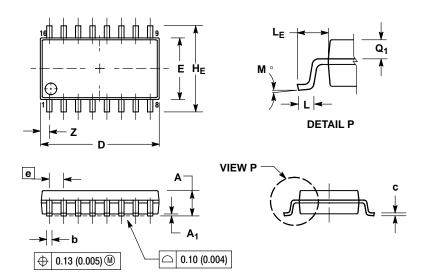
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

  5. DIMENSION K DOES NOT INCLUDE DAMBAR
- PROTRUSION. ALLOWABLE DAMBAR
  PROTRUSION. SHALL BE 0.08 (0.003) TOTAL IN
  EXCESS OF THE K DIMENSION AT MAXIMUM
  MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
  DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	METERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
М	0°	8°	0°	8°

#### **PACKAGE DIMENSIONS**

SOEIAJ-16 **M SUFFIX** CASE 966-01 **ISSUE O** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z		0.78		0.031

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