

# MC74LVX259

## 8-Bit Addressable Latch/1-of-8 Decoder CMOS Logic Level Shifter with LSTTL-Compatible Inputs

The MC74LVX259 is an 8-bit Addressable Latch fabricated with silicon gate CMOS technology.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The LVX259 is designed for general purpose storage applications in digital systems. The device has four modes of operation as shown in the mode selection table. In the addressable latch mode, the data on Data In is written into the addressed latch. The addressed latch follows the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs. In the one-of-eight decoding or demultiplexing mode, the addressed output follows the state of Data In with all other outputs in the LOW state. In the Reset mode, all outputs are LOW and unaffected by the address and data inputs. When operating the LVX259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

The MC74LVX259 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the MC74LVX259 to be used to interface 5 V circuits to 3 V circuits.

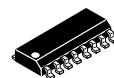
- High Speed:  $t_{PD} = 7.0 \text{ ns}$  (Typ) at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 2 \mu\text{A}$  (Max) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- CMOS-Compatible Outputs:  $V_{OH} > 0.8 V_{CC}$ ;  $V_{OL} < 0.1 V_{CC}$  @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V



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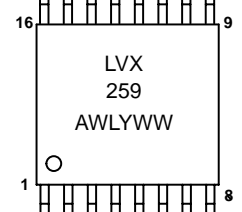
### MARKING DIAGRAMS



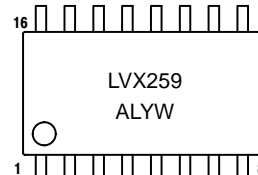
SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



SOIC EIAJ-16  
M SUFFIX  
CASE 966



A = Assembly Location  
WL or L = Wafer Lot  
YY or Y = Year  
WW or W = Work Week

### ORDERING INFORMATION

| Device         | Package    | Shipping        |
|----------------|------------|-----------------|
| MC74LVX259D    | SO-16      | 48 Units/Rail   |
| MC74LVX259DR2  | SO-16      | 2500 Units/Reel |
| MC74LVX259DT   | TSSOP-16   | 96 Units/Rail   |
| MC74LVX259DTR2 | TSSOP-16   | 2000 Units/Reel |
| MC74LVX259M    | SO EIAJ-16 | 48 Units/Rail   |
| MC74LVX259MEL  | SO EIAJ-16 | 2000 Units/Reel |

# MC74LVX259

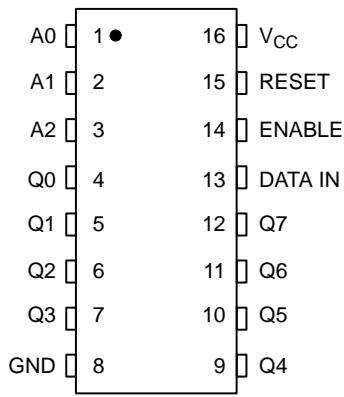


Figure 1. Pin Assignment

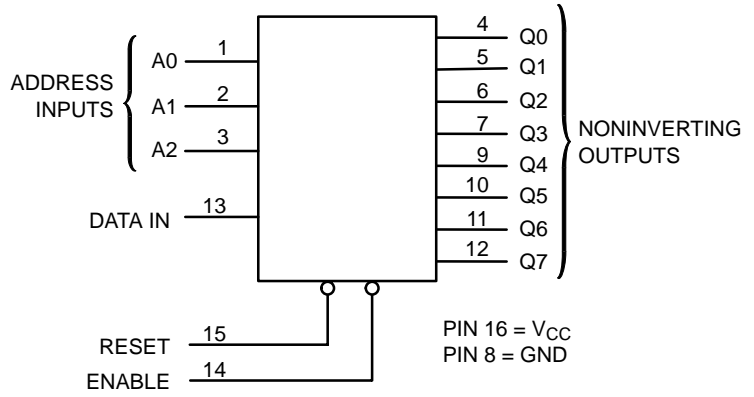


Figure 2. Logic Diagram

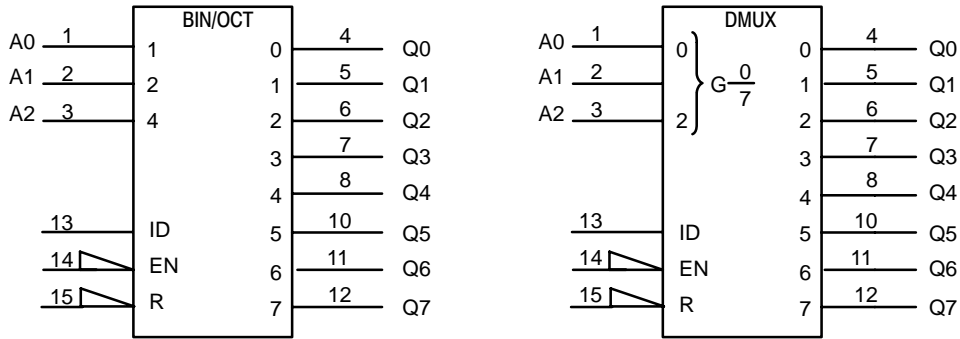


Figure 3. IEC Logic Symbol

MODE SELECTION TABLE

| Enable | Reset | Mode                 |
|--------|-------|----------------------|
| L      | H     | Addressable Latch    |
| H      | H     | Memory               |
| L      | L     | 8-Line Demultiplexer |
| H      | L     | Reset                |

LATCH SELECTION TABLE

| Address Inputs |   |   | Latch Addressed |
|----------------|---|---|-----------------|
| C              | B | A |                 |
| L              | L | L | Q0              |
| L              | L | H | Q1              |
| L              | H | L | Q2              |
| L              | H | H | Q3              |
| H              | L | L | Q4              |
| H              | L | H | Q5              |
| H              | H | L | Q6              |
| H              | H | H | Q7              |

# MC74LVX259

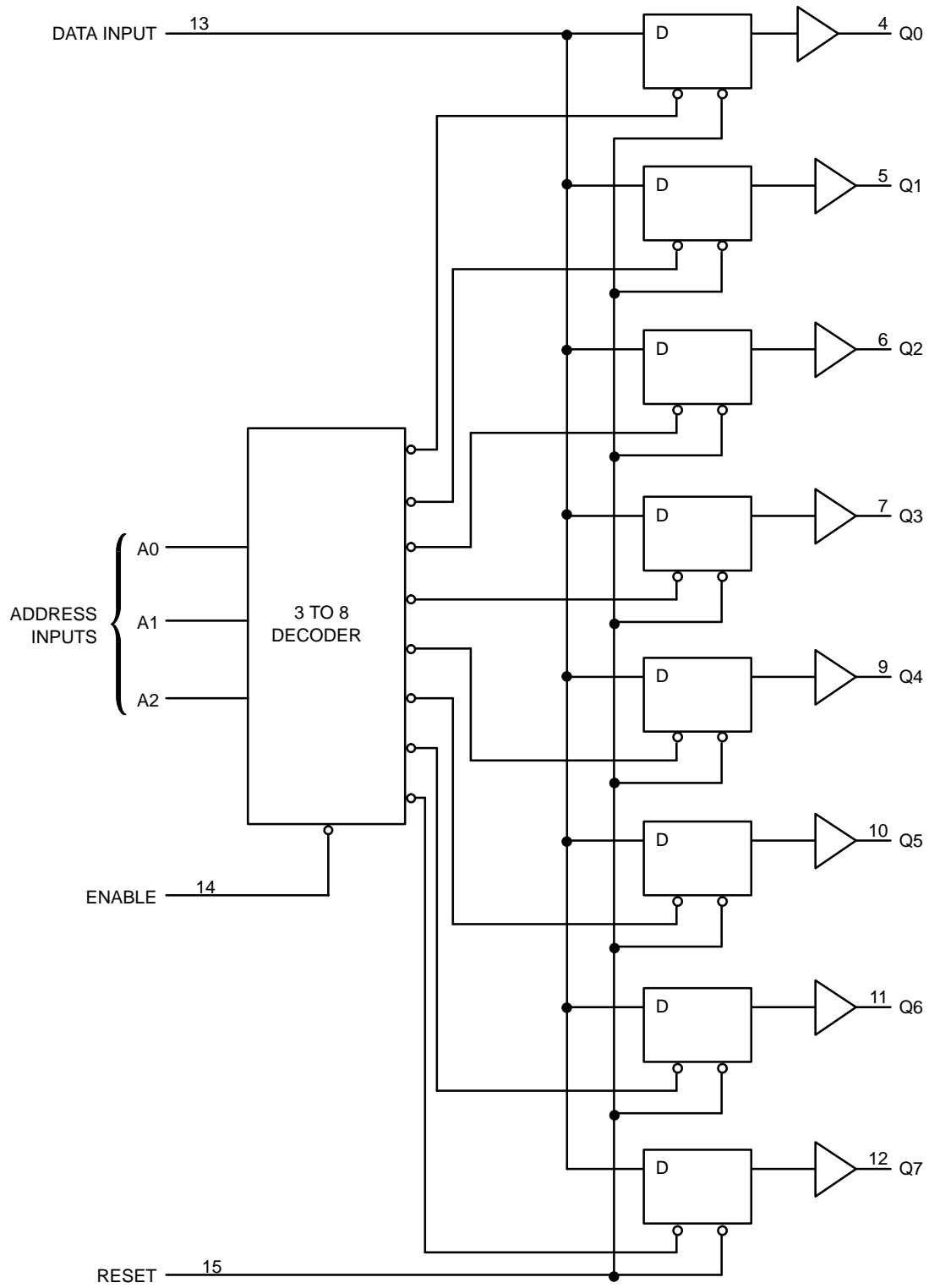


Figure 4. Expanded Logic Diagram

# MC74LVX259

## MAXIMUM RATINGS (Note 1.)

| Symbol                | Parameter                                       | Value   | Unit        |
|-----------------------|---|---|-------------|
| V <sub>CC</sub>       | Positive DC Supply Voltage                      | -0.5 to +7.0  | V           |
| V <sub>IN</sub>       | Digital Input Voltage                           | -0.5 to +7.0  | V           |
| V <sub>OUT</sub>      | DC Output Voltage                               | -0.5 to V <sub>CC</sub> +0.5  | V           |
| I <sub>IK</sub>       | Input Diode Current                             | -20   | mA          |
| I <sub>OK</sub>       | Output Diode Current                            | ± 20  | mA          |
| I <sub>OUT</sub>      | DC Output Current, per Pin                      | ± 25  | mA          |
| I <sub>CC</sub>       | DC Supply Current, V <sub>CC</sub> and GND Pins | ± 75  | mA          |
| P <sub>D</sub>        | Power Dissipation in Still Air                  | SOIC Package<br>200<br>TSSOP<br>180   | mW          |
| T <sub>STG</sub>      | Storage Temperature Range                       | -65 to +150   | °C          |
| V <sub>ESD</sub>      | ESD Withstand Voltage                           | Human Body Model (Note 2.)<br>>2000<br>Machine Model (Note 3.)<br>>200<br>Charged Device Model (Note 4.)<br>>2000 | V           |
| I <sub>LATCH-UP</sub> | Latch-Up Performance                            | Above V <sub>CC</sub> and Below GND at 125°C (Note 5.)  | ± 300<br>mA |
| θ <sub>JA</sub>       | Thermal Resistance, Junction to Ambient         | SOIC Package<br>143<br>TSSOP<br>164   | °C/W        |

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
2. Tested to EIA/JESD22-A114-A
3. Tested to EIA/JESD22-A115-A
4. Tested to JESD22-C101-A
5. Tested to EIA/JESD78

## RECOMMENDED OPERATING CONDITIONS

| Symbol                          | Characteristics                                | Min | Max             | Unit |
|---------------------------------|--|-----|-----------------|------|
| V <sub>CC</sub>                 | DC Supply Voltage                              | 2.0 | 3.6             | V    |
| V <sub>IN</sub>                 | DC Input Voltage                               | 0   | 5.5             | V    |
| V <sub>OUT</sub>                | DC Output Voltage                              | 0   | V <sub>CC</sub> | V    |
| T <sub>A</sub>                  | Operating Temperature Range, all Package Types | -40 | 85              | °C   |
| t <sub>r</sub> , t <sub>f</sub> | Input Rise or Fall Time                        | 0   | 100             | ns/V |

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## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Condition                                | V <sub>CC</sub><br>(V) | T <sub>A</sub> = 25°C  |     |  | -40°C ≤ T <sub>A</sub> ≤ 85°C                                      |  | Unit |
|-----------------|--|--|------------------------|--|-----|--|--|--|------|
|                 |  |  |                        | Min  | Typ | Max  | Min  | Max  |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage               |  | 2.0<br>3.0<br>3.6      | 0.75 V <sub>CC</sub><br>0.7 V <sub>CC</sub><br>0.7 V <sub>CC</sub> |     |  | 0.75 V <sub>CC</sub><br>0.7 V <sub>CC</sub><br>0.7 V <sub>CC</sub> |  | V    |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage                |  | 2.0<br>3.0<br>3.6      |  |     | 0.25 V <sub>CC</sub><br>0.3 V <sub>CC</sub><br>0.3 V <sub>CC</sub> |  | 0.25 V <sub>CC</sub><br>0.3 V <sub>CC</sub><br>0.3 V <sub>CC</sub> | V    |
| V <sub>OH</sub> | High-Level Output Voltage                      | I <sub>OH</sub> = -50 μA                 | 2.0                    | 1.9  | 2.0 |  | 1.9  |  | V    |
|                 |  | I <sub>OH</sub> = -50 μA                 | 3.0                    | 2.9  | 3.0 |  | 2.9  |  |      |
|                 |  | I <sub>OH</sub> = -4 mA                  | 3.0                    | 2.58   |     |  | 2.48   |  |      |
| V <sub>OL</sub> | Low-Level Output Voltage                       | I <sub>OL</sub> = 50 μA                  | 2.0                    |  | 0.0 | 0.1  |  | 0.1  | V    |
|                 |  | I <sub>OL</sub> = 50 μA                  | 3.0                    |  | 0.0 | 0.1  |  | 0.1  |      |
|                 |  | I <sub>OL</sub> = 4 mA                   | 3.0                    |  |     | 0.36   |  | 0.44   |      |
| I <sub>IN</sub> | Input Leakage Current                          | V <sub>IN</sub> = 5.5 V or GND           | 0 to 3.6               |  |     | ±0.1   |  | ±1.0   | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per package) | V <sub>IN</sub> = V <sub>CC</sub> or GND | 3.6                    | 1.0  | 1.0 | 2.0  |  |  | μA   |

## AC ELECTRICAL CHARACTERISTICS Input t<sub>r</sub> = t<sub>f</sub> = 3.0 ns

| Symbol                                 | Parameter   | Test Conditions   | T <sub>A</sub> = 25°C |            |             | -40°C ≤ T <sub>A</sub> ≤ 85°C |              | Unit |
|--|---|---|-----------------------|------------|-------------|-------------------------------|--------------|------|
|  |   |   | Min                   | Typ        | Max         | Min                           | Max          |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Data to Output (Figures 5 and 9)           | V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF         |                       | 6.3<br>9.0 | 9.0<br>14.0 | 1.0<br>1.0                    | 12.0<br>15.0 | ns   |
|  |   | V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 5.6<br>8.0 | 8.0<br>12.0 | 1.0<br>1.0                    | 11.0<br>14.0 |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Address Select to Output (Figures 6 and 9) | V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF         |                       | 6.3<br>9.0 | 9.0<br>14.0 | 1.0<br>1.0                    | 12.0<br>15.0 | ns   |
|  |   | V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 5.6<br>8.0 | 8.0<br>12.0 | 1.0<br>1.0                    | 11.0<br>14.0 |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Enable to Output (Figures NO TAG and 9)    | V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF         |                       | 6.3<br>9.0 | 9.0<br>14.0 | 1.0<br>1.0                    | 12.0<br>15.0 | ns   |
|  |   | V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 5.6<br>8.0 | 9.0<br>12.0 | 1.0<br>1.0                    | 11.0<br>14.0 |      |
| t <sub>PHL</sub>                       | Maximum Propagation Delay, Reset to Output (Figures 7 and 9)          | V <sub>CC</sub> = 2.7 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF         |                       | 6.3<br>9.0 | 9.0<br>14.0 | 1.0<br>1.0                    | 12.0<br>15.0 | ns   |
|  |   | V <sub>CC</sub> = 3.3 V ± 0.3 V    C <sub>L</sub> = 15pF<br>C <sub>L</sub> = 50pF |                       | 5.6<br>8.0 | 9.0<br>12.0 | 1.0<br>1.0                    | 11.0<br>14.0 |      |
| C <sub>IN</sub>                        | Maximum Input Capacitance   |   |                       | 6          | 10          |                               | 10           | pF   |

| C <sub>PD</sub> | Power Dissipation Capacitance (Note 6.) | Typical @ 25°C, V <sub>CC</sub> = 3.3 V |  | pF |
|-----------------|---|---|--|----|
|                 |   | 30                                      |  |    |
|                 |   |   |  |    |

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>. C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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## TIMING REQUIREMENTS Input $t_r = t_f = 3.0$ ns

| Symbol     | Parameter  | Test Conditions                          | $T_A = 25^\circ\text{C}$ |     |     | $T_A = \leq 85^\circ\text{C}$ |     | Unit |
|------------|--|--|--------------------------|-----|-----|-------------------------------|-----|------|
|            |  |  | Min                      | Typ | Max | Min                           | Max |      |
| $t_w$      | Minimum Pulse Width, Reset or Enable (Figure 8)              | $V_{CC} = 2.7\text{ V}$                  | 4.5                      |     |     | 5.0                           |     | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 4.5                      |     |     | 5.0                           |     |      |
| $t_{su}$   | Minimum Setup Time, Address or Data to Enable (Figure 8)     | $V_{CC} = 2.7\text{ V}$                  | 4.0                      |     |     | 4.0                           |     | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 3.0                      |     |     | 3.0                           |     |      |
| $t_h$      | Minimum Hold Time, Enable to Address or Data (Figure 7 or 8) | $V_{CC} = 2.7\text{ V}$                  | 2.0                      |     |     | 2.0                           |     | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 2.0                      |     |     | 2.0                           |     |      |
| $t_r, t_f$ | Maximum Input, Rise and Fall Times (Figure 5)                | $V_{CC} = 2.7\text{ V}$                  |                          |     | 400 |                               | 300 | ns   |
|            |  | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |                          |     | 300 |                               | 300 |      |

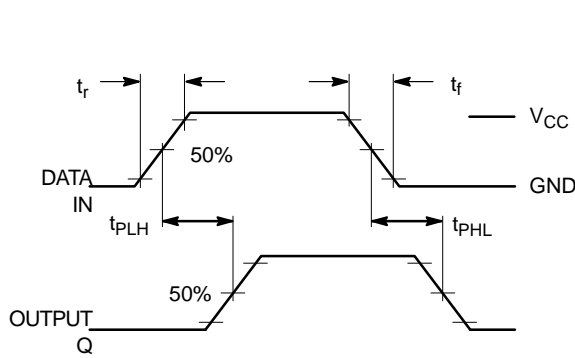


Figure 5. Switching Waveform

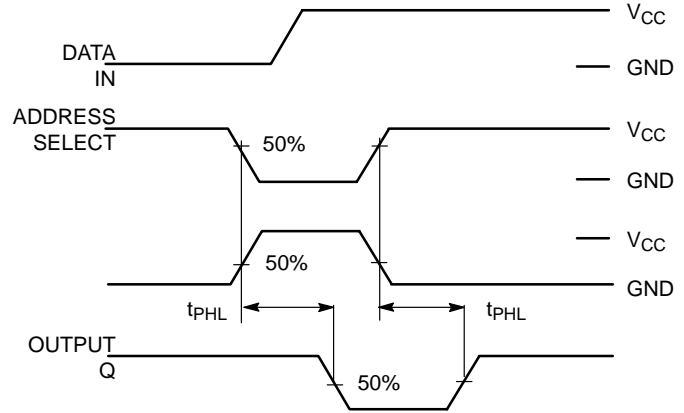


Figure 6. Switching Waveform

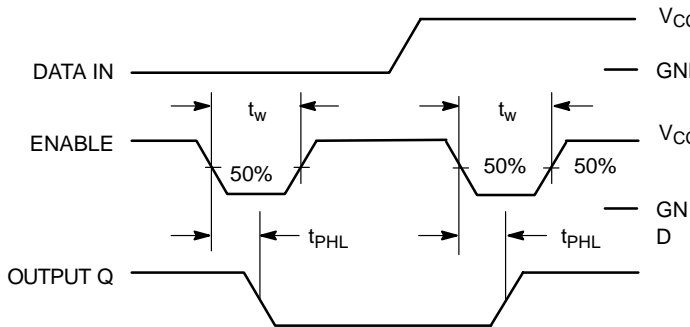


Figure 7. Switching Waveform

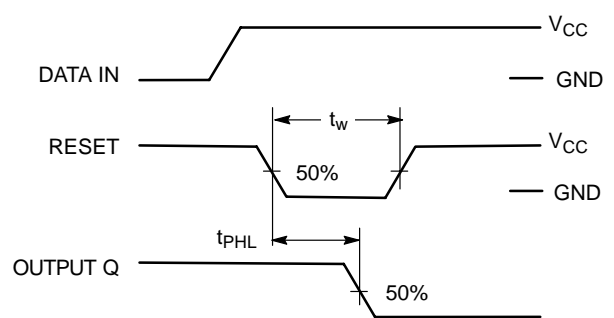


Figure 8. Switching Waveform

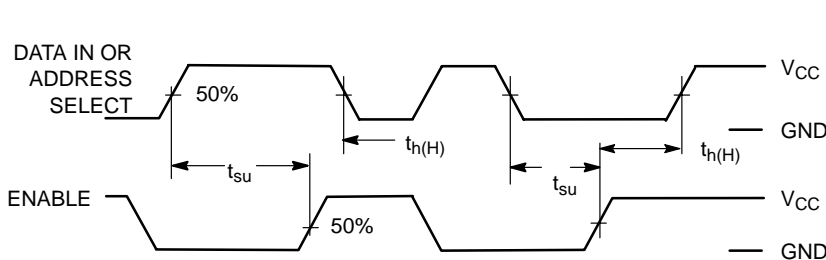
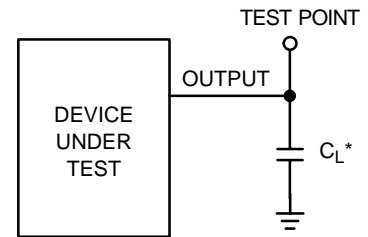


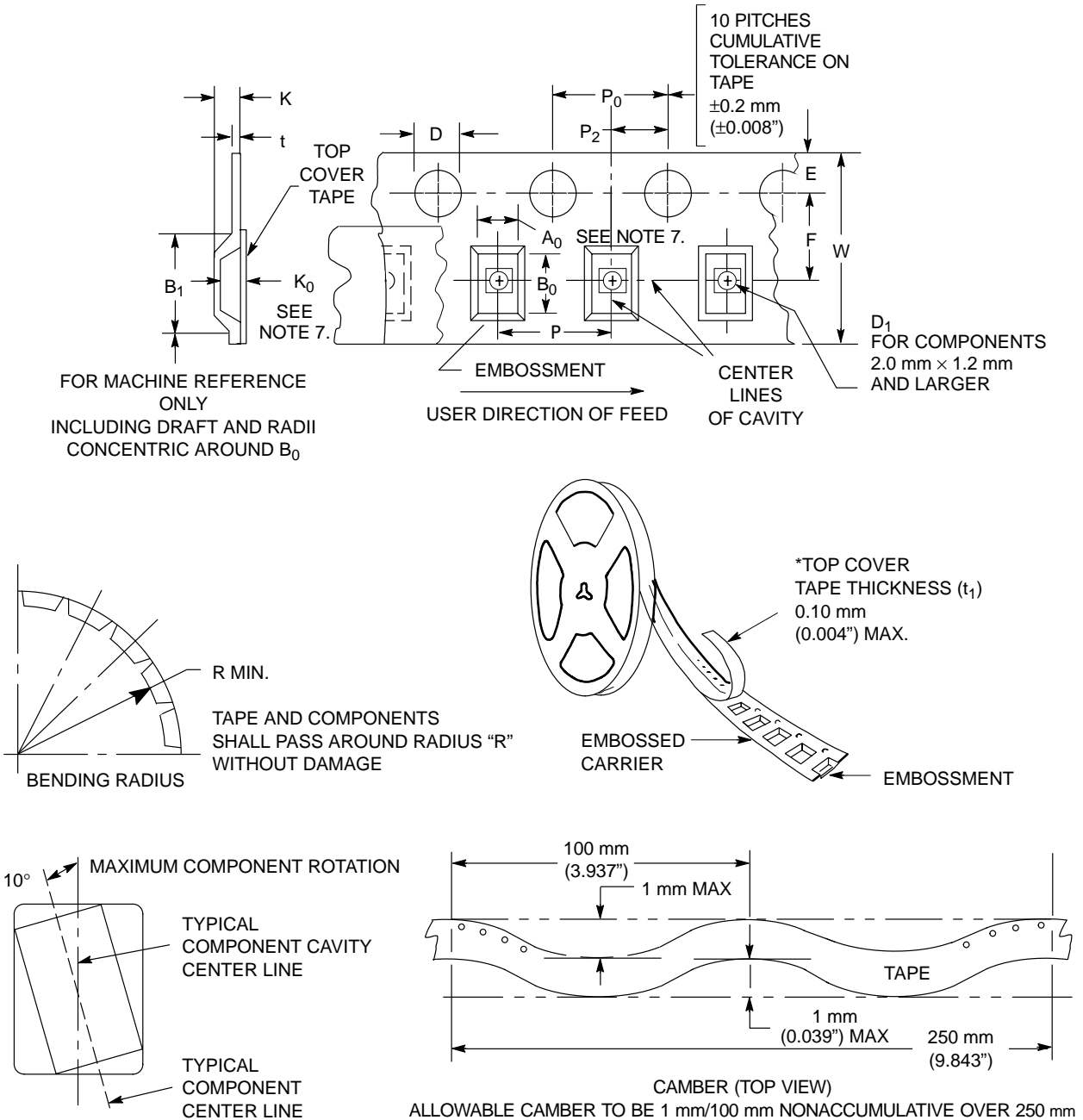
Figure 9. Switching Waveform



\*Includes all probe and jig capacitance

Figure 10. Test Circuit

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7.  $A_0$ ,  $B_0$ , and  $K_0$  are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

**Figure 11. Carrier Tape Specifications**

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## EMBOSSED CARRIER DIMENSIONS (See Notes 8. and 9.)

| Tape Size | B <sub>1</sub> Max  | D   | D <sub>1</sub>            | E                                     | F                                      | K                          | P  | P <sub>0</sub>                       | P <sub>2</sub>                       | R                | T                 | W                                     |
|-----------|---------------------|---|---------------------------|---------------------------------------|--|----------------------------|--|--------------------------------------|--------------------------------------|------------------|-------------------|---------------------------------------|
| 8 mm      | 4.35 mm<br>(0.179") | 1.5 mm<br>+ 0.1<br>-0.0<br>(0.059"<br>+0.004<br>-0.0) | 1.0 mm<br>Min<br>(0.179") | 1.75 mm<br>±0.1<br>(0.069<br>±0.004") | 3.5 mm<br>±0.5<br>(1.38<br>±0.002")    | 2.4 mm<br>Max<br>(0.094")  | 4.0 mm<br>±0.10<br>(0.157<br>±0.004")  | 4.0 mm<br>±0.1<br>(0.157<br>±0.004") | 2.0 mm<br>±0.1<br>(0.079<br>±0.004") | 25 mm<br>(0.98") | 0.6 mm<br>(0.024) | 8.3 mm<br>(0.327)                     |
| 12 mm     | 8.2 mm<br>(0.323")  |   | 1.5 mm<br>Min<br>(0.060)  |                                       | 5.5 mm<br>±0.5<br>(0.217<br>±0.002")   | 6.4 mm<br>Max<br>(0.252")  | 4.0 mm<br>±0.10<br>(0.157<br>±0.004")<br>8.0 mm<br>±0.10<br>(0.315<br>±0.004")   |                                      |                                      | 30 mm<br>(1.18") |                   | 12.0 mm<br>±0.3<br>(0.470<br>±0.012") |
| 16 mm     | 12.1 mm<br>(0.476") |   |                           |                                       | 7.5 mm<br>±0.10<br>(0.295<br>±0.004")  | 7.9 mm<br>Max<br>(0.311")  | 4.0 mm<br>±0.10<br>(0.157<br>±0.004")<br>8.0 mm<br>±0.10<br>(0.315<br>±0.004")<br>12.0 mm<br>±0.10<br>(0.472<br>±0.004") |                                      |                                      |                  |                   | 16.3 mm<br>(0.642)                    |
| 24 mm     | 20.1 mm<br>(0.791") |   |                           |                                       | 11.5 mm<br>±0.10<br>(0.453<br>±0.004") | 11.9 mm<br>Max<br>(0.468") | 16.0 mm<br>±0.10<br>(0.63<br>±0.004")  |                                      |                                      |                  |                   | 24.3 mm<br>(0.957)                    |

8. Metric Dimensions Govern—English are in parentheses for reference only.

9. A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity



# MC74LVX259

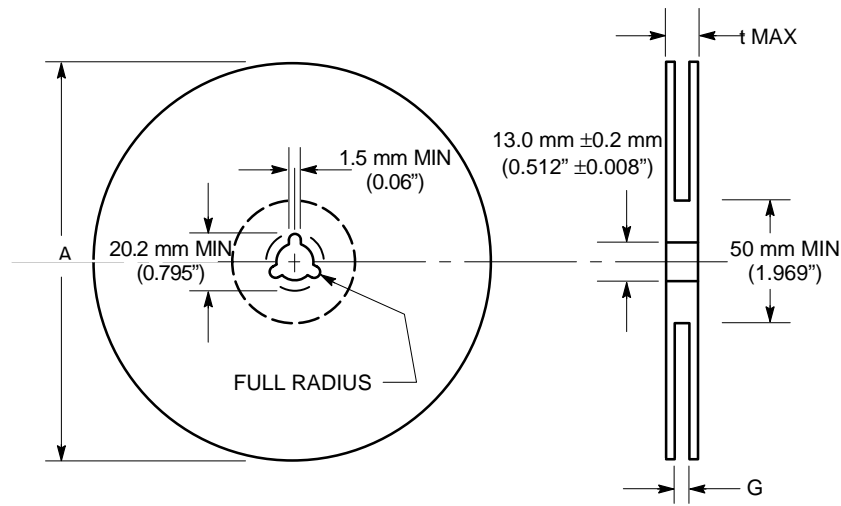


Figure 12. Reel Dimensions

## REEL DIMENSIONS

| Tape Size | T&R Suffix | A Max               | G  | t Max               |
|-----------|------------|---------------------|--|---------------------|
| 8 mm      | T1, T2     | 178 mm<br>(7")      | 8.4 mm, +1.5 mm, -0.0<br>(0.33" + 0.059", -0.00)   | 14.4 mm<br>(0.56")  |
| 8 mm      | T3, T4     | 330 mm<br>(13")     | 8.4 mm, +1.5 mm, -0.0<br>(0.33" + 0.059", -0.00)   | 14.4 mm<br>(0.56")  |
| 12 mm     | R2         | 330 mm<br>(13")     | 12.4 mm, +2.0 mm, -0.0<br>(0.49" + 0.079", -0.00)  | 18.4 mm<br>(0.72")  |
| 16 mm     | R2         | 360 mm<br>(14.173") | 16.4 mm, +2.0 mm, -0.0<br>(0.646" + 0.078", -0.00) | 22.4 mm<br>(0.882") |
| 24 mm     | R2         | 360 mm<br>(14.173") | 24.4 mm, +2.0 mm, -0.0<br>(0.961" + 0.078", -0.00) | 30.4 mm<br>(1.197") |

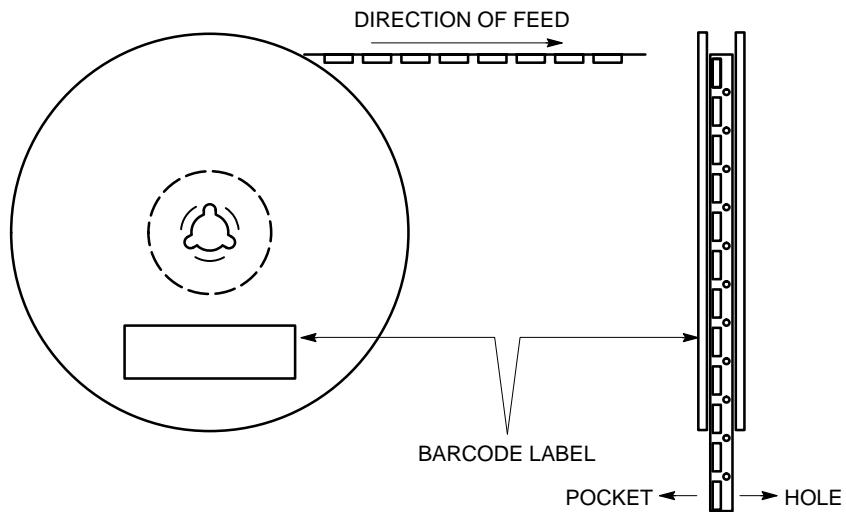


Figure 13. Reel Winding Direction

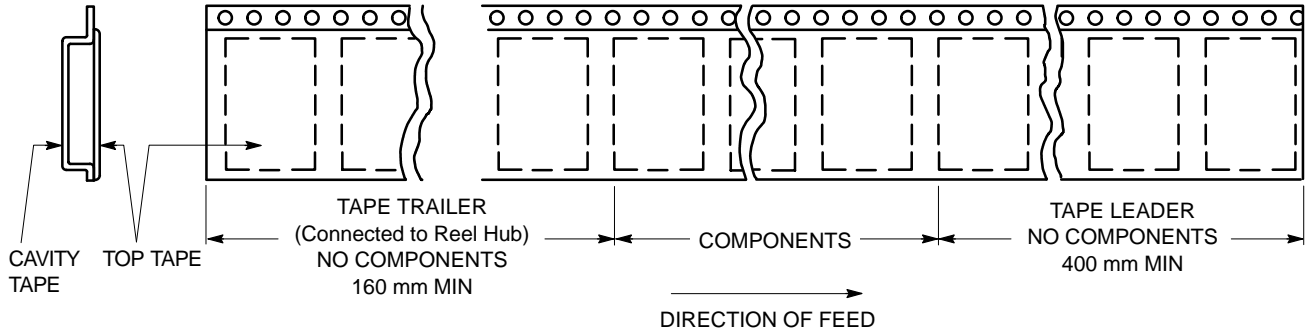


Figure 14. Tape Ends for Finished Goods

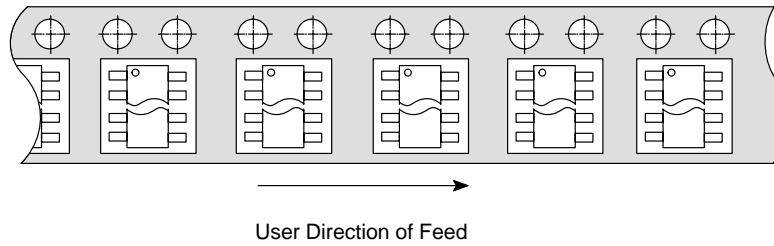


Figure 15. TSSOP and SOIC R2 Reel Configuration/Orientation

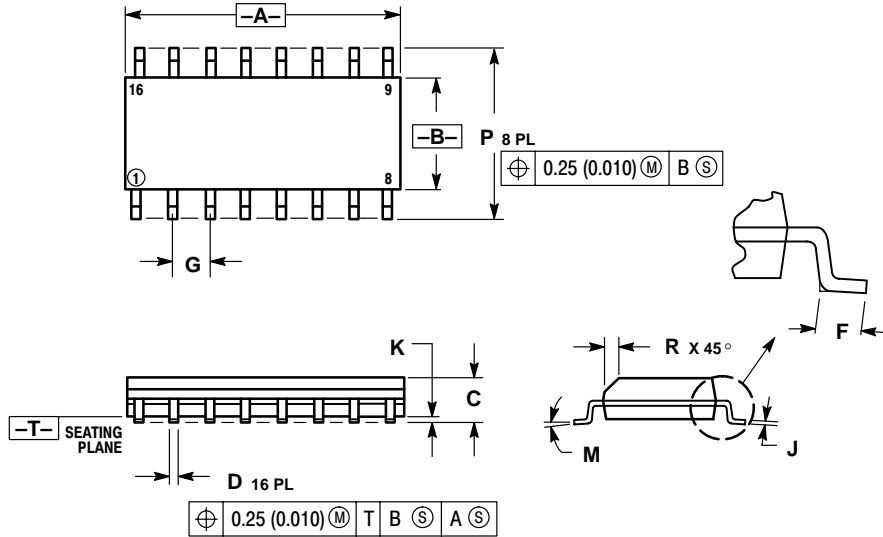
**TAPE UTILIZATION BY PACKAGE**

| Tape Size | SOIC                   | TSSOP            | QFN              | SC88A / SOT-353<br>SC88/SOT-363 |
|-----------|------------------------|------------------|------------------|---------------------------------|
| 8 mm      |                        |                  |                  | 5-, 6-Lead                      |
| 12 mm     | 8-Lead                 | 8-, 14-, 16-Lead | 8-, 14-, 16-Lead |                                 |
| 16 mm     | 14-, 16-Lead           | 20-, 24-Lead     | 20-, 24-Lead     |                                 |
| 24 mm     | 18-, 20-, 24-, 28-Lead | 48-, 56-Lead     | 48-, 56-Lead     |                                 |

# MC74LVX259

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J

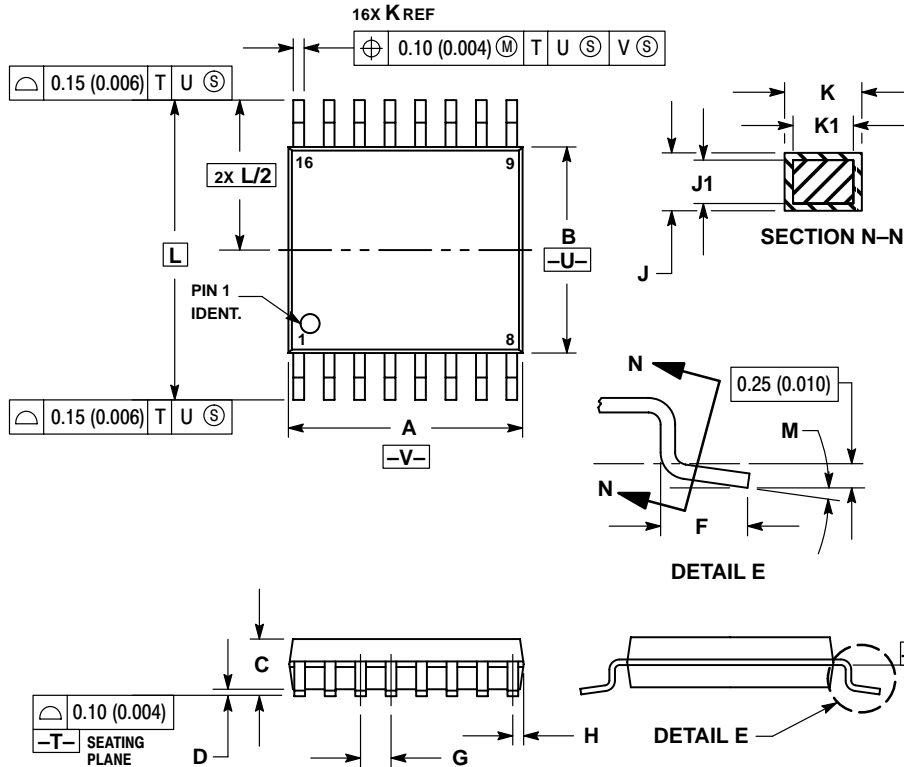


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE O



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |