Multi-layer ceramic chip capacitors

MCH55 (5750 (2220) size, chip capacitor)

●Features

1) High capacitance
2) Achieved high capacitance by thin and multi layer technology
3) Lead-free plating terminal
4) No polarity

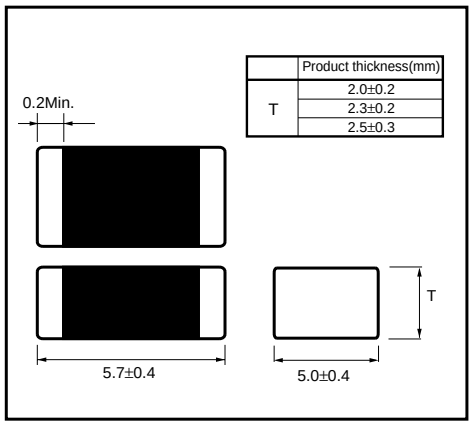
●Quick Reference

The design and specifications are subject to change without prior notice. Please check the most recent technical specifications prior to placing orders or using the product. For more detail information regarding packaging style code, please check product designation.

●High dielectric constant

Part No.	Size code	Temperature characteristics code		Operating temp. range (°C)	Rated voltage (V)	Capacitance (pF)	Capacitance tolerance	Thickness (mm)
MCH55	5750 (2220)	CN	±10% (B)	−25 to +85	50	4,700,000 (E6 Series)	K(±10%)	2.0 ± 0.2
						6,800,000 (E6 Series)		2.5 ± 0.3
					25	10,000,000 (E6 Series)		2.0 ± 0.2
						15,000,000 (E6 Series)		2.3 ± 0.2
					16	22,000,000 (E6 Series)		2.5 ± 0.3
			±15% (R) (X7R)	−55 to +125	50	4,700,000 (E6 Series)		2.0 ± 0.2
						6,800,000 (E6 Series)		2.5 ± 0.3
					25	10,000,000 (E6 Series)		2.0 ± 0.2
						15,000,000 (E6 Series)		2.3 ± 0.2
					16	22,000,000 (E6 Series)		2.5 ± 0.3
			±15% (X5R)	−55 to +85	16	33,000,000 (E6 Series)	M(±20%)	2.0 ± 0.2
						47,000,000 (E6 Series)		2.3 ± 0.2
					6.3	68,000,000 (E6 Series)		
		FN	+30% , −80% (F)	−25 to +85	50	22,000,000 (E3 Series)	Z(+80% , −20%)	2.0 ± 0.2
					25	47,000,000 (E3 Series)		
					16	100,000,000 (E3 Series)		2.5 ± 0.3
			+22% , −82% (Y5V)	−30 to +85	50	22,000,000 (E3 Series)		2.0 ± 0.3
					25	47,000,000 (E3 Series)		
					16	100,000,000 (E3 Series)		2.5 ± 0.3

●External dimensions (Unit : mm)



●Product designation

Code	Product thickness	Packing specification	Reel	Basic ordering unit (pcs.)
P	**2.0mm**	Plustic tape (width 8mm, pitch 4mm)	ϕ180mm (7in.)	500
P	**2.3mm**	Plustic tape (width 8mm, pitch 4mm)	ϕ180mm (7in.)	500
P	**2.5mm**	Plustic tape (width 8mm, pitch 4mm)	ϕ180mm (7in.)	500

Reel (ϕ180mm) : compatible with EIAJ ET-7200A

Part No. Packing Style

M C H 5 5 3 F N 1 0 7 Z P

Rated voltage

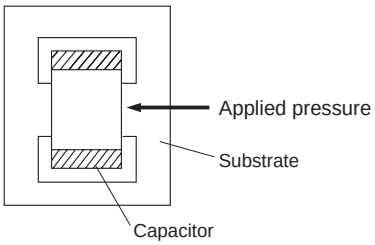
Code	Voltage
8	6.3V
4	10V
3	16V
2	25V
5	50V

Temperature characteristic code
: Refer to quick reference table.

Nominal capacitance	Capacitance tolerance	
	Code	Tolerance
3-digit designation according to IEC	**K**	±10%
	M	±20%
	Z	+80%, –20%

●Performance and test method

No.	Items	Performance	Test Method (As per JIS C 5101-1, JIS C 5101-10)
1	Appearance and dimensions	No marked defects shall be allowed for appearance. Dimensions shall be as specified the clause 4.	As per 4.4 of JIS C 5101-1. As per 4.5 of JIS C 5101-10 Using a Magnifier.
2	Withstanding voltage	No dielectrical breakdown or other damage shall be allowed.	As per 4.6 of JIS C 5101-1. As per 4.6.4 of JIS C 5101-10 Voltage shall be applied as per Table1. Table 1 Charac-teristic: Voltage CN, FN: 250% Rated voltage Voltage shall be applied for 1 to 5s with 50mA charging and discharging current.
3	Insulation resistance	Not less than 10000MΩ or 100MΩ・μF, whichever is less.	As per 4.5 of JIS C 5101-1. As per 4.6.3 of JIS C 5101-10 Measurements shall be made after 60+/–5s period of the rated voltage applied.
4	Capacitance	Capacitance shall be within specified tolerance range.	As per 4.7 of JIS C 5101-1. As per 4.6.1 of JIS C 5101-10 Measurements shall be made under the conditions specified in Table 2. Table 2 Charac-teristic: Frequency・Voltage CN: ≤ 10μF: 1+/–0.1kHz 1+/–0.2Vrms.; > 10μF: 120+/–24Hz 0.5+/–0.2Vrms. FN: 1+/–0.1kHz 1+/–0.2Vrms.; 120+/–24Hz 0.5+/–0.2Vrms.
5	Dielectric loss tangent	C N: tan δ ≤ 7.5% F N: Rated voltage=16V tan δ ≤ 10.0%	As per 4.8 of JIS C 5101-1. As per 4.6.2 of JIS C 5101-10 Measurements shall be made under the conditions specified in Table 2.

<table>
<tr><th>No.</th><th colspan="2">Items</th><th colspan="3">Performance</th><th>Test Method
(As per JIS C 5101-1, JIS C 5101-10)</th></tr>
<tr><td>6</td><td colspan="2">Temperature characteristic</td><td>C N</td><td>B</td><td>+/–10%
(–25°C to +85°C)</td><td rowspan="3">As per 4.24 of JIS C 5101-1.
As per 4.7 of JIS C 5101-10
If required, measurements shall be made at a given temperature.</td></tr>
<tr><td></td><td></td><td>X5R</td><td>+/–15%
(–55°C to +85°C)</td></tr>
<tr><td></td><td></td><td>F N</td><td colspan="2">+30%, –80%
(–25°C to +85°C)
+22%, –82%
(–30°C to +85°C)</td></tr>
<tr><td>7</td><td colspan="2">Solderability</td><td colspan="3">More than 3/4 of each end termination shall be covered with new solder.</td><td>As per 4.15.2 of JIS C 5101-1.
As per 4.11 of JIS C 5101-10
The solder specified in JIS Z 3282 H63A shall be used. Ans the flux containing 25% rosin and ethanol solution shall be used.
The specimens shall be immersed into the solder at 235+/–5°C for 2+/–0.5s
So that both end terminations are completely under solder.</td></tr>
<tr><td rowspan="5">8</td><td rowspan="5">Resistance to soldering heat</td><td>Appearance</td><td colspan="3">Without mechanical damage.</td><td rowspan="5">As per 4.14 of JIS C 5101-1.
As per 4.10 of JIS C 5101-10
The solder specified in JIS Z 3282. H63A shall be used.
The specimens shall be immersed into the solder at 260+/–5°C for 5+/–0.5s so that both end terminations are completely under the solder.
Pre-heating at 150+/–10°C for 1 to 2min
Initial measurements prior to test shall be performed after the thermal
Pre-conditioning specified in Remarks (1).
Final measurements shall be made after the specimens have been left at room temperature as per Table3.
Table3
<table><tr><th>Charac-teristic</th><th>Time</th></tr><tr><td>CN, FN</td><td>48+/–4 h</td></tr></table></td></tr>
<tr><td>Change rate from initial value</td><td>C N</td><td>Within +/–7.5%</td></tr>
<tr><td></td><td>F N</td><td>Within +/–20%</td></tr>
<tr><td>Dielectric loss tangent</td><td colspan="2">Within specified initial value.</td></tr>
<tr><td>Insulation resistance</td><td colspan="2">Within specified initial value.</td></tr>
<tr><td>Withstanding voltage</td><td colspan="2">No defects shall be allowed.</td></tr>
<tr><td>9</td><td colspan="2">End termination adherence</td><td colspan="3">Without peeling or sign of peeling shall be allowed on the end terminations.</td><td>As per 4.13 of JIS C 5101-1.
As per 4.8 ofJIS C 5101-10
A 5N weight for 10+/–1s shall be applied to the soldered specimens as shown by the arrow mark in the below sketch.
 
</td></tr>
</table>

<table>
<tr><th>No.</th><th colspan="2">Items</th><th colspan="2">Performance</th><th>Test Method
(As per JIS C 5101-1, JIS C 5101-10)</th></tr>
<tr><td>10</td><td>Bending strength</td><td>Appearance</td><td colspan="2">Without mechanical damage.</td><td>As per 4.35 of JIS C 5101-1.
As per 4.9 of JIS C 5101-10
Glass epoxy board with soldered specimens shall be bent till 1mm by 1.0mm/s.</td></tr>
<tr><td rowspan="4">11</td><td rowspan="4">Vibration</td><td>Appearance</td><td colspan="2">Without mechanical damage.</td><td rowspan="4">As per 4.17 of JIS C 5101-1.
The specimens shall be soldered on the specified test jig.
Initial measurements shall be made after the thermal pre-conditioning specified in Remarks(1).
Final measurements shall be made after the specimens have been left at room temperature as per Table3.
[Condition]
Directions : 2h each X, Y and Z directions
Total : 6h
Frequency range : 10 to 55 to 10Hz(1min)
Applitude : 1.5mm
(shall not exceed acceleration196m/s^2)
Table3<table><tr><th>Charac-teristic</th><th>Time</th></tr><tr><td>CN, FN</td><td>48+/–4 h</td></tr></table></td></tr>
<tr><td rowspan="2">Change rate from initial value</td><td>C N</td><td>Within +/–7.5%</td></tr>
<tr><td>F N</td><td>Within +/–20%</td></tr>
<tr><td>Dielectric loss tangent</td><td colspan="2">Within specified initial value.</td></tr>
<tr><td rowspan="6">12</td><td rowspan="6">Temperature cycling</td><td>Appearance</td><td colspan="2">Without mechanical damage.</td><td rowspan="6">As per 4.16 of JIS C 5101-1
As per 4.12 of JIS C 5101-10
The specimens shall be soldered on the test jig shown in Remarks.
Temperature cycle : 100cycles Initial measurements prior to test shall be performed after the thermal per-conditioning specified in Remarks (1).
Final measurements shall be made after the specimens have been left at room temperature as per Table3.
Test condition<table><tr><th>Step</th><th>Temp. (°C)</th><th>Time (min)</th></tr><tr><td>1</td><td>Min operating temp.</td><td>30+/–3</td></tr><tr><td>2</td><td>Room temp.</td><td>≤ 3</td></tr><tr><td>3</td><td>Max operating temp.</td><td>30+/–3</td></tr><tr><td>4</td><td>Room temp.</td><td>≤ 3</td></tr></table>Table3<table><tr><th>Charac-teristic</th><th>Time</th></tr><tr><td>CN, FN</td><td>48+/–4 h</td></tr></table></td></tr>
<tr><td rowspan="2">Change rate from initial value</td><td>C N</td><td>Within +/–7.5%</td></tr>
<tr><td>F N</td><td>Within +/–20%</td></tr>
<tr><td>Dielectric loss tangent</td><td colspan="2">Within specified initial value.</td></tr>
<tr><td>Insulation resistance</td><td colspan="2">Within specified initial value.</td></tr>
<tr><td>Withstanding voltage</td><td colspan="2">No defects shall be allowed.</td></tr>
</table>

<table>
<tr><th>No.</th><th colspan="2">Items</th><th colspan="2">Performance</th><th>Test Method
(As per JIS C 5101-1, JIS C 5101-10)</th></tr>
<tr><td rowspan="6">13</td><td rowspan="6">Humidity
(Steady)</td><td>Appearance</td><td colspan="2">Without mechanical damage.</td><td rowspan="6">As per 4.22 of JIS C 5101-1
As per JIS C 5101-10
Test temperature : 60+/–2°C
Relative humidity : 90 to 95%
Test time : 500 +24/–0 h
Initial measurements prior to test shall be made after the voltage pre-conditioning specified in Remarks (2).
Final measurements have been left at room temperature as per Table3.

Table3
<table><tr><th>Charac-teristic</th><th>Time</th></tr><tr><td>CN, FN</td><td>48+/–4 h</td></tr></table></td></tr>
<tr><td rowspan="2">Change rate from initial value</td><td>C N</td><td>Within +/–12.5%</td></tr>
<tr><td>F N</td><td>Within +/–30%</td></tr>
<tr><td rowspan="2">Dielectric tangent</td><td>C N</td><td>Less than 200% of initial spec.</td></tr>
<tr><td>F N</td><td>Less than 150% of initial spec.</td></tr>
<tr><td>Insulation resistance</td><td colspan="2">Not less than 1000MΩ or 10MΩ・μF, whichever is less.</td></tr>
<tr><td rowspan="6">14</td><td rowspan="6">Humidity life test</td><td>Appearance</td><td colspan="2">Without mechanical damage.</td><td rowspan="6">As per 4.22 of JIS C 5101-1
As per 4.14 of JIS C 5101-10
Test temperature : 60+/–2°C
Relative humidity : 90 to 95%
Voltage : Rated voltage
Test time : 500 +24/–0 h
Initial measurements prior to test shall be made after the voltage pre-conditioning specified in Remarks (2).
Final measurements shall be made after the specimens have been left at room temperature as per Table3.

Table3
<table><tr><th>Charac-teristic</th><th>Time</th></tr><tr><td>CN, FN</td><td>48+/–4 h</td></tr></table></td></tr>
<tr><td rowspan="2">Change rate from initial value</td><td>C N</td><td>Within +/–12.5%</td></tr>
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<tr><td>Insulation resistance</td><td colspan="2">Not less than 500MΩ or 5MΩ・μF, whichever is less.</td></tr>
</table>

<table>
<tr><th>No.</th><th colspan="2">Items</th><th colspan="2">Performance</th><th>Test Method
(As per JIS C 5101-1, JIS C 5101-10)</th></tr>
<tr><td rowspan="5">15</td><td rowspan="5">Heat life test</td><td>Appearance</td><td colspan="2">Without mechanical damage.</td><td rowspan="5">As per 4.23 of JIS C 5101-1.
As per 4.15 of JIS C 5101-10
<table><tr><th></th><th>Test temperature(°C)</th><th>Voltage</th><th>Test time (h)</th></tr><tr><td>CN</td><td>85
(B・X5R)</td><td>200%
Rated voltage</td><td>1000
+48/–0</td></tr><tr><td>FN</td><td>85</td><td>200%
Rated voltage</td><td>1000
+48/–0</td></tr></table>Initial measurements prior to test shall be made after the voltage pre-conditioning specified in Remarks (2).
Final measurements shall be made after the specimens have been left at room temperature
Table3<table><tr><th>Charac-teristic</th><th>Time</th></tr><tr><td>CN, FN</td><td>48+/–4 h</td></tr></table></td></tr>
<tr><td rowspan="2">Change rate from initial value</td><td>C N</td><td>Within +/–15%</td></tr>
<tr><td>F N</td><td>Within +/–30%</td></tr>
<tr><td rowspan="2">Dielectric loss tangent</td><td>C N</td><td>Less than 200% of initial spec.</td></tr>
<tr><td>F N</td><td>Less than 150% of initial spec.</td></tr>
<tr><td>Insulation resistance</td><td colspan="2">Not less than 1000MΩ or 10MΩ・μF, whichever is less.</td></tr>
</table>

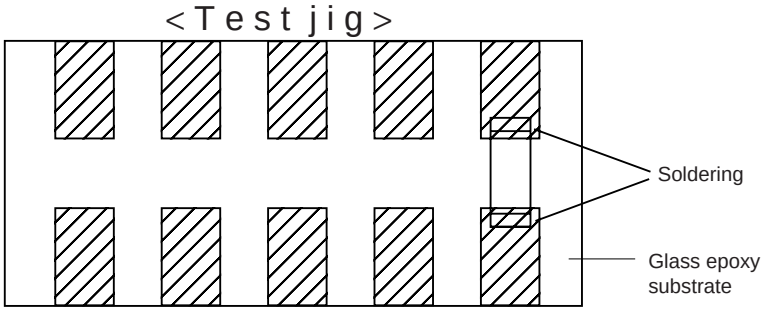
[Remarks]

Pre-conditioning

If specified in test method of as per 3(Performance and test method), capacitors of CN, FN characteristics shall be pre-conditionded as follows.

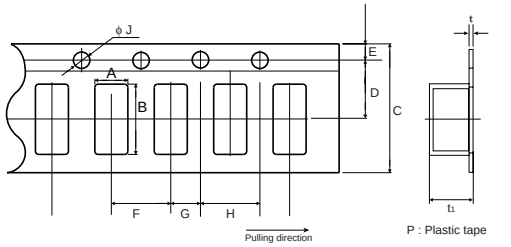
(1) Thermal pre-conditioning
Prior to initial measurements, specimens shall be conditioned at a temperature of 150 0/–10°C for a period of 1hr., and shall be allowed to stabilize at room temperature for 48+/–4h

(2) Voltage pre-conditioning
Prior to initial measurements, voltage specified as a test condition shall be applied to specimens for a period of 1hr., and the specimens shall be allowed to stabilize at room temperature for 48+/–4h



●Packaging specifications

Taping dimensions



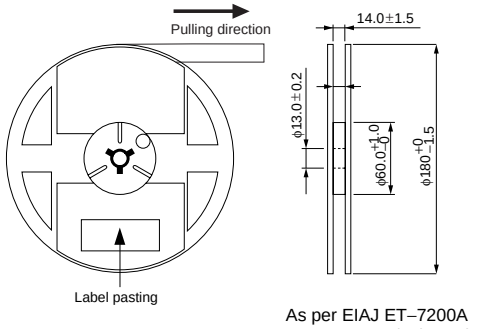
Symbol	C	D	E	F	G	H	J	t	t1
								Plastic	
Dimensions	12.0 +/ −0.3	5.5 +/ −0.05	1.75 +/ −0.1	8.0 +/ −0.1	2.0 +/ −0.05	4.0 +/ −0.1	ϕ1.5 +0.1/ −0	0.6 MAX.	6.5 MAX.

(Unit : mm)

Style \ Symbol	A	B
MCH55	5.4	6.1

(Unit : mm)

Reel dimensions



As per EIAJ ET−7200A

(Unit : mm)

(1) The quantity for one reel is as bellows.

Kind of reel	Series	Plastic tape	
		Quantity	Symbol
ϕ180 reel	MCH55	500 pcs.	P

(2) When the tape is pulled out towards the operator with the cover tape facing upward, the feeding holes shall be found on the right portion of the tape.
(3) Specification of beginning and ending of the tape are as follows.

Ending(reel's center) : Approx. Over 160mm (no chips)
Beginning(reel's round) : Approx. Over 160mm (no chips)
: Approx. 240mm (cover tape only)

(4) No juncture of tape shall be allowed.
(5) The share strength of tape shall be more than 5N at the break down strength.
(6) The peel strength of the cover tape shall be 0.1 to 0.7(N) when the cover tape are peeled 0 to 15° degree from the surface.
(7) The number of missing components shall not exceed 0.1% of the total number of components (marked number) or one whichever is the larger, and no consecutive missing exceeding two is allowed.
(8) The reels made from resin shall be used, as per EIAJ ET-7200A.

●Marking

No marking shall be performed on the chip.

Trademark, parts number, quantity, lot No. , and country of origin shall be labeled on each reel.

●Numbering system for LOT No.

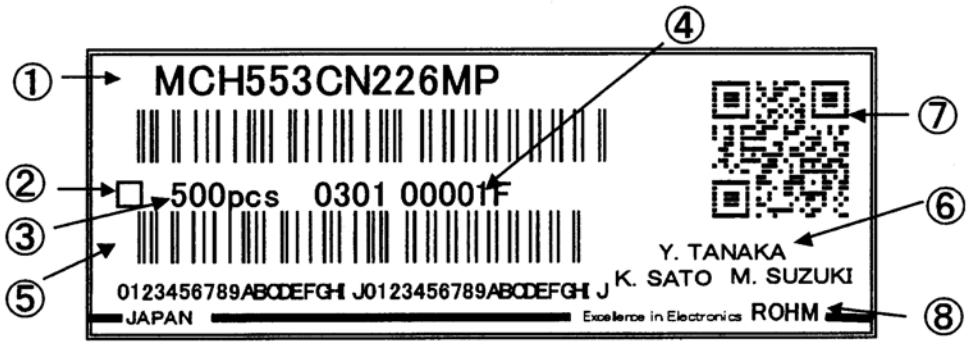
Example 03 (1) 01 (2) A0001 (3) F (4)

(1) The end of the Christian Era < two digits> of production finish.
(2) Week in completing part of production finish.
(3) Manufacture continuity number.
(4) The symbol of manufacturing plant.

●**Label expression**

The Figure below is label expression

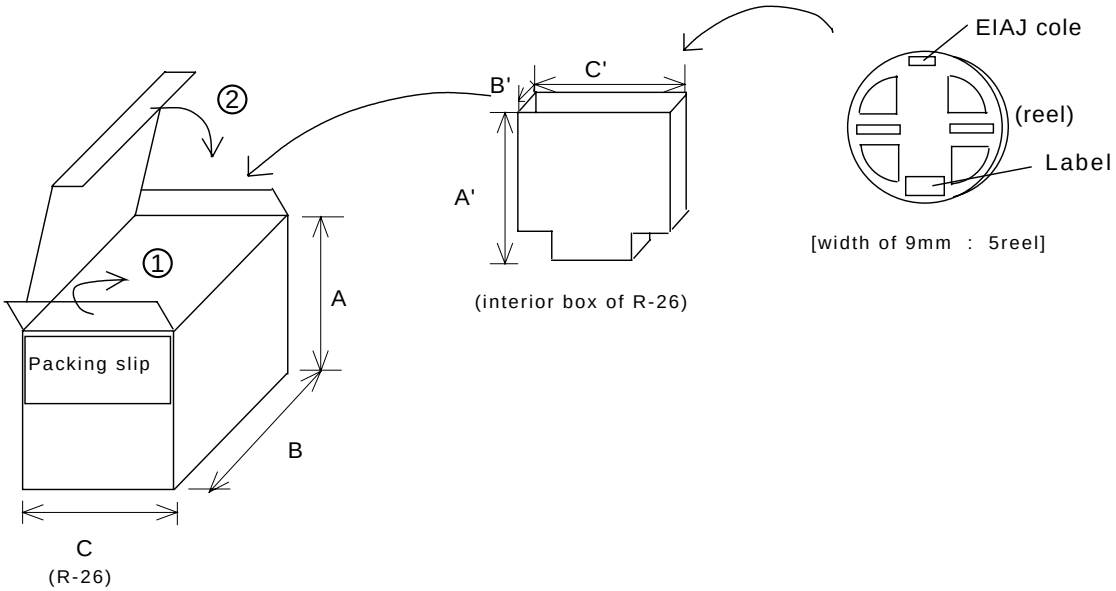
< Label Example > Part Number : MCH553CN226MP



① Part Number
② Division cord
③ Quantity
④ Lot No.
⑤ The Country of origin
⑥ Inspector
⑦ QR code
⑧ Trademark

●**Packing method**

1) ϕ180mm Reel



< Packaging unit >

Symbol	K
Quantity of reel in interior box	3
Quantity of reel in box of R-26	12

Dimensions	Packaging	
	R-26	interior box of R-26
A (A')	195	185
B (B')	255	60
C (C')	190	185

(Unit : mm)

< Appearance >

Carton

< Accumulation >

You must do accumulation by ten boxes

< Packaging slip >

1. Customer
2. Parts number
3. Quantity
4. Box quantity
5. Trade mark

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