MCM6323A

Product Preview

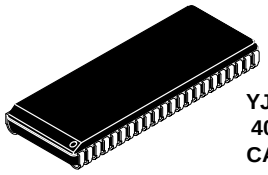
64K x 16 Bit 3.3 V Asynchronous Fast Static RAM

The MCM6323A is a 1,048,576 bit static random access memory organized as 65,536 words of 16 bits. Static design eliminates the need for external clocks or timing strobes; CMOS circuitry reduces power consumption and provides for greater reliability.

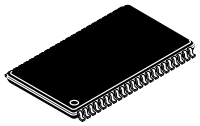
The MCM6323A is equipped with chip enable ($\overline{E}$), write enable ($\overline{W}$), and output enable ($\overline{G}$) pins, allowing for greater system flexibility and eliminating bus contention problems. Separate byte enable controls ($\overline{LB}$ and $\overline{UB}$) allow individual bytes to be written and read. $\overline{LB}$ controls the 8 DQa bits, while $\overline{UB}$ controls the 8 DQb bits.

The MCM6323A is available in a 400 mil small–outline J–leaded (SOJ) package and a 44–lead TSOP Type II package in copper leadframe for optimum printed circuit board (PCB) reliability.

- Single 3.3 V ± 0.3 V Power Supply
- Fast Access Time: 10, 12, 15 ns
- Equal Address and Chip Enable Access Time
- All Inputs and Outputs are TTL Compatible
- Data Byte Control
- Fully Static Operation
- Power Operation: 140/135/130 mA Maximum, Active AC
- Industrial Temperature Option: – 40 to + 85°C
  Part Number: SCM6323AYJ10A

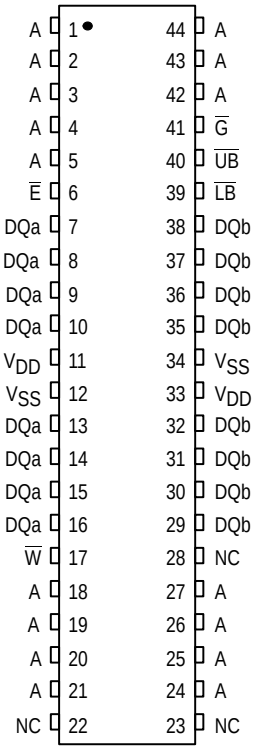


YJ PACKAGE
400 MIL SOJ
CASE 919–01



TS PACKAGE
44–LEAD
TSOP TYPE II
CASE 924A–01

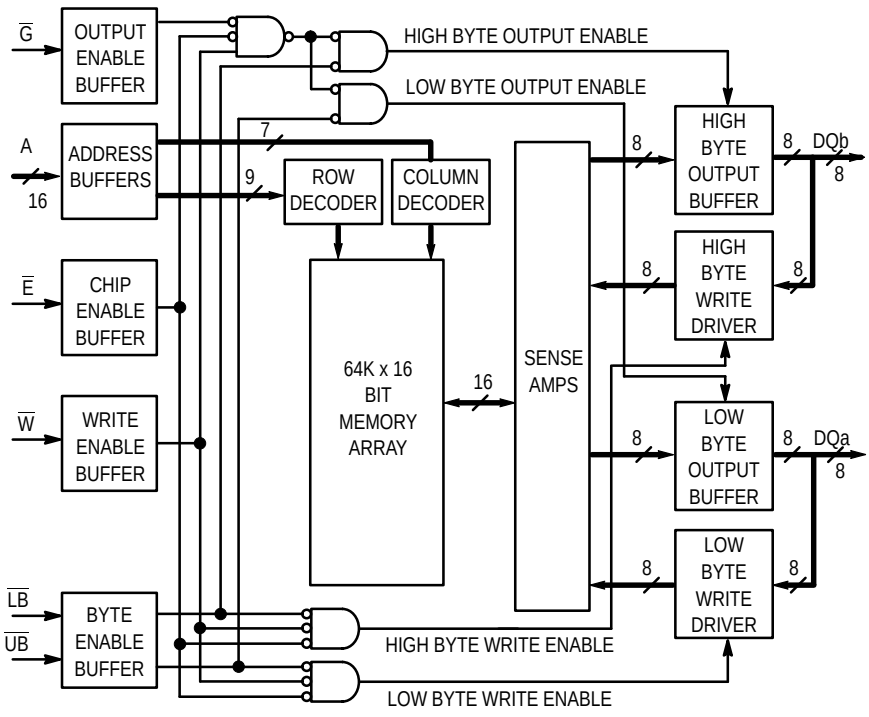
PIN ASSIGNMENT



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{UB}$	Upper Byte
$\overline{LB}$	Lower Byte
DQa	Lower Data Input/Output
DQb	Upper Data Input/Output
V_{DD}	+ 3.3 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



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MOTOROLA

TRUTH TABLE (X = Don't Care)

$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{LB}$	$\overline{UB}$	Mode	V_{DD} Current	DQa's	DQb's
H	X	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	High–Z
L	H	H	X	X	Output Disabled	I_{DDA}	High–Z	High–Z
L	X	X	H	H	Output Disabled	I_{DDA}	High–Z	High–Z
L	L	H	L	H	Low Byte Read	I_{DDA}	D_{out}	High–Z
L	L	H	H	L	High Byte Read	I_{DDA}	High–Z	D_{out}
L	L	H	L	L	Word Read	I_{DDA}	D_{out}	D_{out}
L	X	L	L	H	Low Byte Write	I_{DDA}	D_{in}	High–Z
L	X	L	H	L	High Byte Write	I_{DDA}	High–Z	D_{in}
L	X	L	L	L	Word Write	I_{DDA}	D_{in}	D_{in}

ABSOLUTE MAXIMUM RATINGS (See Notes)

Rating		Symbol	Value	Unit
Supply Voltage		V_{DD}	– 0.5 to + 4.6	V
Voltage on Any Pin		V_{in}	– 0.5 to V_{DD} + 0.5	V
Output Current per Pin		I_{out}	± 20	mA
Package Power Dissipation		P_D	.75	W
Temperature Under Bias	Commerial Industrial	T_{bias}	– 10 to + 85 – 45 to + 90	°C
Operating Temperature	Commerial Industrial	T_A	0 to + 70 – 40 to + 85	°C
Storage Temperature		T_{stg}	– 55 to + 150	°C

NOTES:
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. All voltages are referenced to V_{SS}.
3. Power dissipation capability will be dependent upon package characteristics and use environment.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

This CMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.2	—	V_{DD} + 0.3**	V
Input Low Voltage	V_{IL}	– 0.5*	—	0.8	V

* V_{IL} (min) = – 0.5 V dc; V_{IL} (min) = – 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.
** V_{IH} (max) = V_{DD} + 0.3 V dc; V_{IH} (max) = V_{DD} + 2.0 V ac (pulse width ≤ 20 ns) for I ≤ 20.0 mA.

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{DD})		$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{DD})		$I_{lkg(O)}$	—	± 1.0	µA
Output Low Voltage	(I_{OL} = + 4.0 mA) (I_{OL} = + 100 µA)	V_{OL}	—	0.4 V_{SS} + 0.2	V
Output High Voltage	(I_{OH} = – 4.0 mA) (I_{OH} = – 100 µA)	V_{OH}	2.4 V_{DD} – 0.2	—	V

POWER SUPPLY CURRENTS (See Note 1)

Parameter		Symbol	6323A–10	6323A–12	6323A–15	Unit	Notes
AC Active Supply Current (I_{out} = 0 mA) (V_{DD} = max, f = f_{max})	Commerical Industrial	I_{DDA}	140 150	135 140	130 135	mA	2
AC Standby Current ($\overline{E}$ = V_{IH}, V_{DD} = max, f = f_{max})	Commerical Industrial	I_{SB1}	40 45	35 40	30 35	mA	2
CMOS Standby Current (V_{DD} = max, f = 0 MHz, $\overline{E}$ ≥ V_{DD} – 0.2 V, V_{in} ≤ V_{SS} + 0.2 V, or ≥ V_{DD} – 0.2 V)	Commerical Industrial	I_{SB2}	5 5	5 5	5 5	mA	

NOTES:
1. Typical current = 25°C @ 3.3 V.
2. Reference AC Operating Conditions and Characteristics for input and timing (V_{IH}/V_{IL}, t_r/t_f, pulse level 0 to 3.0 V, V_{IH} = 3.0 V, V_{IL} = 0 V).

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Address Input Capacitance	C_{in}	—	6	pF
Control Input Capacitance	C_{in}	—	6	pF
Input/Output Capacitance	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V ± 0.3 V, T_A = 0 to +70°C, Unless Otherwise Noted)
(T_A = – 40 to + 85°C for Industrial Temperature Offering)

Logic Input Timing Measurement Reference Level . . . . . 1.50 V
Logic Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 2 ns

Output Timing Reference Level . . . . . 1.50 V
Output Load . . . . . See Figure 1

READ CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	5
Address Access Time	t_{AVQV}	—	10	—	12	—	15	ns	
Enable Access Time	t_{ELQV}	—	10	—	12	—	15	ns	
Output Enable Access Time	t_{GLQV}	—	4	—	5	—	6	ns	6
Output Hold from Address Change	t_{AXQX}	3	—	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	3	—	3	—	3	—	ns	6, 7, 8
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	0	—	ns	6, 7, 8
Enable High to Output High–Z	t_{EHQZ}	—	4	—	5	—	6	ns	6, 7, 8
Output Enable High to Output High–Z	t_{GHQZ}	—	4	—	5	—	6	ns	6, 7, 8
Byte Enable Access Time	t_{BLQV}	—	4	—	5	—	6	ns	
Byte Enable Low to Output Active	t_{BLQX}	0	—	0	—	0	—	ns	6, 7, 8
Byte High to Output High–Z	t_{BHQZ}	0	5	0	5	0	5	ns	6, 7, 8

NOTES:
1. $\overline{W}$ is high for read cycle.
2. For common I/O applications, minimization, or elimination of bus contention conditions is necessary during read and write cycles.
3. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, and $\overline{LB}$ and/or $\overline{UB}$ = V_{IL}).
4. Addresses valid prior to or coincident with $\overline{E}$ going low.
5. All read cycle timings are referenced from the last valid address to the first transitioning address.
6. Transition is measured 200 mV from steady–state voltage.
7. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
8. This parameter is sampled and not 100% tested.

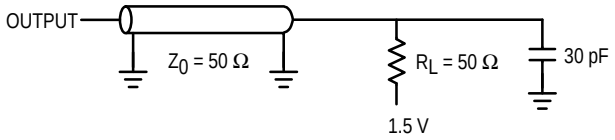


Figure 1. Equivalent AC Test Load

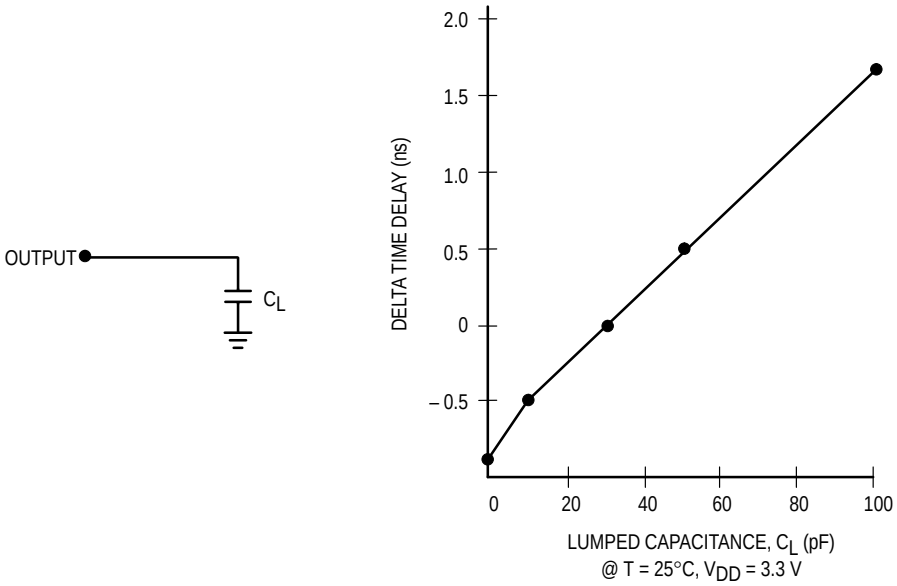


Figure 2. Lumped Capacitive Load and Typical Derating Curve

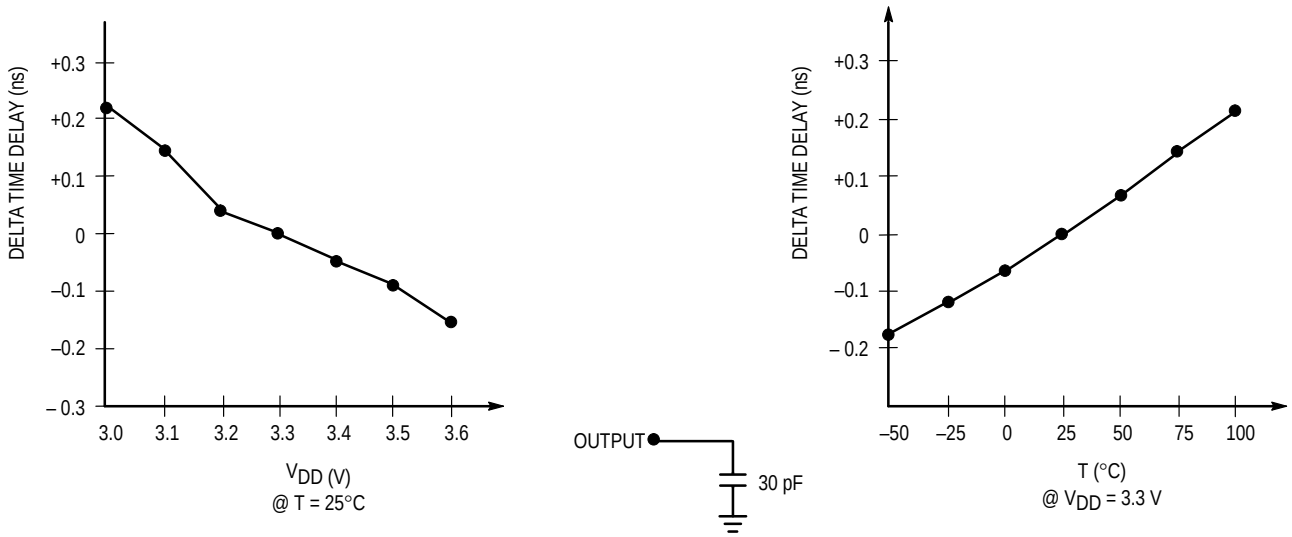
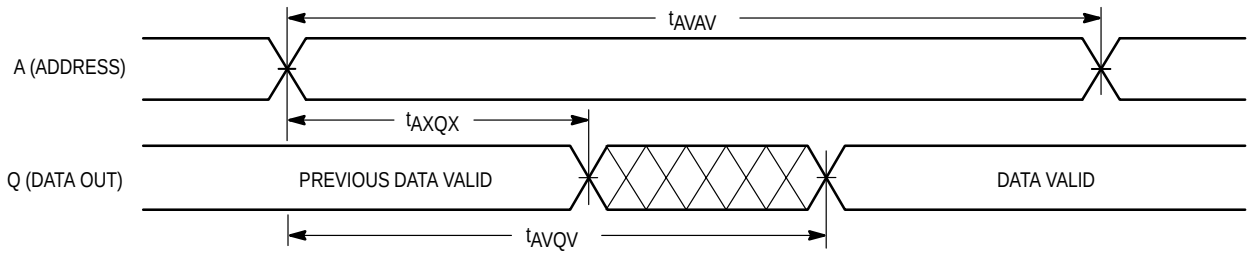
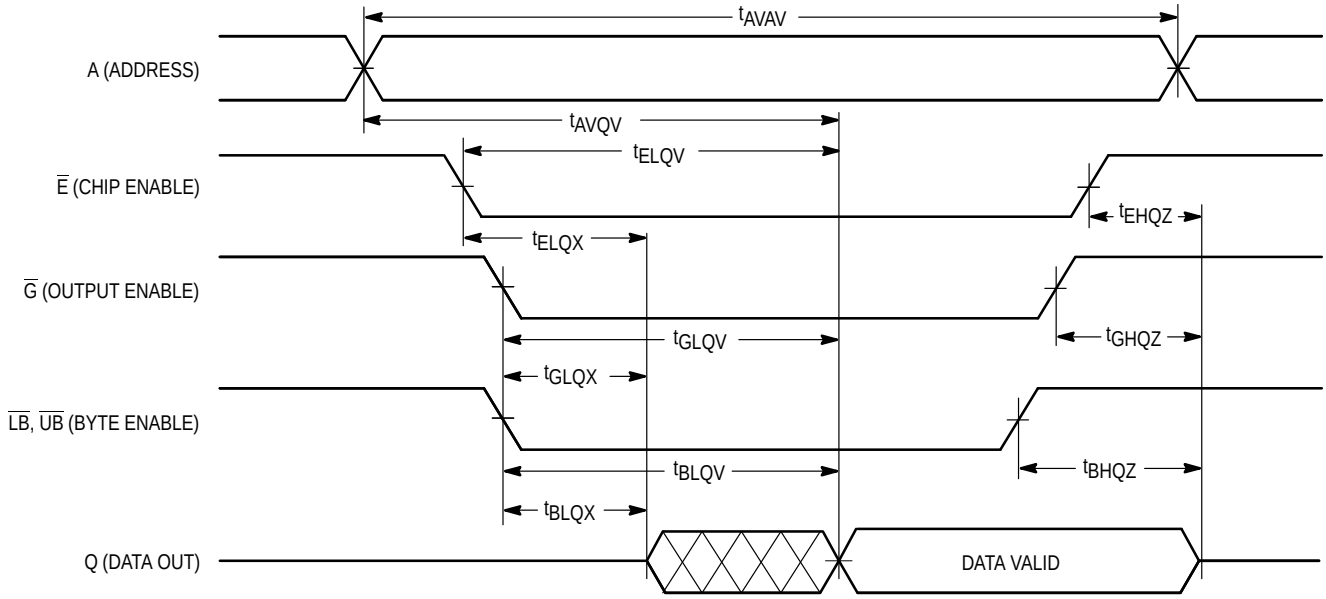


Figure 3. Derating Across Temperature and Voltage

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note 8)

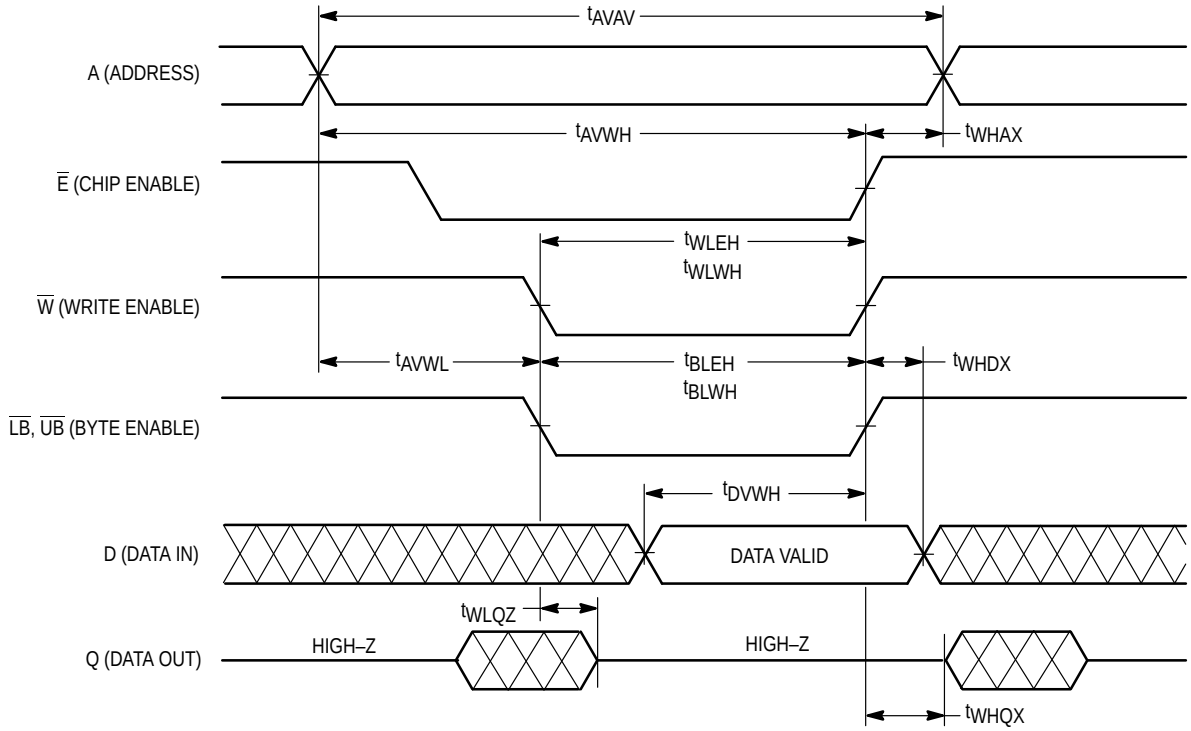


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVWL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Byte Pulse Width	t_{BLWH}, t_{BLEH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and $\overline{LB}$ and/or $\overline{UB}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.
6. This parameter is sampled and not 100% tested.

WRITE CYCLE 1
($\overline{W}$ Controlled)

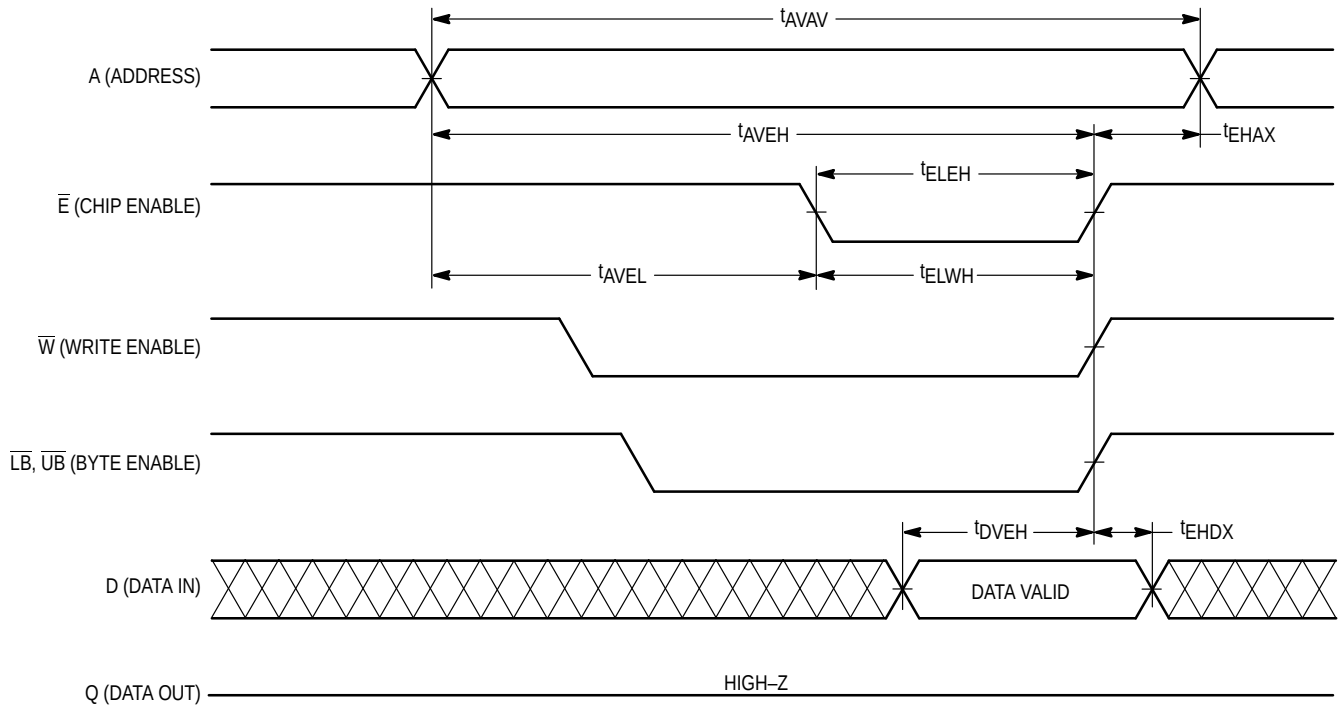


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVEL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	8	—	9	—	10	—	ns	
Enable to End of Write	t_{ELEH}, t_{ELWH}	8	—	9	—	10	—	ns	4, 5
Data Valid to End of Write	t_{DVEH}	4	—	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and $\overline{LB}$ and/or $\overline{UB}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2
($\overline{E}$ Controlled)

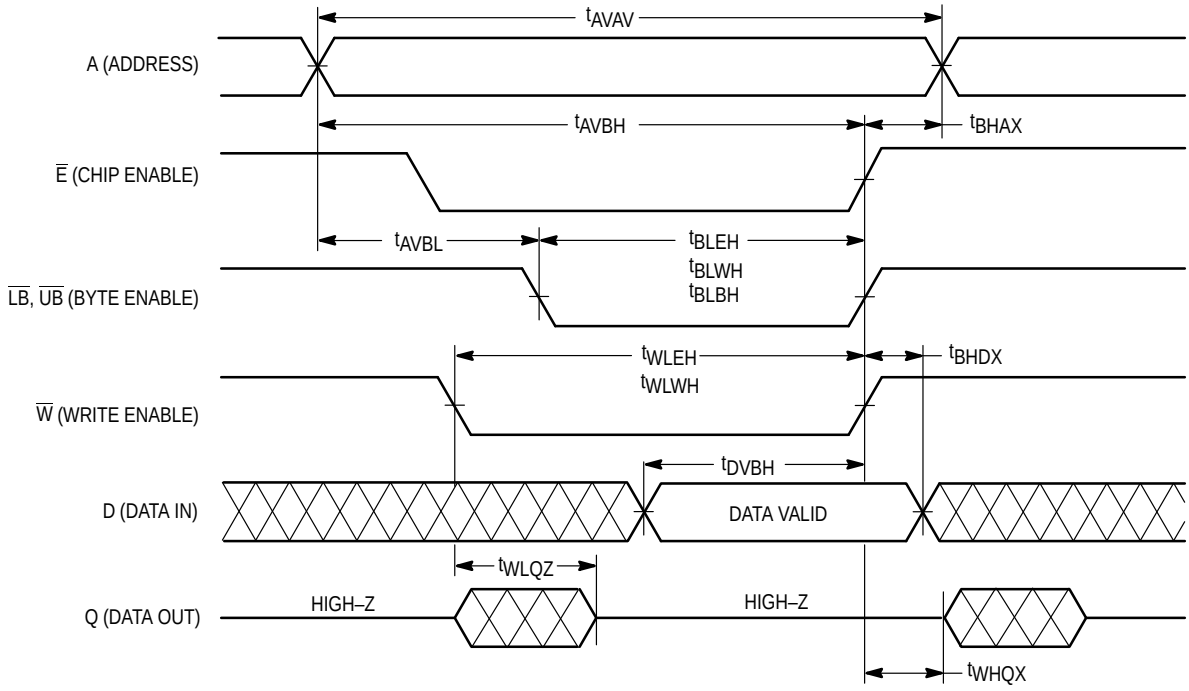


WRITE CYCLE 3 ($\overline{B}$ Controlled, See Notes 1 and 2)

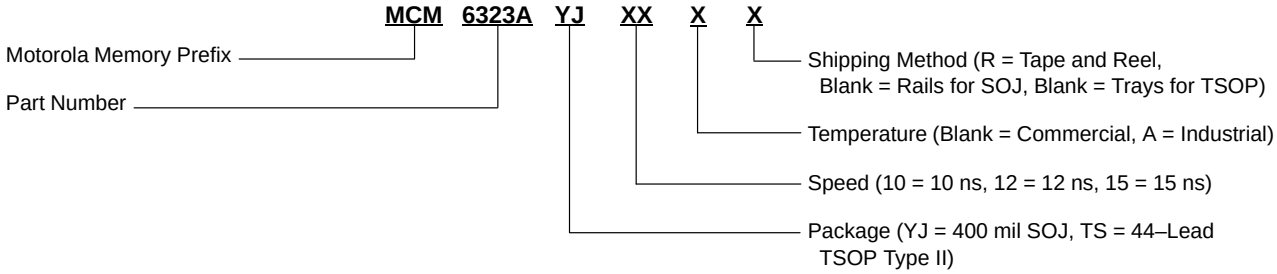
Parameter	Symbol	MCM6323A–10		MCM6323A–12		MCM6323A–15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	15	—	ns	3
Address Setup Time	t_{AVBL}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVBH}	8	—	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	8	—	9	—	10	—	ns	
Byte Pulse Width	t_{BLWH}, t_{BLEH}, t_{BLBH}	8	—	9	—	10	—	ns	
Data Valid to End of Write	t_{DVBH}	5	—	6	—	7	—	ns	
Data Hold Time	t_{BHDX}	0	—	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	4	0	5	0	6	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	3	—	3	—	3	—	ns	4, 5, 6
Write Recovery Time	t_{BHAX}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low, $\overline{W}$ low, and $\overline{LB}$ and/or $\overline{UB}$ low.
2. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycles.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured 200 mV from steady–state voltage.
5. At any given voltage and temperature, t_{WLQZ} max < t_{WHQX} min both for a given device and from device to device.
6. This parameter is sampled and not 100% tested.

WRITE CYCLE 3
($\overline{B}$ Controlled)



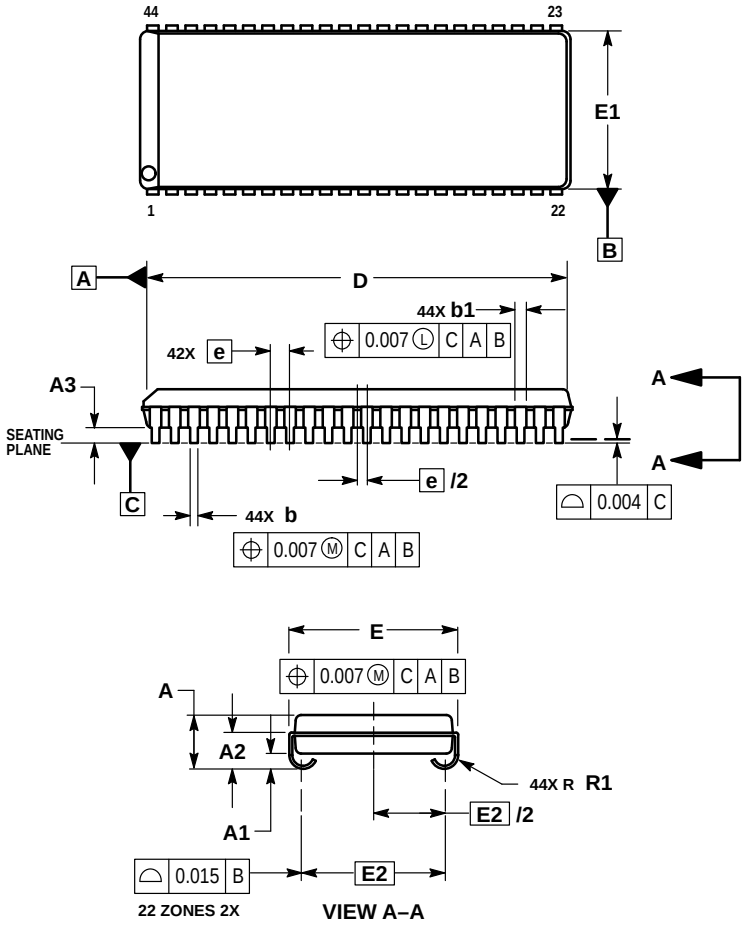
ORDERING INFORMATION
(Order by Full Part Number)



Full Commercial Part Numbers —	MCM6323AYJ10	MCM6323AYJ12	MCM6323AYJ15
	MCM6323AYJ10R	MCM6323AYJ12R	MCM6323AYJ15R
	MCM6323ATS10	MCM6323ATS12	MCM6323ATS15
	MCM6323ATS10R	MCM6323ATS12R	MCM6323ATS15R
Full Industrial Part Numbers —	SCM6323AYJ10A	SCM6323AYJ12A	SCM6323AYJ15A
	SCM6323AYJ10AR	SCM6323AYJ12AR	SCM6323AYJ15AR
	SCM6323ATS10A	SCM6323ATS12A	SCM6323ATS15A
	SCM6323ATS10AR	SCM6323ATS12AR	SCM6323ATS15AR

PACKAGE DIMENSIONS

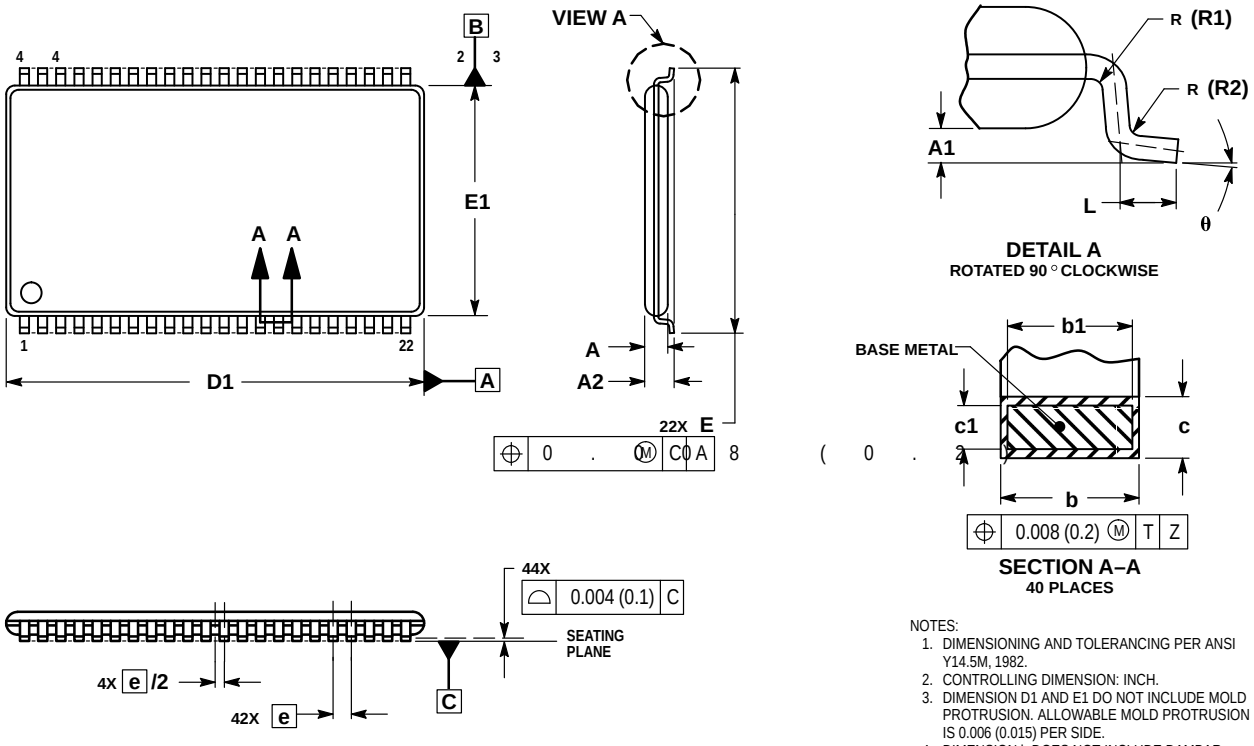
YJ PACKAGE
400 MIL SOJ
CASE 919–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS SHALL NOT EXCEED 0.006 PER END. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010 PER SIDE.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 AND, HENCE, DATUMS A AND B, ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b1 MAX BY MORE THAN 0.005. THE DAMBAR INTRUSION(S) SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001 BELOW b1 MIN.

	INCHES	
DIM	**MIN**	**MAX**
A	0.128	0.148
A1	0.025	—
A2	0.082	—
A3	0.035	0.045
b	0.015	0.020
b1	0.026	0.032
D	1.120	1.130
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
e	0.050 BSC	
R1	0.030	0.040

TS PACKAGE
44–LEAD
TSOP TYPE II
CASE 924A–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.006 (0.015) PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT ALLOW THE b DIMENSION TO EXCEED 0.023 (0.58).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	—	0.050	—	1.270
A1	0.002	0.006	0.051	0.152
A2	0.038	0.042	0.965	1.067
b	0.012	0.018	0.305	0.457
b1	0.012	0.016	0.305	0.406
c	0.005	0.008	0.127	0.203
c1	0.004	0.006	0.101	0.152
D1	0.721	0.729	18.313	18.517
e	0.0315 BSC		0.800 BSC	
E	0.456	0.470	11.582	11.938
E1	0.396	0.404	10.058	10.262
L	0.016	0.023	0.406	0.584
R1	0.004 REF		0.100 REF	
R2	0.004 REF		0.100 REF	
θ	0°	5°	0°	5°

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