

# OKI Semiconductor

**FEDD56V62160E-01**

Issue Date: Feb. 4, 2002

## MD56V62160E

**4-Bank × 1,048,576-Word × 16-Bit SYNCHRONOUS DYNAMIC RAM**

### DESCRIPTION

The MD56V62160E is a 4-Bank × 1,048,576-word × 16-bit Synchronous dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The device operates at 3.3 V. The inputs and outputs are LVTTL compatible.

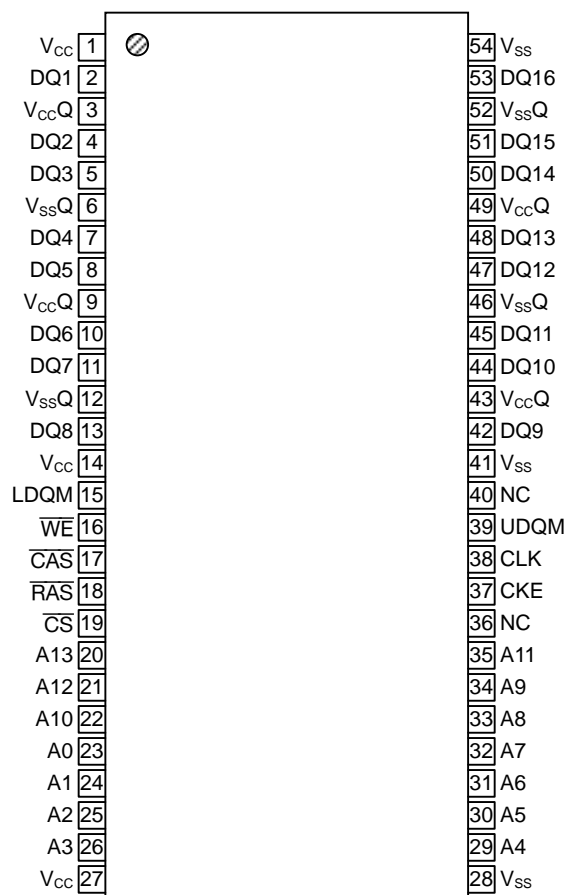
### FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4-Bank × 1,048,576-word × 16-bit configuration
- Single 3.3 V power supply, ±0.3 V tolerance
- Input : LVTTL compatible
- Output : LVTTL compatible
- Refresh : 4096 cycles/64 ms
- Programmable data transfer mode
  - CAS Latency (1, 2, 3)
  - Burst Length (1, 2, 4, 8, Full Page)
  - Data scramble (sequential, interleave)
- CBR auto-refresh, Self-refresh capability
- Packages:
  - 54-pin 400 mil plastic TSOP (TypeII) (TSOP(2)54-P-400-0.80-K)(Product: MD56V62160E-xxTA)  
xx indicates speed rank.

### PRODUCT FAMILY

Family	Max. Frequency	Access Time (Max.)	
		t <sub>AC2</sub>	t <sub>AC3</sub>
MD56V62160E-7	143 MHz	6 ns	6 ns
MD56V62160E-10	100 MHz	6 ns	6 ns

**PIN CONFIGURATION (TOP VIEW)**



54-Pin Plastic TSOP(II)  
(K Type)

Pin Name	Function	Pin Name	Function
CLK	System Clock	UDQM, LDQM	Data Input/ Output Mask
CS	Chip Select	DQi	Data Input/ Output
CKE	Clock Enable	V <sub>CC</sub>	Power Supply (3.3 V)
A0–A10	Address	V <sub>SS</sub>	Ground (0 V)
A11	Bank Select Address	V <sub>CC</sub> Q	Data Output Power Supply (3.3 V)
RAS	Row Address Strobe	V <sub>SS</sub> Q	Data Output Ground (0 V)
CAS	Column Address Strobe	NC	No Connection
WE	Write Enable		

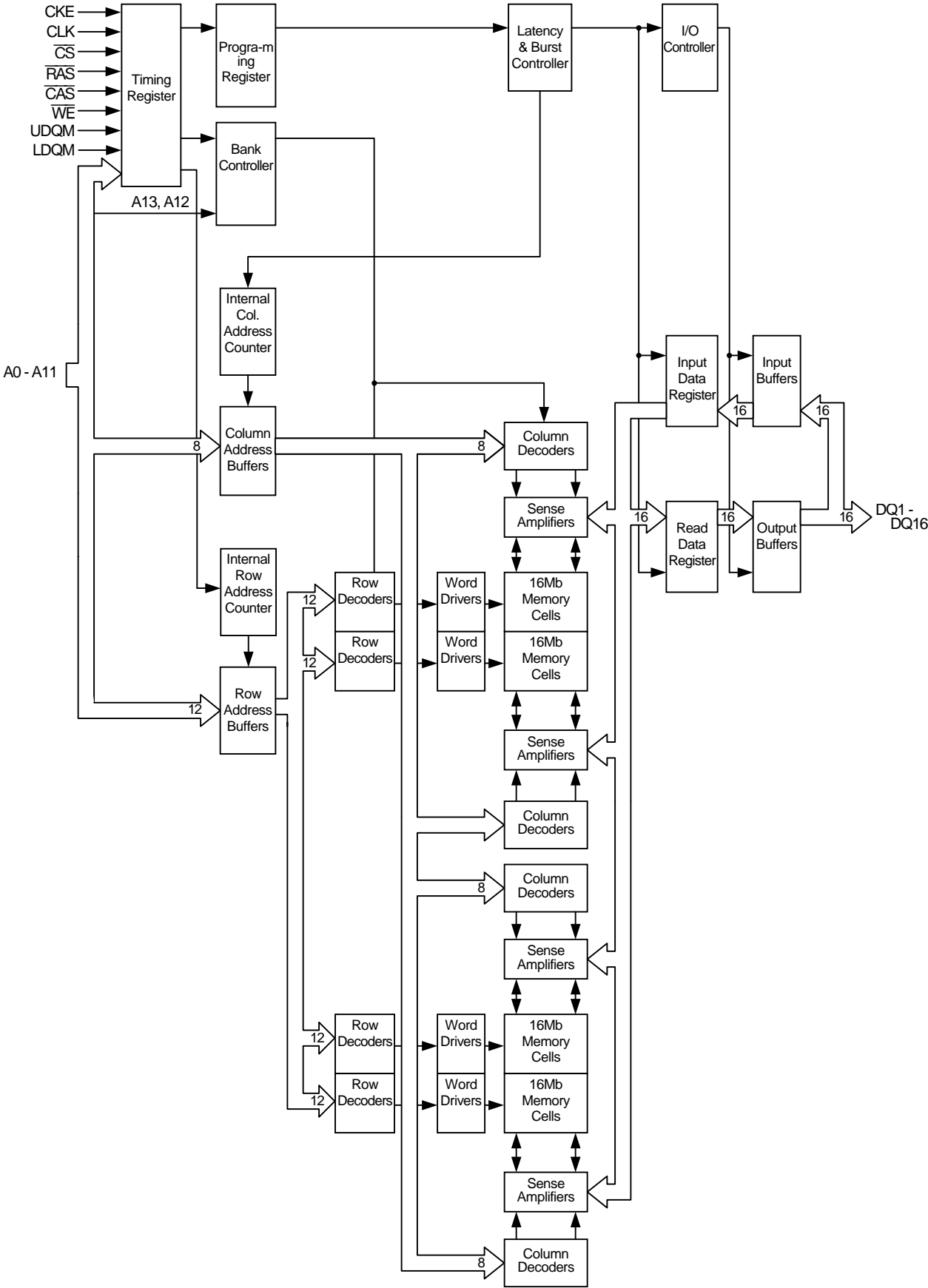
Note : The same power supply voltage must be provided to every V<sub>CC</sub> pin and V<sub>CC</sub>Q pin.

The same GND voltage level must be provided to every V<sub>SS</sub> pin and V<sub>SS</sub>Q pin.

**PIN DESCRIPTION**

CLK	Fetches all inputs at the "H" edge.
$\overline{CS}$	Disables or enables device operation by asserting or deactivating all inputs except CLK, CKE, UDQM and LDQM.
CKE	Masks system clock to deactivate the subsequent CLK operation. If CKE is deactivated, system clock will be masked so that the subsequent CLK operation is deactivated. CKE should be asserted at least one cycle prior to a new command.
Address	Row & column multiplexed. Row address : RA0 – RA11 Column Address : CA0 – CA7
A13, A12 (BA0, BA1)	Selects bank to be activated during row address latch time and selects bank for precharge and read/write during column address latch time.
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$	Functionality depends on the combination. For details, see the function truth table.
UDQM, LDQM	Masks the read data of two clocks later when UDQM and LDQM are set "H" at the "H" edge of the clock signal. Masks the write data of the same clock when UDQM and LDQM are set "H" at the "H" edge of the clock signal. UDQM controls upper byte and LDQM controls lower byte.
DQi	Data inputs/outputs are multiplexed on the same pin.

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
$V_{CC}$ Supply Voltage	$V_{CC}, V_{CCQ}$	-0.5 to 4.6	V
Storage Temperature	$T_{stg}$	-55 to 150	°C
Power Dissipation	$P_{D^*}$	1000	mW
Short Circuit Output Current	$I_{OS}$	50	mA
Operating Temperature	$T_{opr}$	0 to 70	°C

\*:  $T_a = 25^{\circ}\text{C}$ **Recommended Operating Conditions**(Voltages referenced to  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}, V_{CCQ}$	3.0	3.3	3.6	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

**Pin Capacitance** $(V_{bias} = 1.4\text{ V}, T_a = 25^{\circ}\text{C}, f = 1\text{ MHz})$ 

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance (CLK)	$C_{CLK}$	2.5	4	pF
Input Capacitance ( $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{CS}$ , $\overline{CKE}$ , $\overline{UDQM}$ , $\overline{LDQM}$ , A0 - A13)	$C_{IN}$	2.5	5	pF
Input/Output Capacitance (DQ1 – DQ16)	$C_{OUT}$	4	6.5	pF

## DC Characteristics

Parameter	Symbol	Condition			MD56V62160				Unit	Note
					E-7		E-10			
		Bank	CKE	Others	Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	—	—	$I_{OH} = -2.0\text{mA}$	2.4	—	2.4	—	V	
Output Low Voltage	$V_{OL}$	—	—	$I_{OL} = 2.0\text{mA}$	—	0.4	—	0.4	V	
Input Leakage Current	$I_{LI}$	—	—	—	-10	10	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	—	—	—	-10	10	-10	10	$\mu\text{A}$	
Average Power Supply Current (Operating)	$I_{CC1}$	One Bank Active	$\text{CKE} \geq V_{IH}$	$t_{CC} = \text{Min.}$ $t_{RC} = \text{Min.}$ No Burst	—	85	—	70	mA	1,2
	$I_{CC1D}$	Both Banks Active	$\text{CKE} \geq V_{IH}$	$t_{CC} = \text{Min.}$ $t_{RC} = \text{Min.}$ $t_{RRD} = \text{Min.}$ No Burst	—	135	—	115	mA	1,2
Power Supply Current (Standby)	$I_{CC2}$	Both Banks Precharge	$\text{CKE} \geq V_{IH}$	$t_{CC} = \text{Min.}$	—	30	—	30	mA	3
Average Power Supply Current (Clock Suspension)	$I_{CC3S}$	Both Banks Active	$\text{CKE} \leq V_{IL}$	$t_{CC} = \text{Min.}$	—	3	—	3	mA	2
Average Power Supply Current (Active Standby)	$I_{CC3}$	One Bank Active	$\text{CKE} \geq V_{IH}$	$t_{CC} = \text{Min.}$	—	40	—	30	mA	3
Power Supply Current (Burst)	$I_{CC4}$	Both Banks Active	$\text{CKE} \geq V_{IH}$	$t_{CC} = \text{Min.}$	—	110	—	90	mA	1,2
Power Supply Current (Auto-Refresh)	$I_{CC5}$	One Bank Active	$\text{CKE} \geq V_{IH}$	$t_{CC} = \text{Min.}$ $t_{RC} = \text{Min.}$	—	135	—	115	mA	2
Average Power Supply Current (Self-Refresh)	$I_{CC6}$	Both Banks Precharge	$\text{CKE} \leq V_{IL}$	$t_{CC} = \text{Min.}$	—	2	—	2	mA	
Average Power Supply Current (Power Down)	$I_{CC7}$	Both Banks Precharge	$\text{CKE} \leq V_{IL}$	$t_{CC} = \text{Min.}$	—	2	—	2	mA	

- Notes: 1. Measured with outputs open.  
2. The address and data can be changed once or left unchanged during one cycle.  
3. The address and data can be changed once or left unchanged during two cycles. DC

**Mode Set Address Keys**

Single Write		CAS Latency				Burst Type		Burst Length				
A9	BRSW	A6	A5	A4	CL	A3	BT	A2	A1	A0	BT = 0	BT = 1
0	Normal	0	0	0	Reserved	0	Sequential	0	0	0	1	1
1	Single Write	0	0	1	1	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	Reserved			1	0	0	Reserved	Reserved
		1	0	1	Reserved			1	0	1	Reserved	Reserved
		1	1	0	Reserved			1	1	0	Reserved	Reserved
		1	1	1	Reserved			1	1	1	Full Page	Reserved

Notes: A7, A8, A10, A11, A12 and A13 should stay “L” during mode set cycle.

MD56V62160E supports two methods of Power on Sequence.

**POWER ON SEQUENCE 1**

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the  $V_{CC}$  voltage has reached the specified level, pause for 200  $\mu$ s or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Apply a CBR auto-refresh eight or more times.
5. Enter the mode register setting command.

**POWER ON SEQUENCE 2**

1. With inputs in NOP state, turn on the power supply and start the system clock.
2. After the  $V_{CC}$  voltage has reached the specified level, pause for 200  $\mu$ s or more with the input kept in NOP state.
3. Issue the precharge all bank command.
4. Enter the mode register setting command.
5. Apply a CBR auto-refresh eight or more times.

## AC Characteristics (1/2)

Note1, 2

Parameter		Symbol	MD56V62160				Unit	Note
			E-7		E-10			
			Min.	Max.	Min.	Max.		
Clock Cycle Time	CL = 3	t <sub>CC3</sub>	7	—	10	—	ns	
	CL = 2	t <sub>CC2</sub>	10	—	10	—	ns	
	CL = 1	t <sub>CC1</sub>	20	—	20	—	ns	
Access Time from Clock	CL = 3	t <sub>AC3</sub>	—	6	—	6	ns	3, 4
	CL = 2	t <sub>AC2</sub>	—	6	—	6	ns	3, 4
	CL = 1	t <sub>CC1</sub>	—	17	—	17	ns	3, 4
Clock High Pulse Time		t <sub>CH</sub>	2	—	3	—	ns	4
Clock Low Pulse Time		t <sub>CL</sub>	2	—	3	—	ns	4
Input Setup Time		t <sub>SI</sub>	1.5	—	3	—	ns	
Input Hold Time		t <sub>HI</sub>	0.8	—	1	—	ns	
Output Low Impedance Time from Clock		t <sub>OLZ</sub>	1	—	1	—	ns	
Output High Impedance Time from Clock		t <sub>OHZ</sub>	—	6	—	6	ns	
Output Hold from Clock		t <sub>OH</sub>	2	—	3	—	ns	3
Random Read or Write Cycle Time		t <sub>RC</sub>	69	—	70	—	ns	
R <sub>AS</sub> Precharge Time		t <sub>RP</sub>	20	—	20	—	ns	
R <sub>AS</sub> Pulse Width		t <sub>RAS</sub>	49	100,000	50	100,000	ns	
R <sub>AS</sub> to C <sub>AS</sub> Delay Time		t <sub>RCD</sub>	20	—	20	—	ns	
Write Recovery Time		t <sub>WR</sub>	8	—	10	—	ns	
R <sub>AS</sub> to C <sub>AS</sub> Bank Active Delay Time		t <sub>RRD</sub>	14	—	20	—	ns	
Refresh Time		t <sub>REF</sub>	—	64	—	64	ms	
Power-down Exit setup Time		t <sub>RDE</sub>	t <sub>SI</sub> + 1CLK	—	t <sub>SI</sub> + 1CLK	—	ns	
C <sub>AS</sub> to C <sub>AS</sub> Delay Time (Min.)		t <sub>CCD</sub>	1		1		Cycle	
Clock Disable Time from CKE		t <sub>CKE</sub>	1		1		Cycle	
Data Output High Impedance Time from UDQM, LDQM		t <sub>DOZ</sub>	2		2		Cycle	
Data Input Mask Time from UDQM, LDQM		t <sub>DOD</sub>	0		0		Cycle	



**AC Characteristics (2/2)**

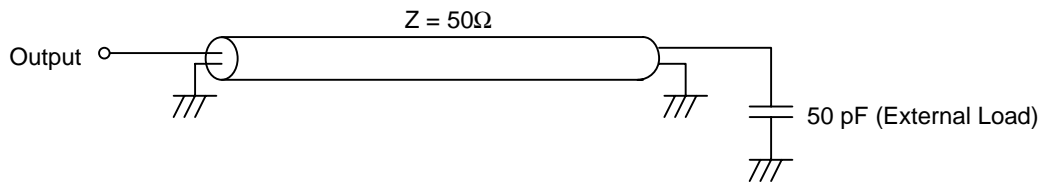
Note1, 2

Parameter	Symbol	MD56V62160				Unit	Note
		E-7		E-10			
		Min.	Max.	Min.	Max.		
Data Input Mask Time from Write Command	I <sub>DWD</sub>	0		0		Cycle	
Data Output High Impedance Time from Precharge Command	I <sub>ROH</sub>	CL		CL		Cycle	
Active Command Input Time from Mode Register Set Command Input (Min.)	I <sub>MRD</sub>	2		2		Cycle	
Write Command Input Time from Output	I <sub>OWD</sub>	2		2		Cycle	

Notes: 1. AC measurements assume that  $t_T = 1$  ns.

2. The reference level for timing of input signals is 1.4 V.  
 The input signal conditions are below.  
 $V_{IH} = 2.4$  V,  $V_{IL} = 0.4$  V

3. Output load.

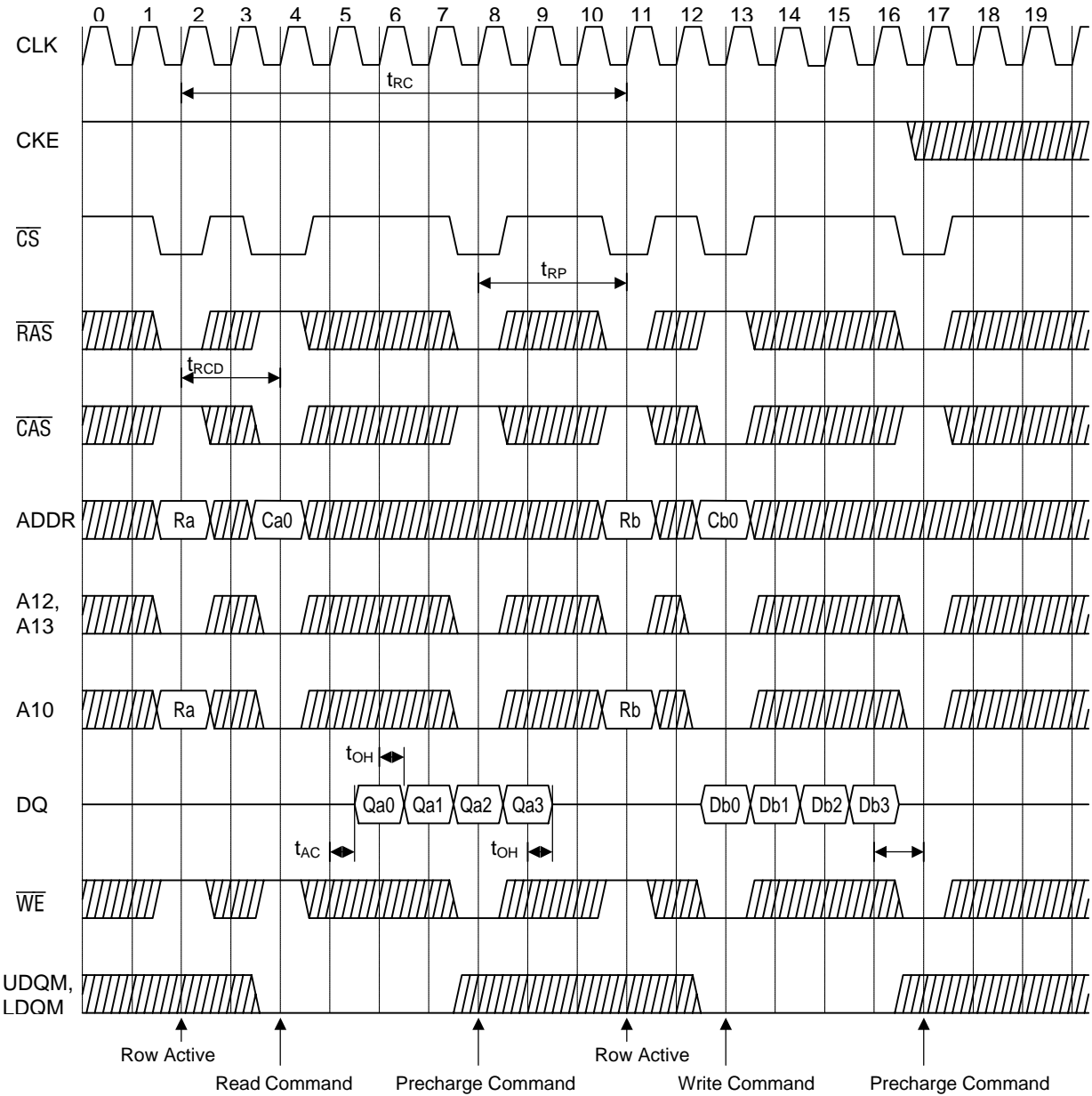


4. The access time is defined at 1.4 V.

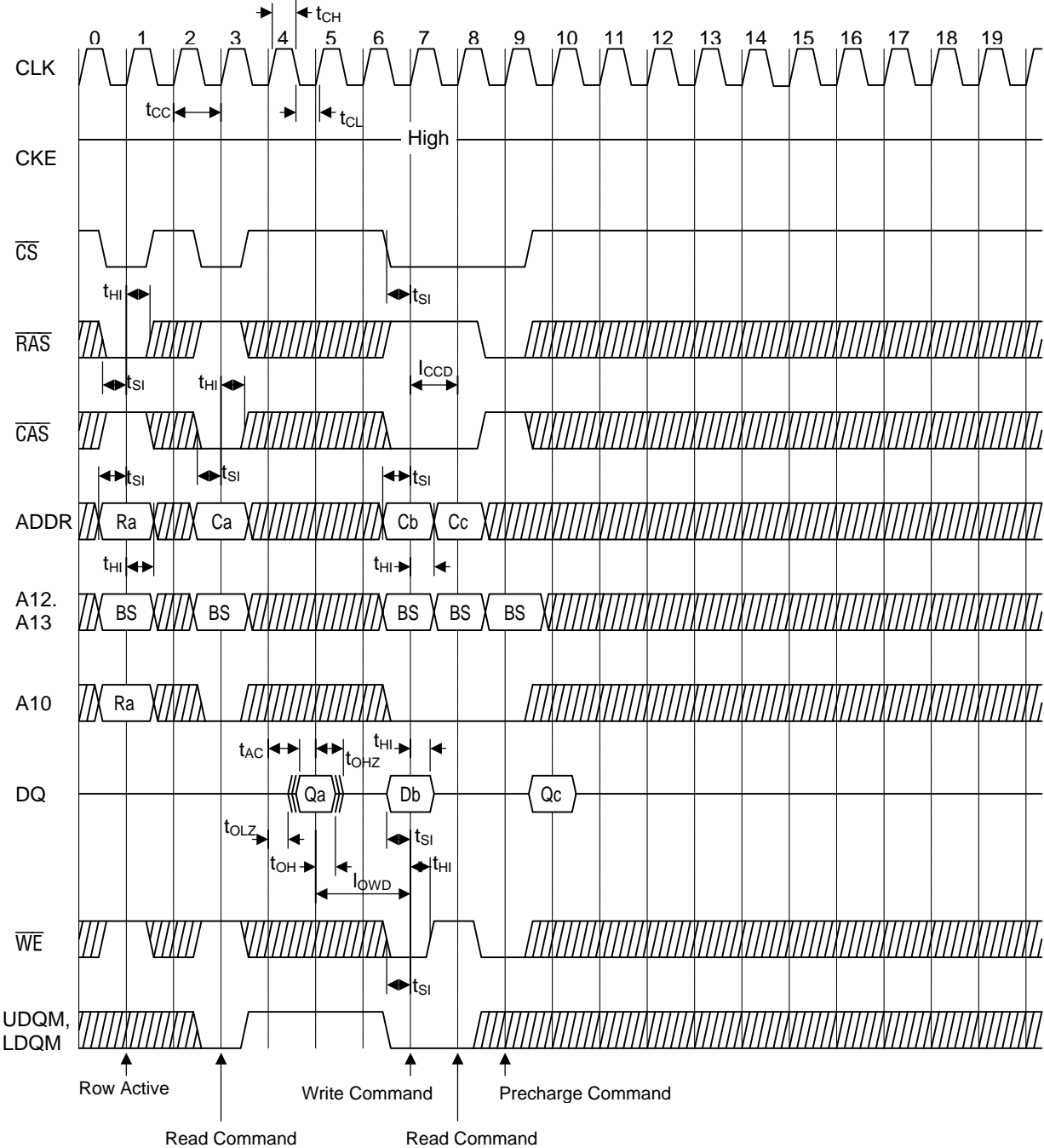
5. If  $t_T$  is longer than 1 ns, then the reference level for timing of input signals is  $V_{IH}$  and  $V_{IL}$ .

TIMING CHART

Read & Write Cycle (Same Bank) @CAS Latency = 2, Burst Length = 4



Single Bit Read-Write-Read Cycle (Same Page) @CAS Latency = 2, Burst Length = 4



- \*Notes: 1. When  $\overline{CS}$  is set “High” at a clock transition from “Low” to “High”, all inputs except CLK, CKE, UDQM and LDQM are invalid.
2. When issuing an active, read or write command, the bank is selected by A12 and A13.

A11	A12	Active, read or write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

3. The auto precharge function is enabled or disabled by the A10 input when the read or write command is issued.

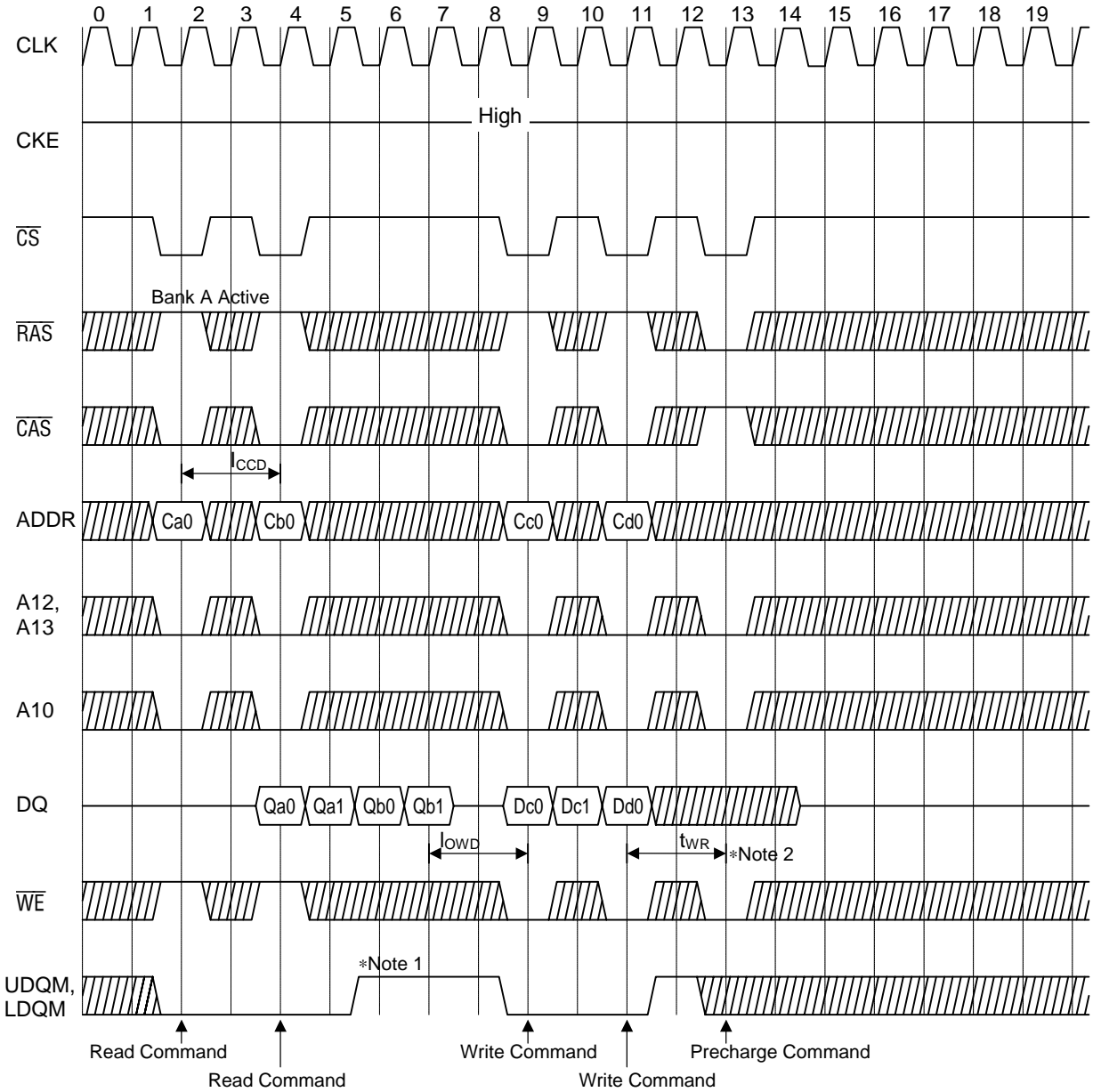
A10	A12	A13	Operation
0	0	0	After the end of burst, bank A holds the idle status.
1	0	0	After the end of burst, bank A is precharged automatically.
0	0	1	After the end of burst, bank B holds the idle status.
1	0	1	After the end of burst, bank B is precharged automatically.
0	1	0	After the end of burst, bank C holds the idle status.
1	1	0	After the end of burst, bank C is precharged automatically.
0	1	1	After the end of burst, bank D holds the idle status.
1	1	1	After the end of burst, bank D is precharged automatically.

4. When issuing a precharge command, the bank to be precharged is selected by the A10 and A11 inputs.

A10	A12	A13	Operation
0	0	0	Bank A is precharged.
0	0	1	Bank B is precharged.
0	1	0	Bank C is precharged.
0	1	1	Bank D is precharged.
1	X	X	All banks are precharged.

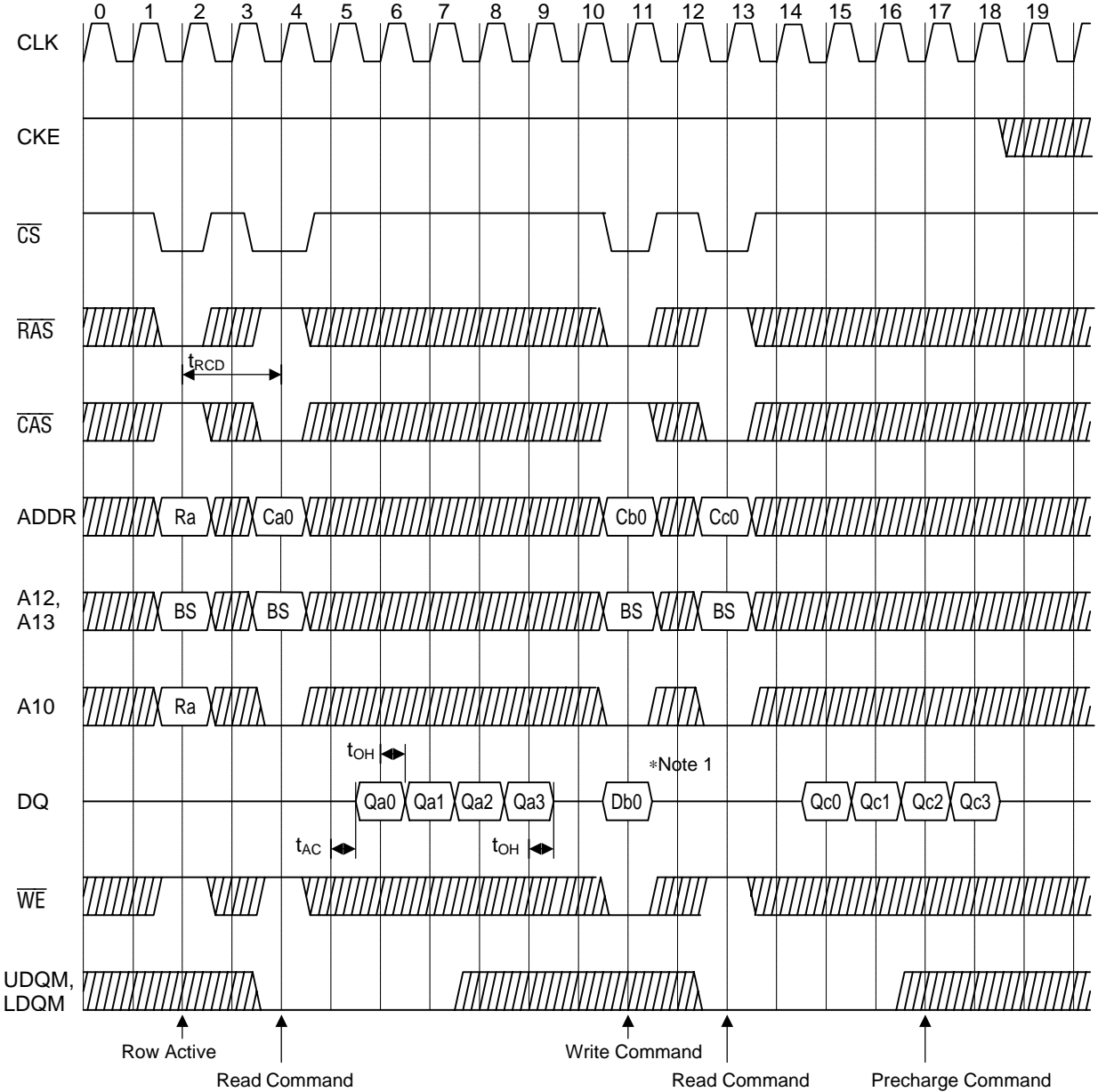
5. The input data and the write command are latched by the same clock (Write latency = 0).
6. The output is forced to high impedance by  $(1CLK + t_{OHZ})$  after UDQM, LDQM entry.

Page Read & Write Cycle (Same Bank) @CAS Latency = 2, Burst Length = 4



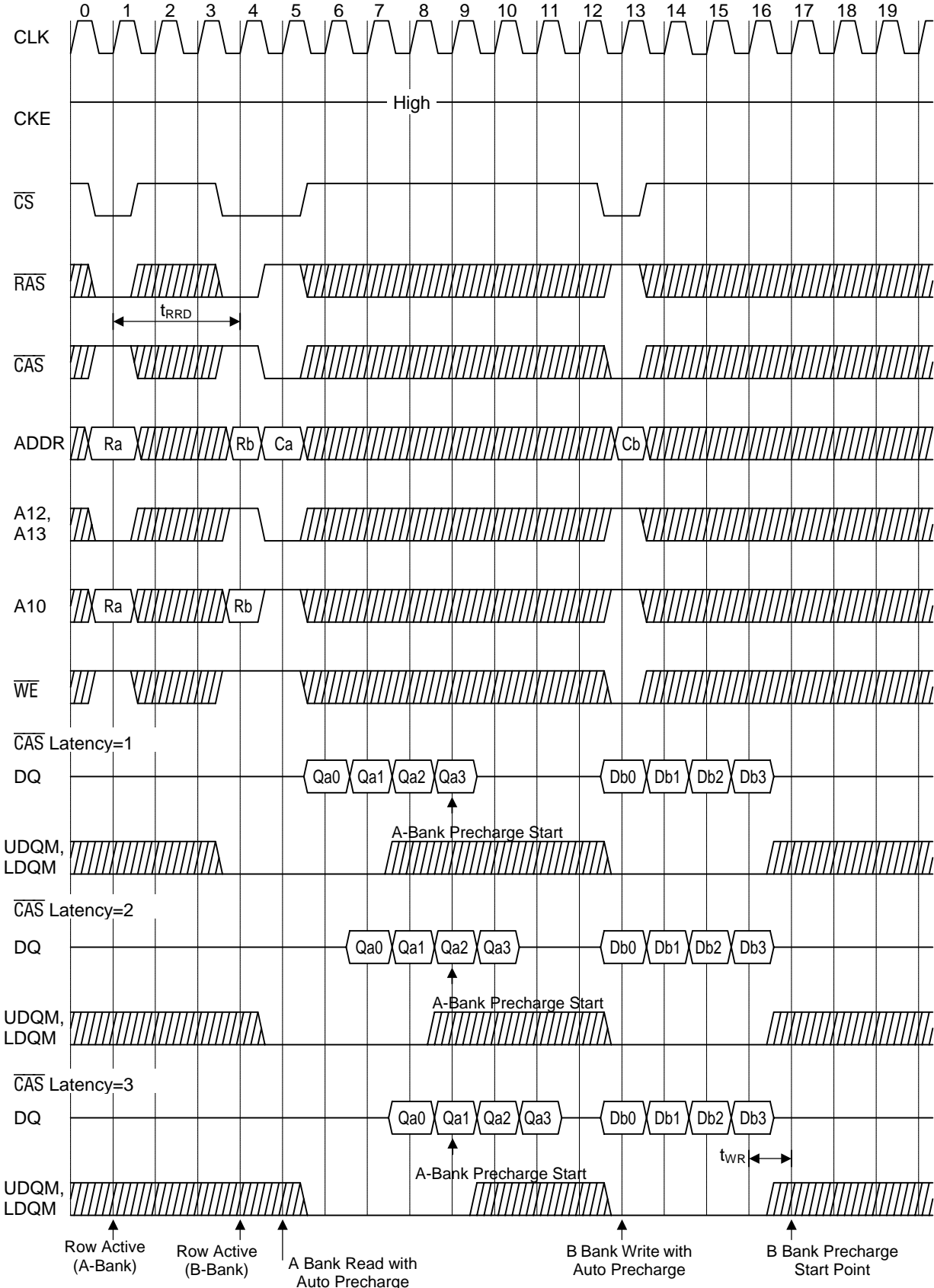
\*Notes: 1. To write data before a burst read ends, UDQM and LDQM should be asserted three cycles prior to the write command to avoid bus contention.  
 2. To assert row precharge before a burst write ends, wait  $t_{WR}$  after the last write data input. Input data during the precharge input cycle will be masked internally.

**Burst Read & Single Write Cycle (Same Bank) @CAS Latency = 2, Burst Length = 4**

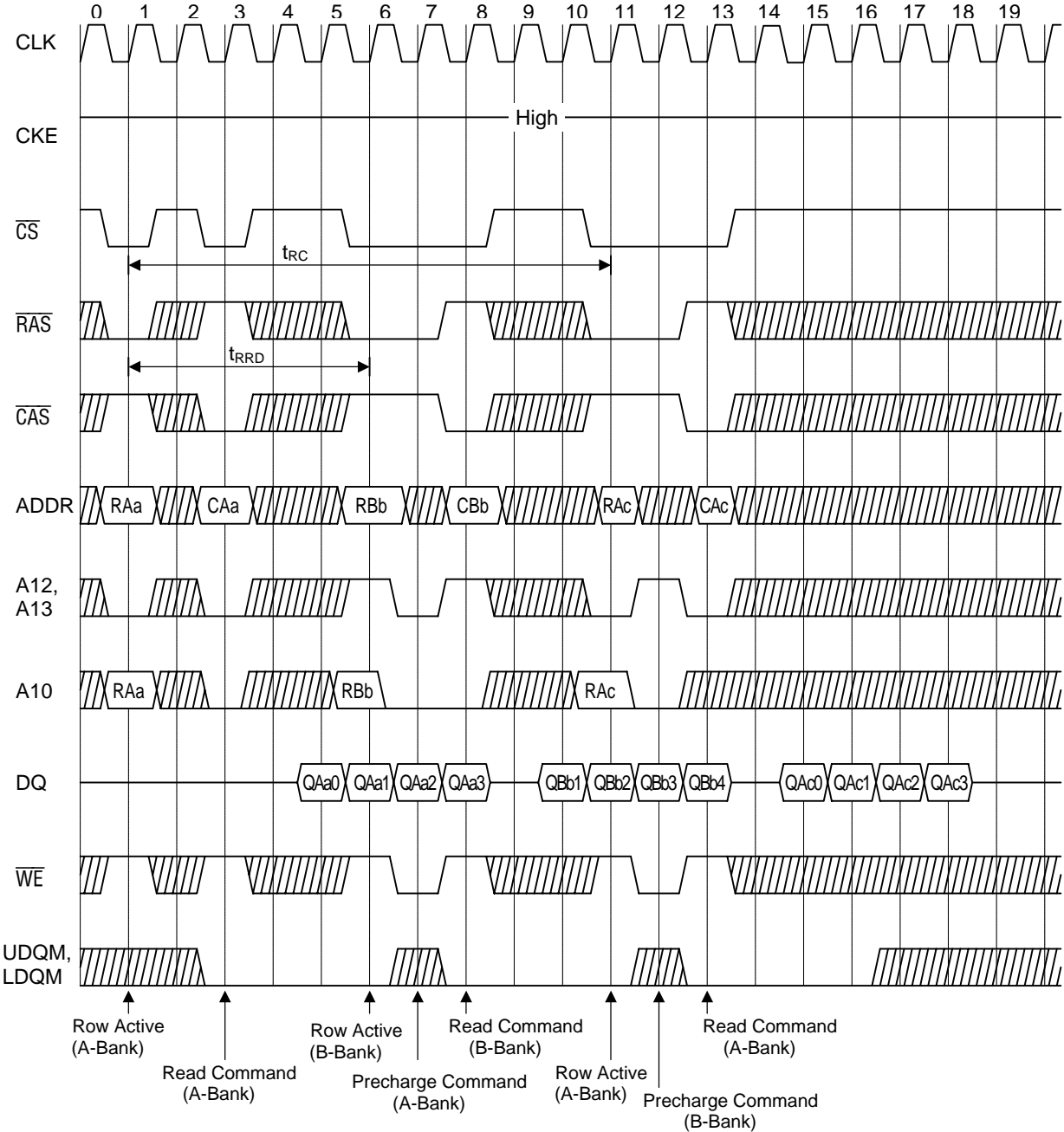


\*Note: 1. If you set A9 to high during mode register set cycle, the write burst length is set to 1.

Read & Write Cycle with Auto Precharge @ Burst Length = 4

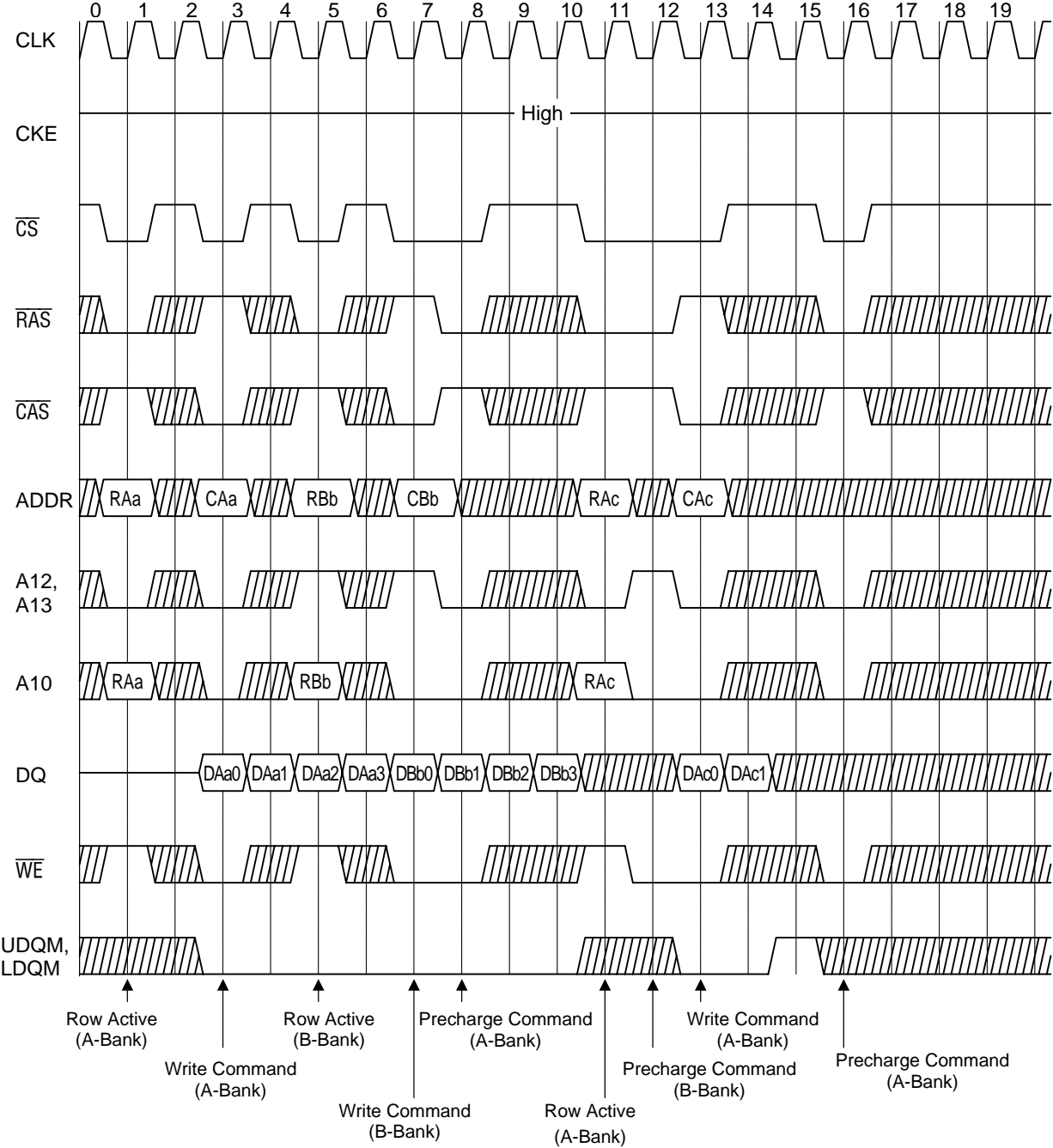


Bank Interleave Random Row Read Cycle @CAS Latency = 2, Burst Length = 4

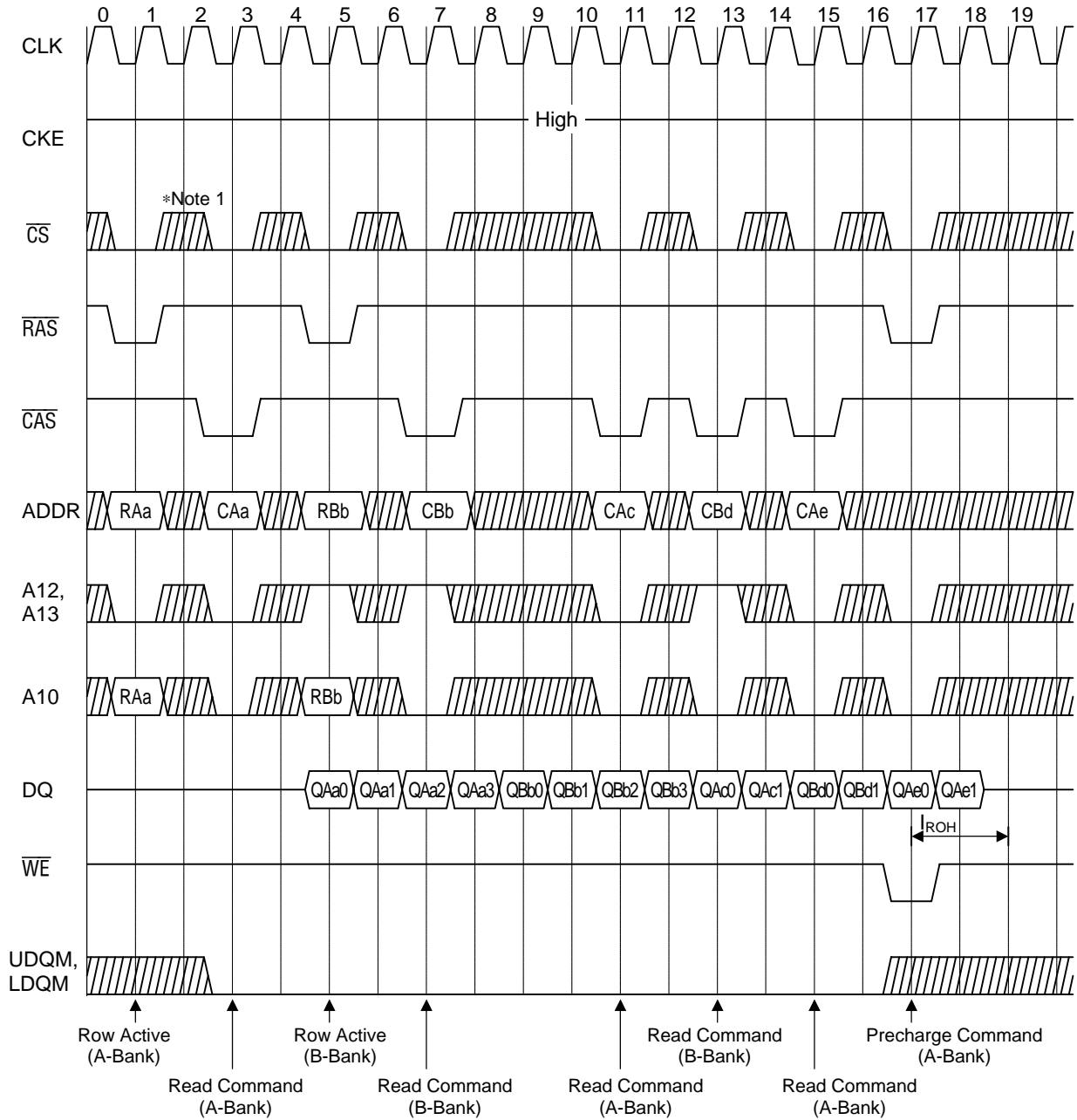




Bank Interleave Random Row Write Cycle @CAS Latency = 2, Burst Length = 4

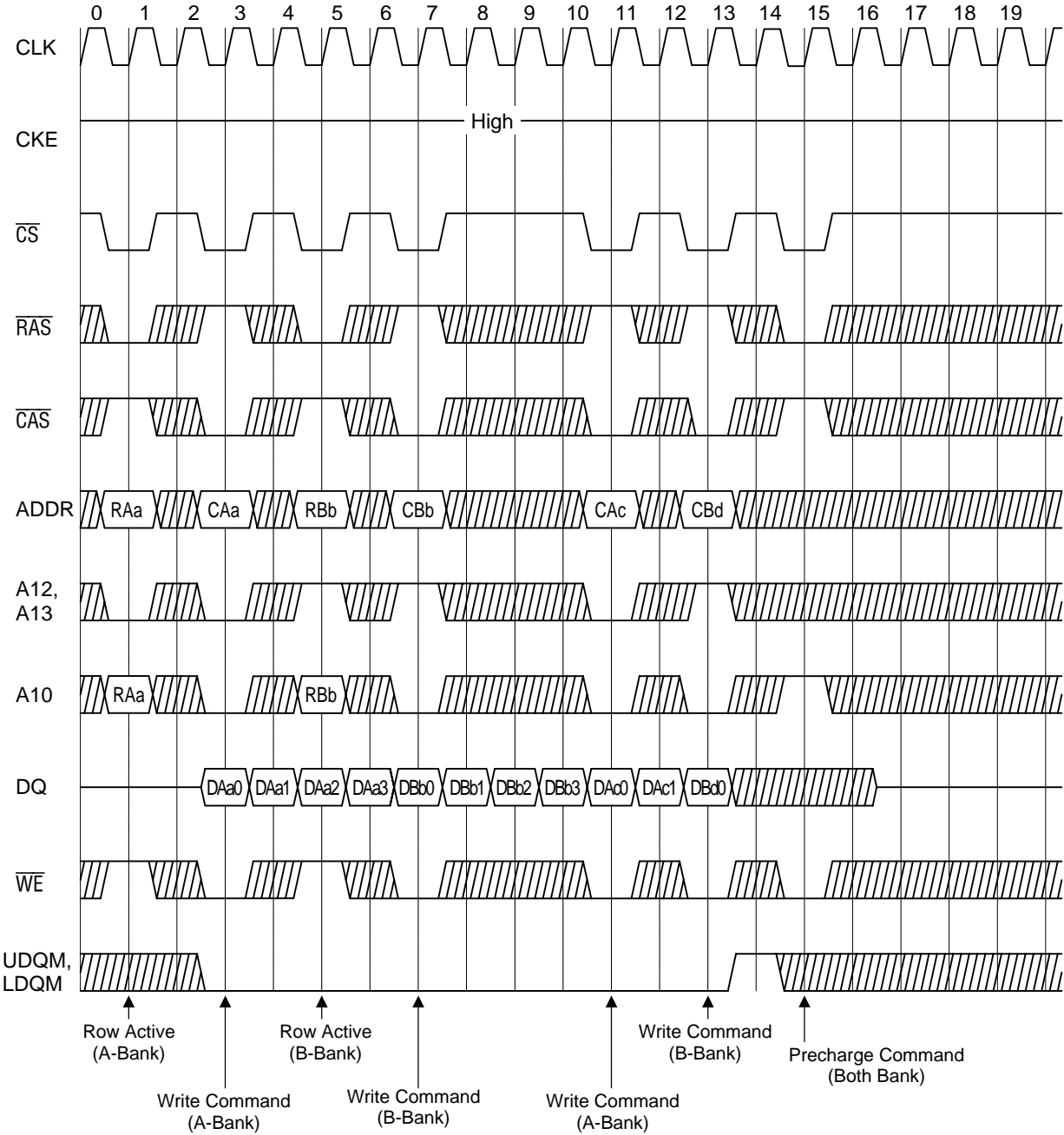


Bank Interleave Page Read Cycle @CAS Latency = 2, Burst Length = 4

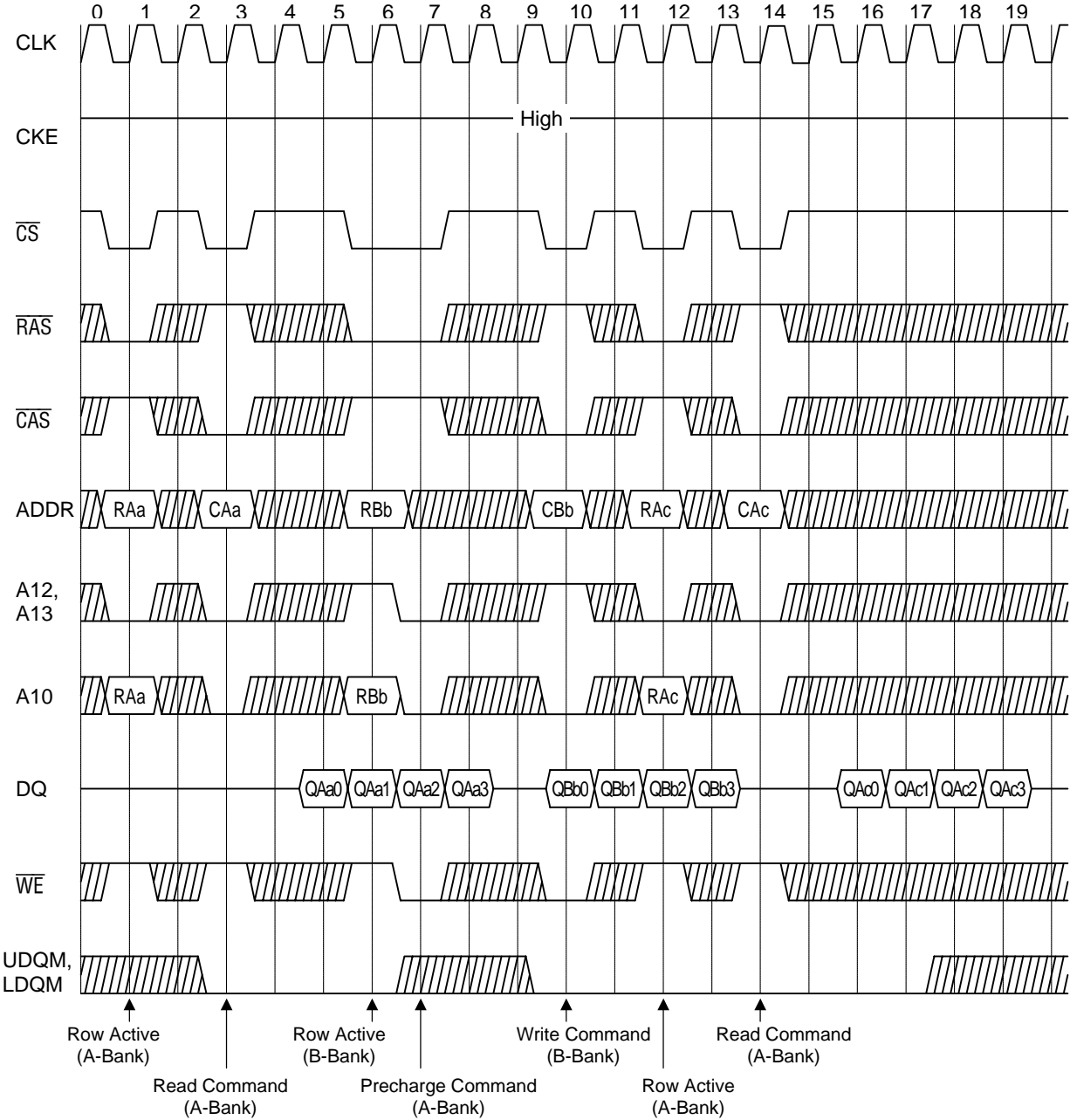


\*Note: 1. CS is ignored when RAS, CAS and WE are high at the same cycle.

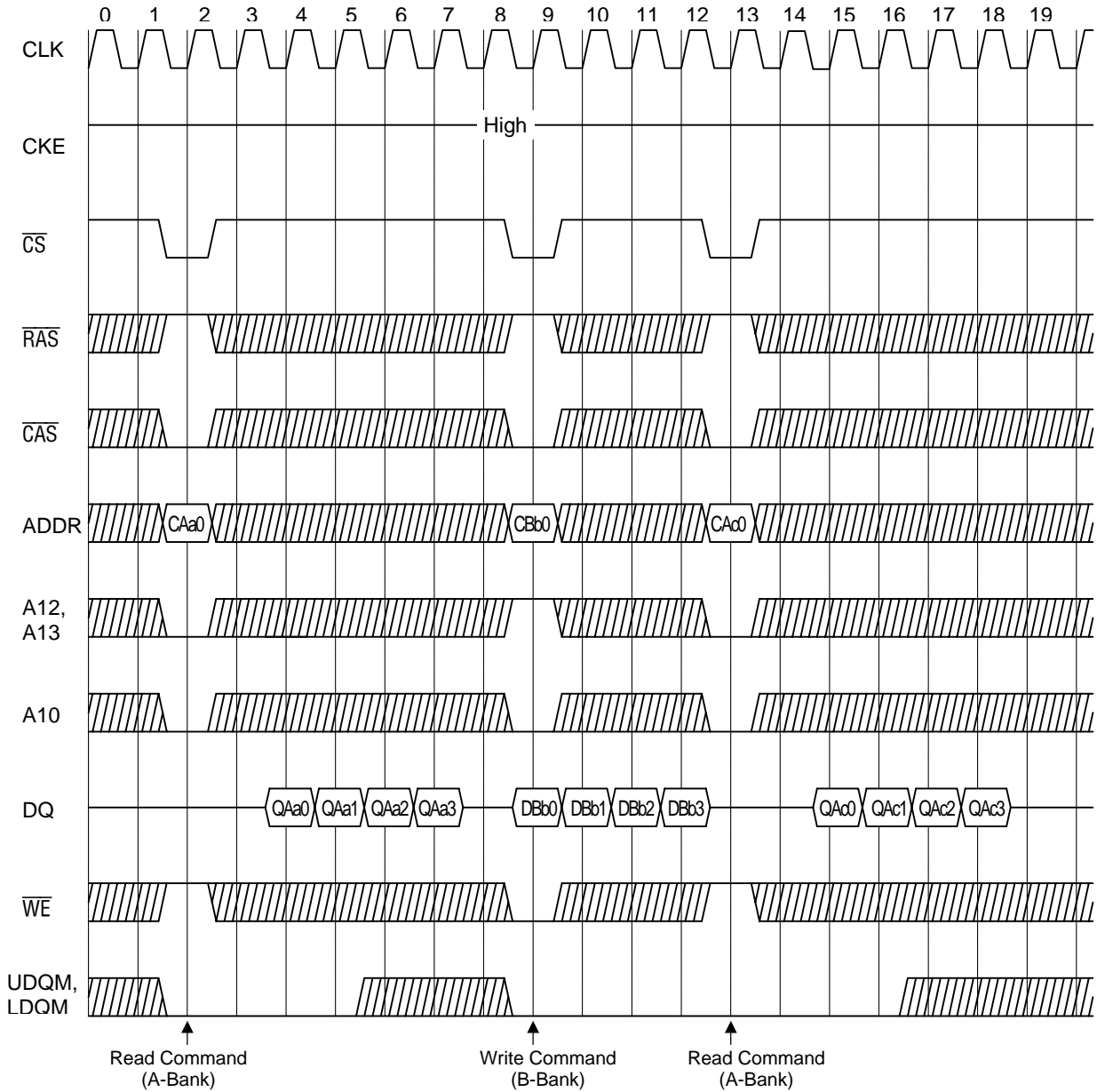
Bank Interleave Page Write Cycle @CAS Latency = 2, Burst Length = 4



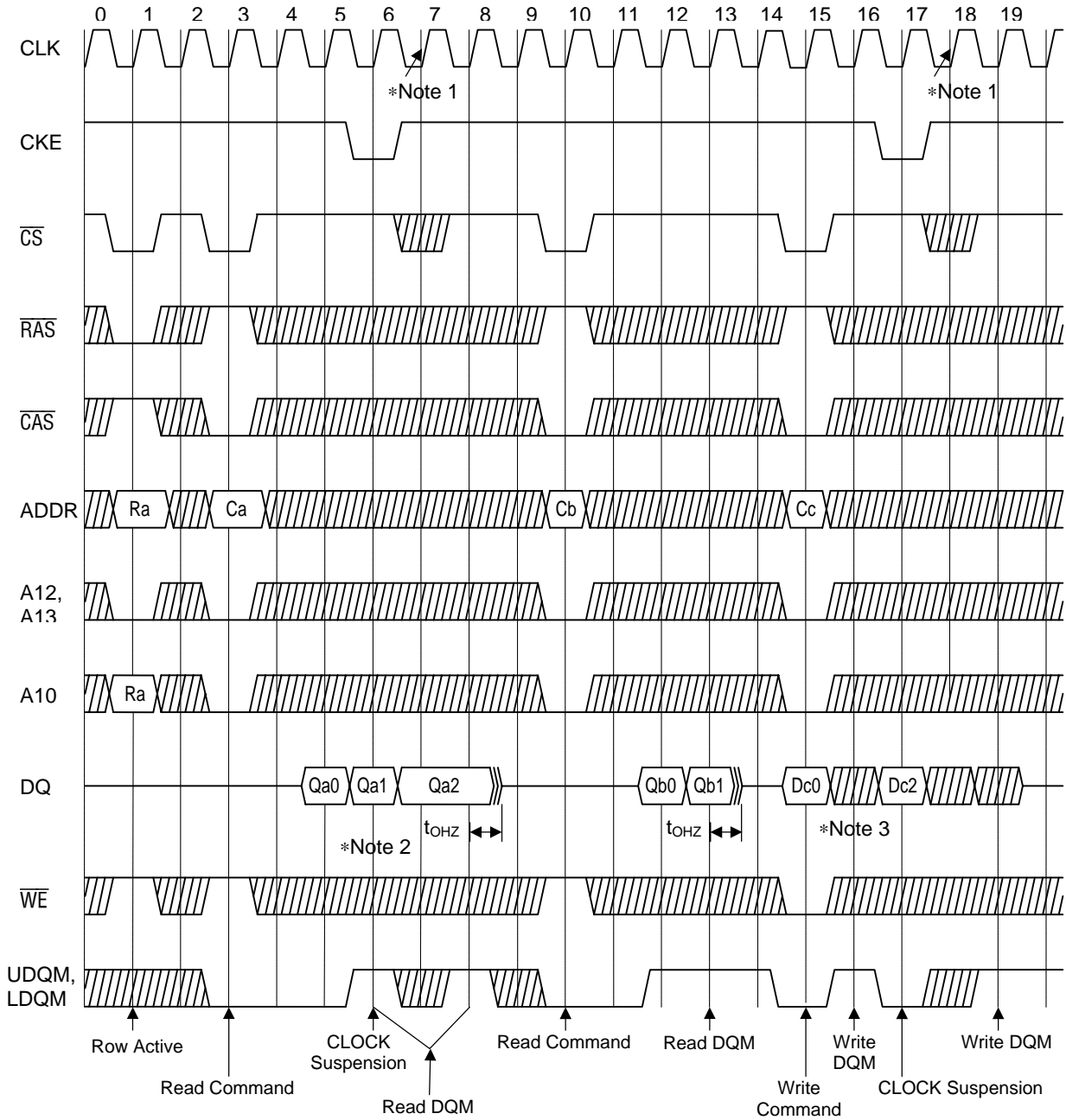
Bank Interleave Random Row Read/Write Cycle @CAS Latency = 2, Burst Length = 4



Bank Interleave Page Read/Write Cycle @CAS Latency = 2, Burst Length = 4

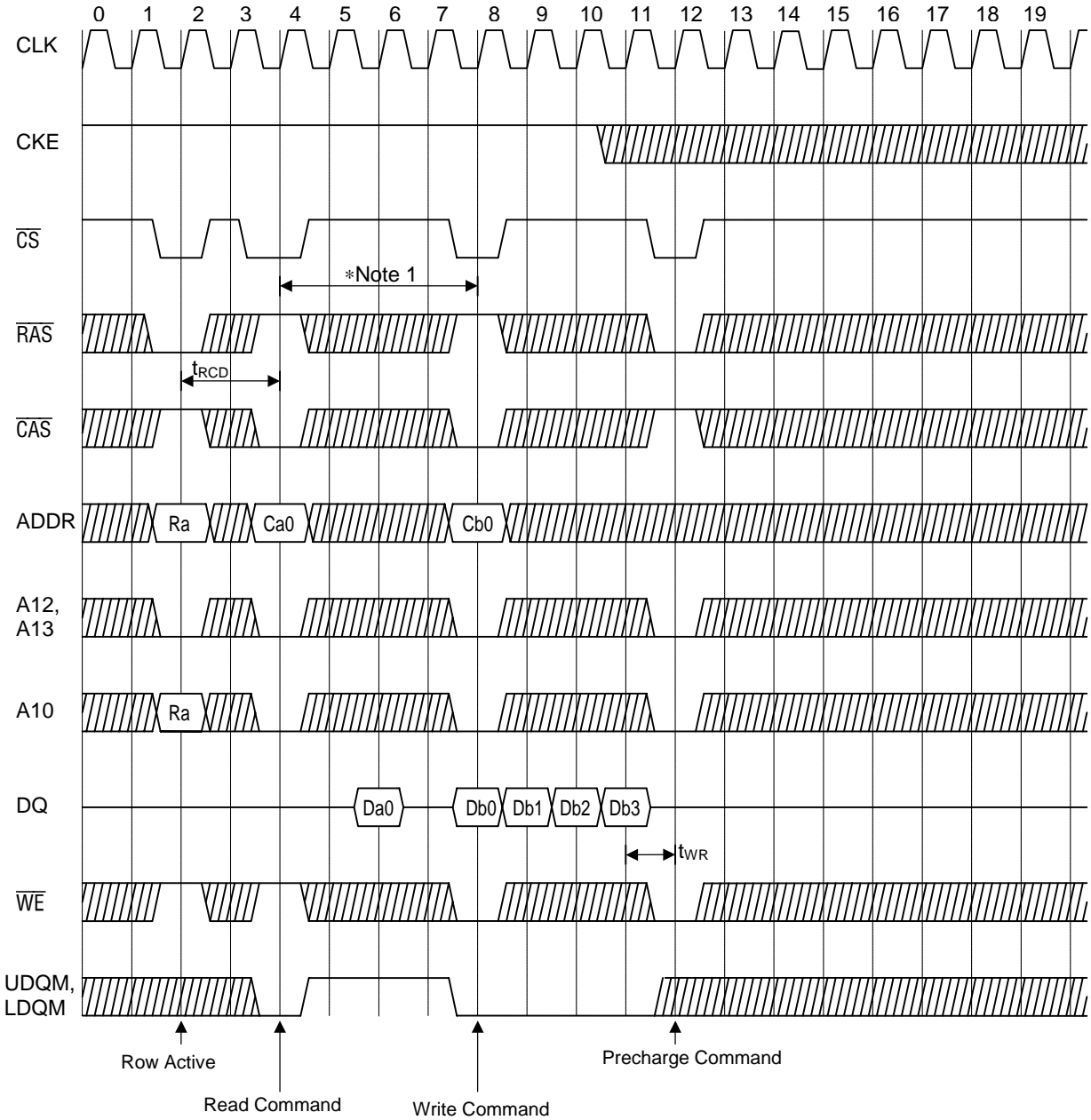


Clock Suspension & DQM Operation Cycle @CAS Latency = 2, Burst Length = 4



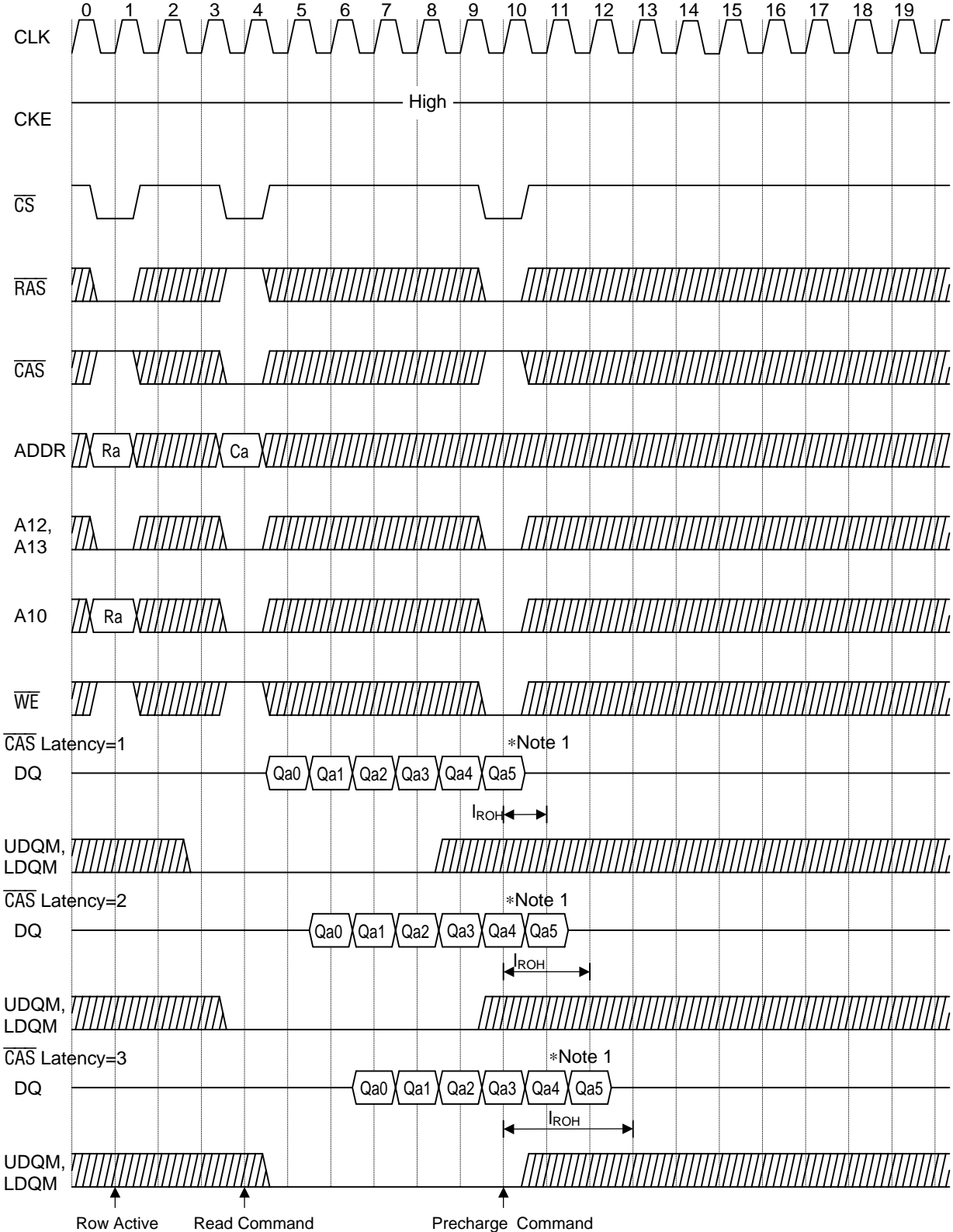
- \*Note: 1. When Clock Suspension is asserted, the next clock cycle is ignored.
- 2. When UDQM and LDQM are asserted, the read data after two clock cycles is masked.
- 3. When UDQM and LDQM are asserted, the write data in the same clock cycle is masked.
- 4. When LDQM is set High, the input/output data of DQ1 – DQ8 is masked.
- 5. When UDQM is set High, the input/output data of DQ9 – DQ16 is masked.

Read to Write Cycle (Same Bank) @CAS Latency = 2, Burst Length = 4



\*Note: 1. In Case  $\overline{\text{CAS}}$  latency is 3, READ can be interrupted by WRITE.  
The minimum command interval is [burst length + 1] cycles.  
UDQM, LDQM must be high at least 3 clocks prior to the write command.

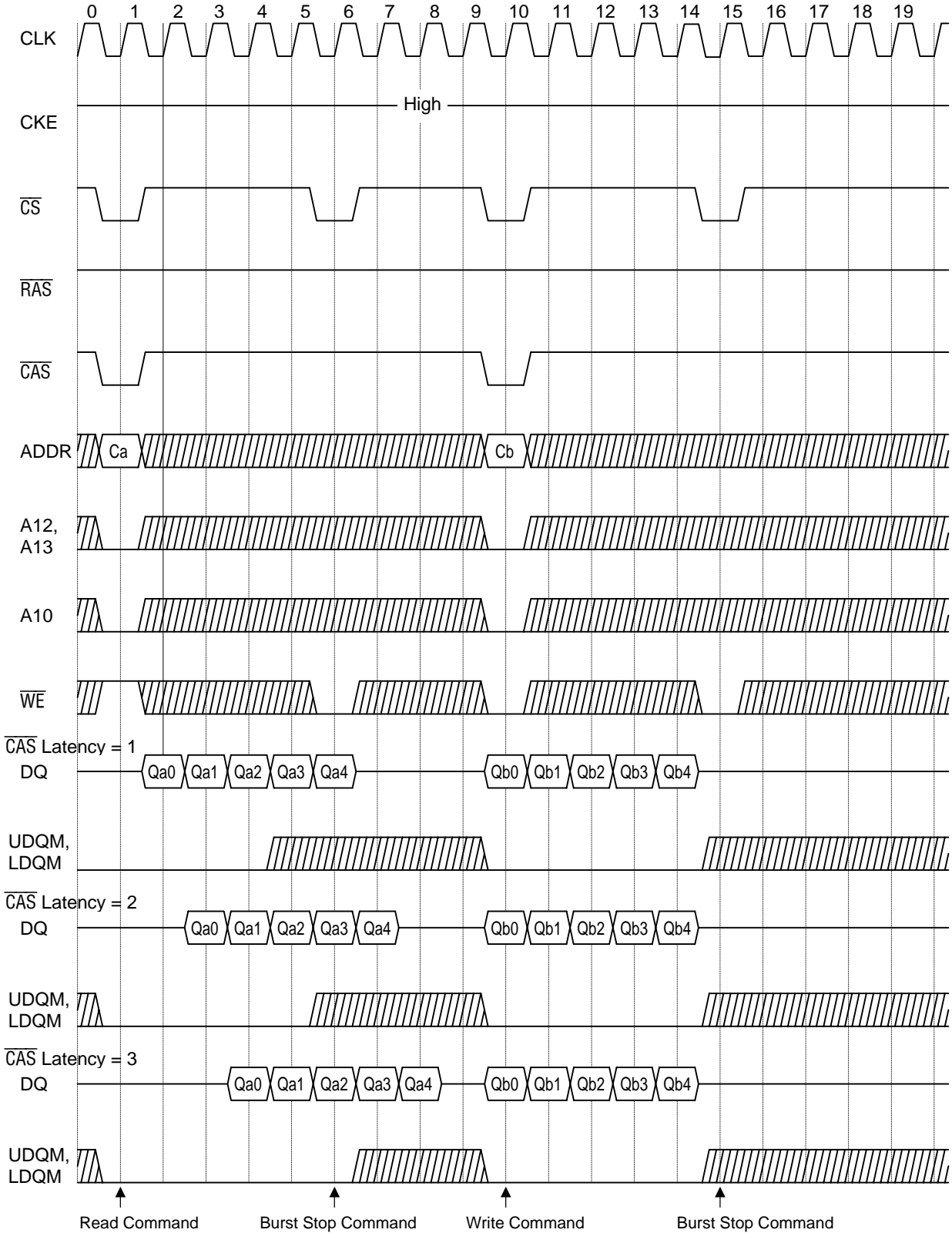
Read Interruption by Precharge Command @Burst Length = 8



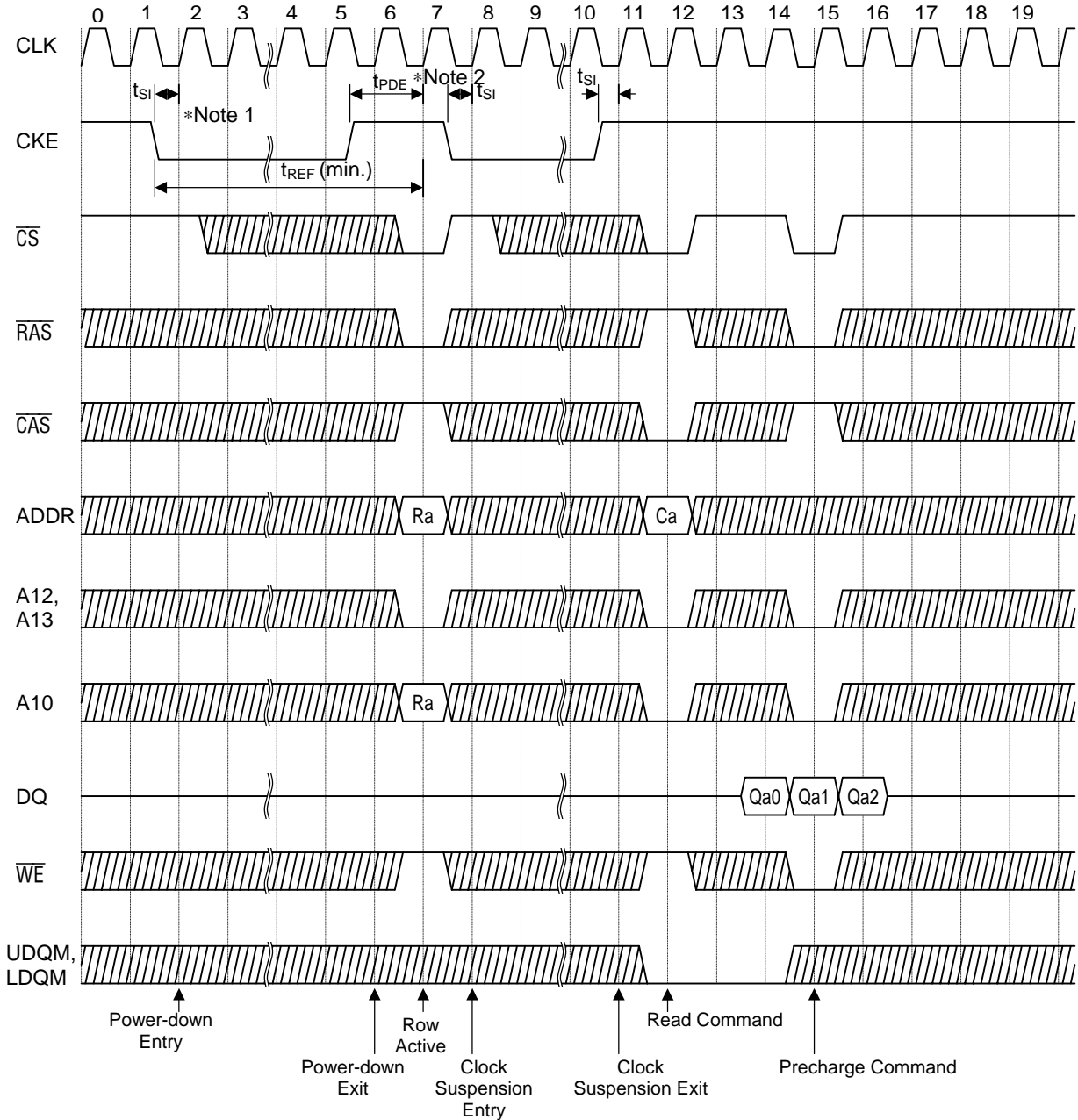
\*Note: 1. If row precharge is asserted before a burst read ends, then the read data will not output after IROH equals CAS latency.



**Burst Stop Command @Burst Length = 8**

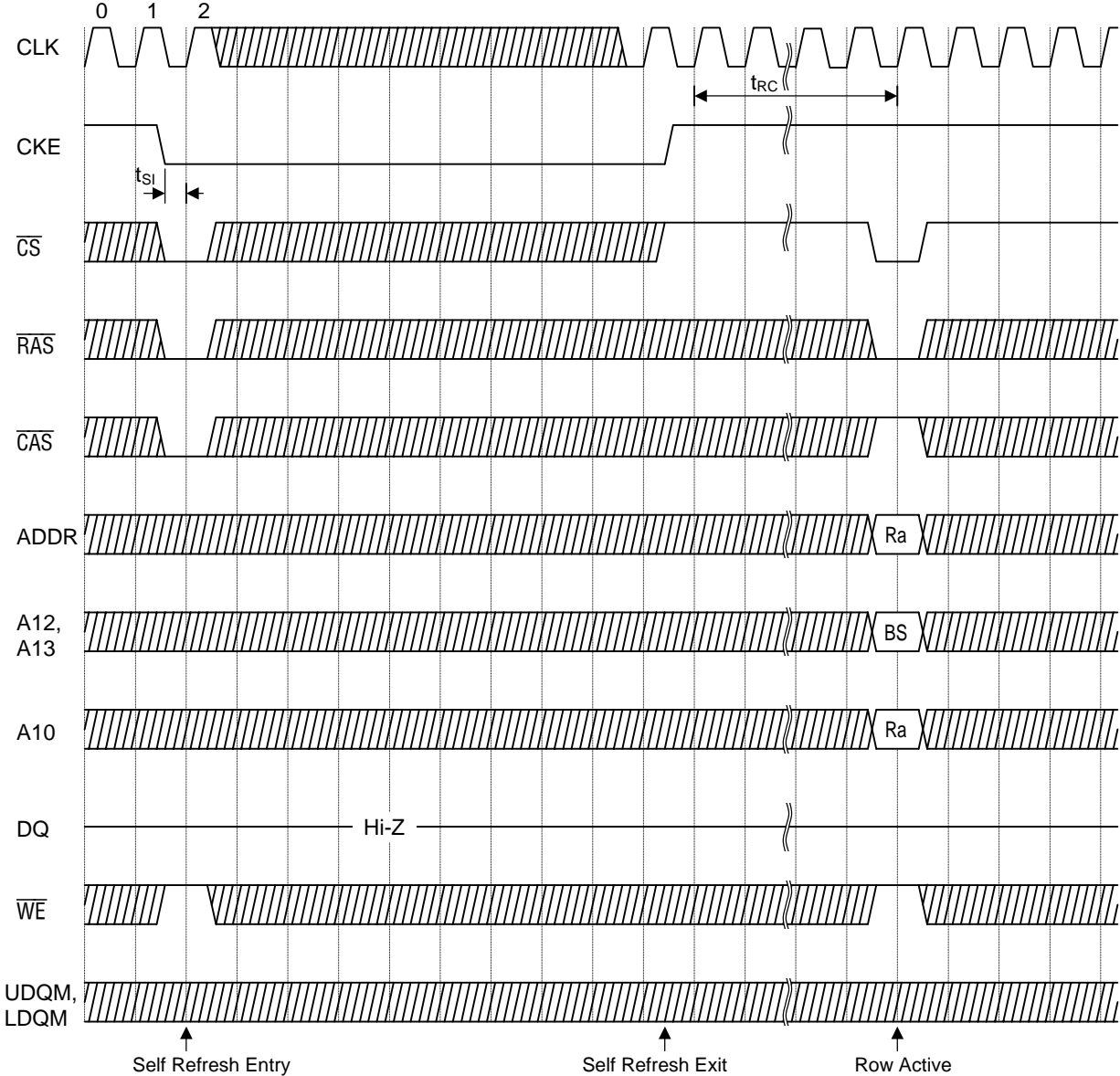


Power Down Mode @CAS Latency = 2, Burst Length = 4



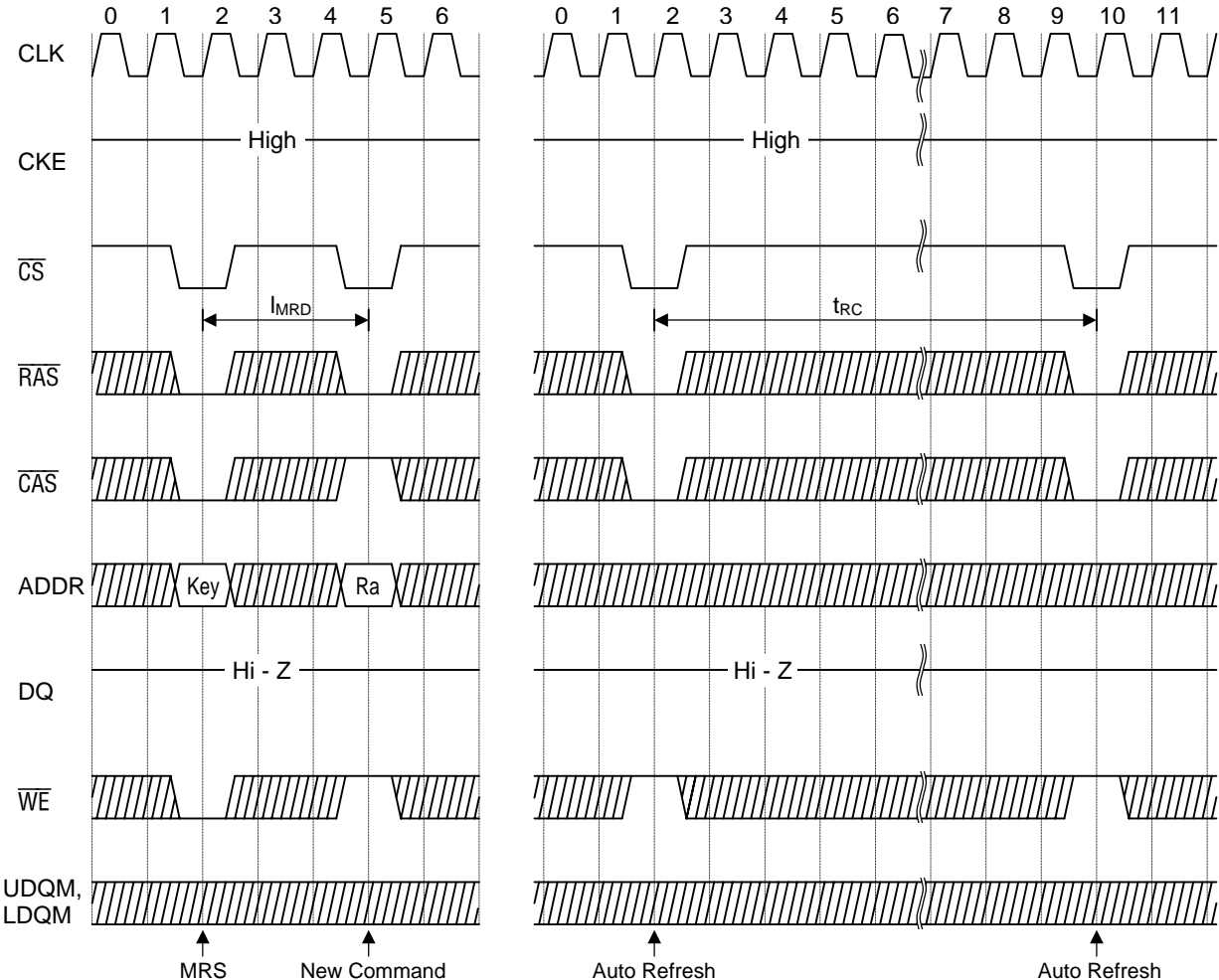
\*Note: 1. When both banks are in precharge state, and if CKE is set low, then the MD56V62160E enters power-down mode and maintains the mode while CKE is low.  
 2. To release the circuit from power-down mode, CKE has to be set high for longer than  $t_{PDE} (t_{SI} + 1CLK)$ .

Self Refresh Cycle



Mode Register Set Cycle

Auto Refresh Cycle



FUNCTION TRUTH TABLE (Table 1) (1/2)

Current State <sup>1</sup>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Idle	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	Row Active
	L	L	H	L	BA	A10	NOP <sup>4</sup>
	L	L	L	H	X	X	Auto-Refresh or Self-Refresh <sup>5</sup>
	L	L	L	L	L	OP Code	Mode Register Write
Row Active	H	X	X	X	X	X	NOP
	L	H	H	X	X	X	NOP
	L	H	L	H	BA	CA, A10	Read
	L	H	L	L	BA	CA, A10	Write
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Precharge
	L	L	L	X	X	X	ILLEGAL
Read	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	X	X	Term Burst --> Row Active
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read <sup>3</sup>
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write <sup>3</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge
	L	L	L	X	X	X	ILLEGAL
Write	H	X	X	X	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	H	X	X	NOP (Continue Row Active after Burst ends)
	L	H	H	L	X	X	Term Burst --> Row Active
	L	H	L	H	BA	CA, A10	Term Burst, start new Burst Read <sup>3</sup>
	L	H	L	L	BA	CA, A10	Term Burst, start new Burst Write <sup>3</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	Term Burst, execute Row Precharge <sup>3</sup>
	L	L	L	X	X	X	ILLEGAL
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA, A10	ILLEGAL <sup>2</sup>
	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	H	X	X	NOP (Continue Burst to End and enter Row Precharge)
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	H	BA	CA, A10	ILLEGAL <sup>2</sup>

**FUNCTION TRUTH TABLE (Table 1) (2/2)**

Current State <sup>1</sup>	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	Action
Write with Auto Precharge	L	H	L	L	X	X	ILLEGAL
	L	L	H	X	BA	RA, A10	ILLEGAL <sup>2</sup>
	L	L	L	X	X	X	ILLEGAL
Precharge	H	X	X	X	X	X	NOP --> Idle after t <sub>RP</sub>
	L	H	H	H	X	X	NOP --> Idle after t <sub>RP</sub>
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	NOP <sup>4</sup>
	L	L	L	X	X	X	ILLEGAL
Write Recovery	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	ILLEGAL <sup>2</sup>
Row Active	L	L	L	X	X	X	ILLEGAL
	H	X	X	X	X	X	NOP --> Row Active after t <sub>RCD</sub>
	L	H	H	H	X	X	NOP --> Row Active after t <sub>RCD</sub>
	L	H	H	L	BA	X	ILLEGAL <sup>2</sup>
	L	H	L	X	BA	CA	ILLEGAL <sup>2</sup>
	L	L	H	H	BA	RA	ILLEGAL <sup>2</sup>
	L	L	H	L	BA	A10	ILLEGAL <sup>2</sup>
Refresh	L	L	L	X	X	X	ILLEGAL
	H	X	X	X	X	X	NOP --> Idle after t <sub>RC</sub>
	L	H	H	X	X	X	NOP --> Idle after t <sub>RC</sub>
	L	H	L	X	X	X	ILLEGAL
	L	L	H	X	X	X	ILLEGAL
Mode Register Access	L	L	L	X	X	X	ILLEGAL
	H	X	X	X	X	X	NOP
	L	H	H	H	X	X	NOP
	L	H	H	L	X	X	ILLEGAL
	L	H	L	X	X	X	ILLEGAL
Mode Register Access	L	L	X	X	X	X	ILLEGAL

**ABBREVIATIONS**

RA = Row Address      BA = Bank Address      NOP = No Operation command  
CA = Column Address    AP = Auto Precharge

- \*Notes :1. All inputs are enabled when CKE is set high for at least 1 cycle prior to the inputs.  
2. Illegal to bank in specified state, but may be legal in some cases depending on the state of bank selection.  
3. Satisfy the timing of I<sub>CCD</sub> and t<sub>WR</sub> to prevent bus contention.  
4. NOP to bank precharging or in idle state. Precharges activated bank by BA or A10.  
5. Illegal if any bank is not idle.

**FUNCTION TRUTH TABLE for CKE (Table 2)**

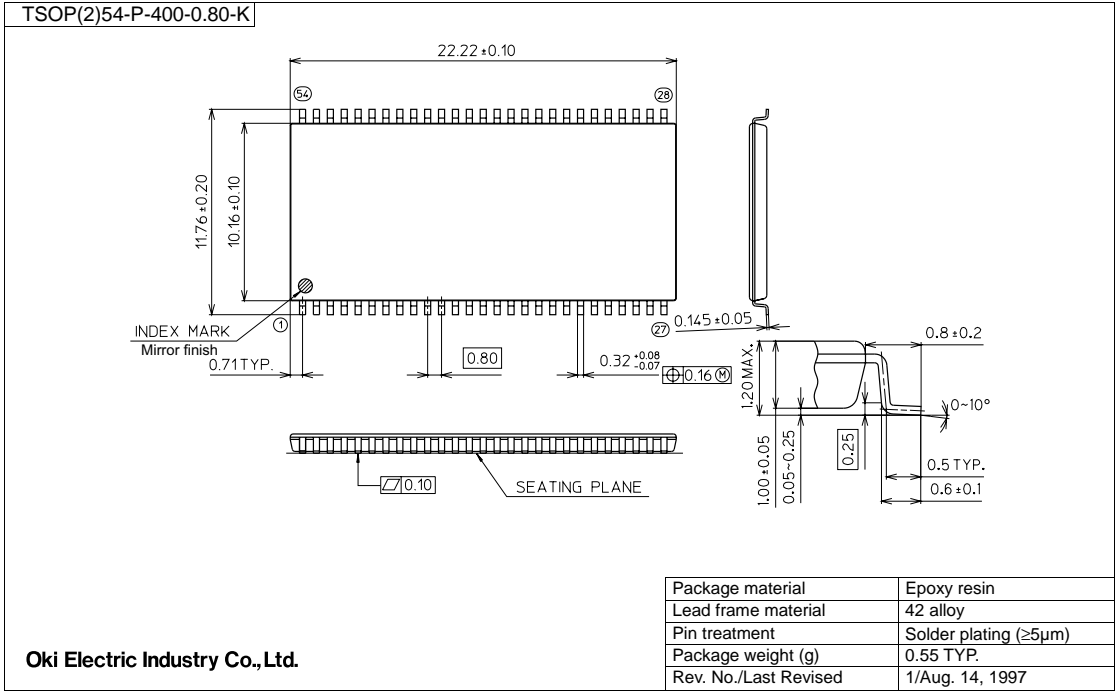
Current State (n)	CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	Action
Self Refresh <sup>6</sup>	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self Refresh --> ABI
	L	H	L	H	H	H	X	Exit Self Refresh --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)
Power Down <sup>6</sup>	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Power Down --> ABI
	L	H	L	H	H	H	X	Exit Power Down --> ABI
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL <sup>6</sup>
	L	L	X	X	X	X	X	NOP (Continue power down mode)
All Banks Idle <sup>7</sup> (ABI)	H	H	X	X	X	X	X	Refer to Table 1
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	H	L	X	ILLEGAL
	H	L	L	L	L	H	X	Enter Self Refresh
	H	L	L	L	L	L	X	ILLEGAL
	L	L	X	X	X	X	X	NOP
Any State Other than Listed Above	H	H	X	X	X	X	X	Refer to Operations in Table 1
	H	L	X	X	X	X	X	Begin Clock Suspend Next Cycle
	L	H	X	X	X	X	X	Enable Clock of Next Cycle
	L	L	X	X	X	X	X	Continue Clock Suspension

\*Notes :6. If the minimum set-up time  $t_{PDE}$  is satisfied when CKE transition from “L” to “H”, CKE operates asynchronously so that a command can be input in the same internal clock cycle.

7. Power-down and self-refresh can be entered only when all the banks are in an idle state.

PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The QFP is a surface mount type package, which is very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).



**REVISION HISTORY**

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDD56V62160E-01	Feb. 4, 2002	-	-	First edition

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