Preliminary

FLASH DRIVES

2.5" Flash Drive

Connector Type

IDE ATA 44-pin

MF6128M-02BJxx
MF6256M-02BJxx
MF6512M-02BJxx
MF6640M-02BJxx
MF601G2-02BJxx

DESCRIPTION

Mitsubishi's Flash Drives provide large memory capacities on a device approximately the size of a 2.5" IDE Type Hard Disk (101.85mm(L) × 69.85mm (W) × 8.47mm (T)).

Available in 128MB, 256MB, 512MB, 640MB and 1.2GB capacities.

FEATURES

- 2.5", IDE ATA 44-pin
- Single 5V Supply
- Up to 1.2GB maximum
- Nonvolatile, No Batteries Required
- High reliability based on internal ECC function
- Fast read/write performance

  Read: 5MB/s(max.)

  Write: 128MB card = 2.0MB/s(max.)

  The others = 3.0MB/s(max.)

- Multiword DMA commands supported.
- 100,000 program/erase cycles

APPLICATIONS

- Computers
- Data Communication
- Office Automation
- Industrial
- Consumer

PRODUCT LIST

	Memory capacity (Bytes)	Data Bus width(bits)	Memory	Cylinder	Head	Sector	Out line
MF6128M-02AJxx	128,057,344	8/16	256Mbit Flash x 4	977	8	32	2.5" IDE
MF6256M-02AJxx	257,163,264		256Mbit Flash x 8	981	16	32	
MF6512M-02AJxx	515,579,904		256Mbit Flash x 16	999	16	63	
MF6640M-02AJxx	640,475,136		256Mbit Flash x 20	1241	16	63	
MF601G2-02AJxx	1,219,534,848		256Mbit Flash x 40	2363	16	63	

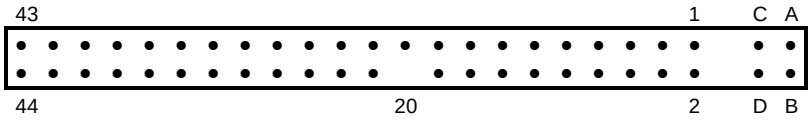
PIN ASSIGNMENT

Pin	Signal	I/O	Pin	Signal	I/O
1	RESET#	I	2	GND	-
3	DD7	I/O	4	DD8	I/O
5	DD6	I/O	6	DD9	I/O
7	DD5	I/O	8	DD10	I/O
9	DD4	I/O	10	DD11	I/O
11	DD3	I/O	12	DD12	I/O
13	DD2	I/O	14	DD13	I/O
15	DD1	I/O	16	DD14	I/O
17	DD0	I/O	18	DD15	I/O
19	GND	-	20	(keypin)	-
21	DMARQ	O	22	GND	-
23	DIOW#	I	24	GND	-
25	RIOR#	I	26	GND	-
27	IORDY	O	28	CSEL	I
29	DMACK#	I	30	GND	-
31	INTRQ	O	32	IOCS16#	O
33	DA1	I	34	PDIAG#	I/O
35	DA0	I	36	DA2	I
37	CS0#	I	38	CS1#	I
39	DASP#	I/O	40	GND	-
41	V_{DD}	-	42	V_{DD}	-
43	GND	-	44	GND	-

Master/Slave/Cable Select Configuration

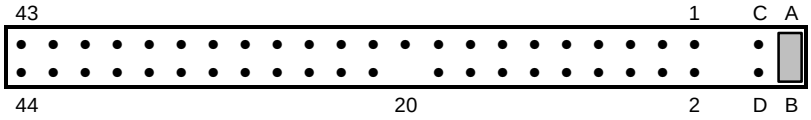
(1) Master(or single) [Default]

If all of pins A, B, C, D are Open, the drive is a Master.



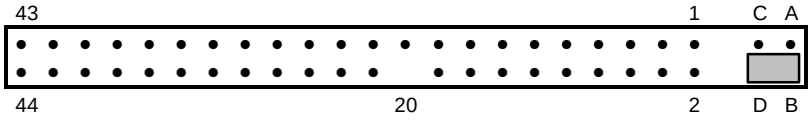
(2) Slave

If pins C, D are open and jumper position A-B is used, the drive is a Slave.



(3) Cable Select [Default]

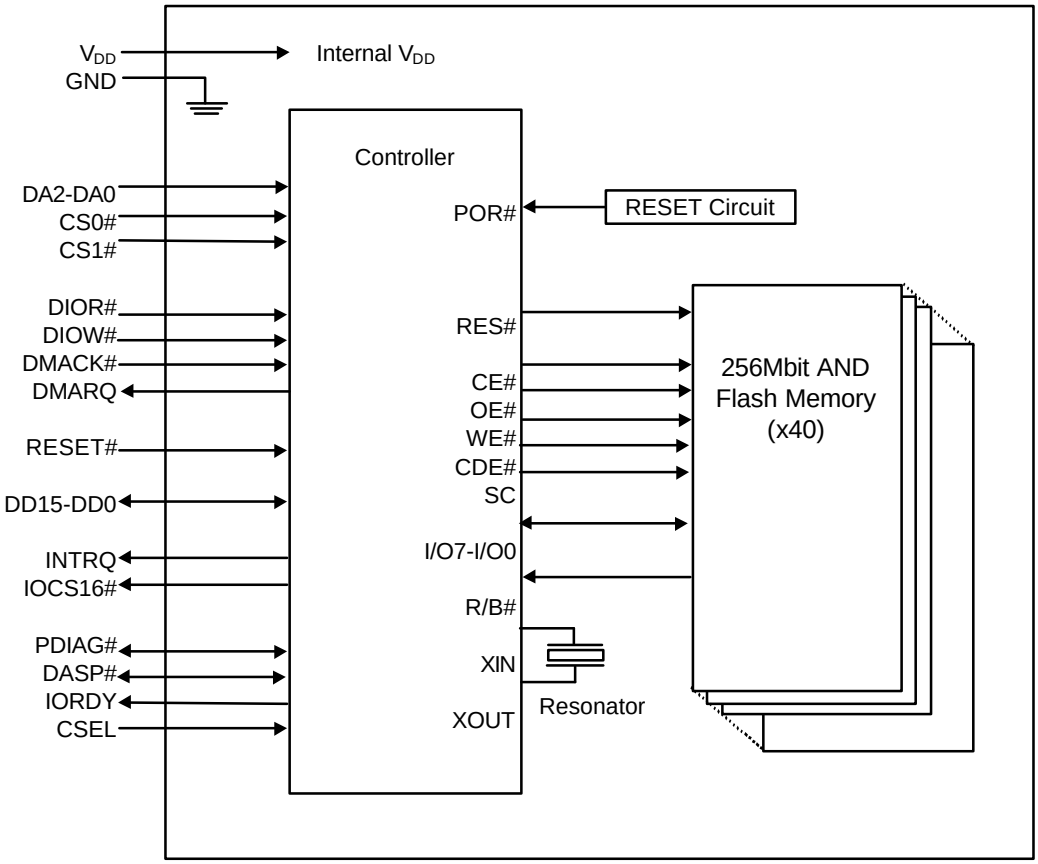
If jumper position D-B is used and pins C, A is open, Master/Slave setting is determined by the condition of CSEL signal from the host.



Signal Description

Signal Name	I/O	Pin No.	Description
Address bus[DA2-DA0]	I	36, 33, 35	Signals DA2-DA0 are address bus. DA2 is the MSB and DA0 is the LSB.
Data bus[D15-D0]	I/O	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Signals DD15-DD0 are data bus.
Chip select[CS0#, CS1#]	I	37, 38	CS0# is used to select the Command Block Registers. CS1# is used to select the Control Block Registers.
Drive I/O read[DIOR#]	I	25	DIOR# is used to read data from the Drive's I/O space.
Drive I/O write[DIOW#]	I	23	DIOW# is used to write data to the Drive's I/O space.
DMA acknowledge[DMACK#]	I	29	This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available.
DMA request[DMARQ]	O	21	This signal, used for DMA data transfer between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host.
Drive interrupt[INTRQ]	O	31	This signal is active high interrupt request to the host.
Drive 16-bit I/O[IOCS16#]	O	32	This output signal is asserted when the I/O port address is capable of 16-bit access.
Drive active/drive1 present[DASP#]	I/O	39	This signal is the DISK Active/Slave Present signal in the Master/Slave handshake protocol.
Drive reset[RESET#]	I	1	This input pin is the active low hardware reset from the host.
I/O channel ready[IORDY]	O	27	This signal is asserted to delay completion of the memory or I/O access cycle.
Passed diagnostics[PDIAG#]	I/O	34	This signal is the Pass Diagnostic signal in the Master/Slave handshake protocol.
Cable select[CSEL]	I	28	This signal is used to configure this Drive as a Master or a Slave. When this signal is grounded, this Drive is configured as a Master. When this signal is Open, this Drive is configure as a Slave.
V_{DD}	-	41, 42	5V power.
GND	-	2, 19, 22, 24, 26, 30, 40, 43, 44	Ground.

BLOCK DIAGRAM



IDE ATA Interface

CS1#	CS0#	DA2-DA0	Register	
			DIOR#="L"	DIOW#="L"
1	0	0h	Data Register(DD15-DD0)	Data Register(DD15-DD0)
1	0	1h	Error Register(DD7-DD0)	Feature Register(DD7-DD0)
1	0	2h	Sector Count Register(DD7-DD0)	Sector Count Register(DD7-DD0)
1	0	3h	Sector Number Register(DD7-DD0)	Sector Number Register(DD7-DD0)
1	0	4h	Cylinder Low Register(DD7-DD0)	Cylinder Low Register(DD7-DD0)
1	0	5h	Cylinder High Register(DD7-DD0)	Cylinder High Register(DD7-DD0)
1	0	6h	Drive Head Register(DD7-DD0)	Drive Head Register(DD7-DD0)
1	0	7h	Status Register(DD7-DD0)	Command Register(DD7-DD0)
0	1	6h	Alt. Status Register(DD7-DD0)	Device Control Register(DD7-DD0)
0	1	7h	Drive Address Register(DD7-DD0)	invalid

ATA Register Specifications

Data Register

This register is a 16 bit register which is used to transfer data blocks between the card data buffer and the host. Data may be transferred by either a series of word accesses to the Data register or a series of byte accesses to the Data register.

DD15	DD14	DD13	DD12	DD11	DD10	DD9	DD8
Data Word							
Odd Data Byte							

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Data Word							
Data Byte							

Error Register

This register contains additional information about the source of an error which has occurred in processing of the preceding command. This register should be checked by the host when ERR bit in the Status register is set. The Error register is a read only register.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
BBK	UNC	0	IDNF	0	ABRT	0	AMNF

Field	function
BBK	This bit is set when a Bad Block is detected in requested ID field. Host can not read/write on data area that is marked as a Bad Block.
UNC	This bit is set when Uncorrectable error is occurred at reading the card.
IDNF	The requested sector ID is in error or cannot be found.
ABRT	This bit is set if the command has been aborted because of the card status condition. (Not ready, Write fault, etc.) or when an invalid command has been issued.
AMNF	This bit is set in case of a general error.

Feature Register

This register is written by the host to provide command specific information to the drive regarding features of the drive which the host wish to utilize. The Feature register is a write only register.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Feature byte							

Sector Count Register

This register is written by the host with the number of sectors or blocks to be processed in the subsequent command. After the command is complete, the host may read this register to obtain the count of sectors left unprocessed by the command.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Sector Count							

Sector Number Register

This register is written by the host with the starting sector number to be used in the subsequent Cylinder-Head-Sector command. After the command is complete, the host may read the final sector number from this register. When logical block addressing is used, this register is written by the host with bit7 to 0 of the starting logical block number and contains bit7 to 0 of the final logical block number after the command is complete.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Sector Number							
Logical Block Number bits A07-A00(LBA Addressing)							

Cylinder Low Register

This register is written by the host with the low-order byte of the starting cylinder address to be used in the subsequent Cylinder-Head-Sector command. After the command is complete, the host may read the low-order byte of the final cylinder number from this register. When logical block addressing is used, this register is written by the host with bits15 to 8 of the starting logical block number and contains bits15 to 8 of the final logical block number after the command complete.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Cylinder Low Byte							
Logical Block Number bits A15-A08(LBA Addressing)							

Cylinder High Register

This register is written by the host with the high-order byte of the starting cylinder address to be used in the subsequent Cylinder-Head-Sector command. After the command is complete, the host may read the high-order byte of the final cylinder number from this register. When logical block addressing is used, this register is written by the host with bits 23 to 16 of the starting logical block number and contains bits23 to 16 of the final logical block number after the command is complete.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Cylinder High Byte							
Logical Block Number bits A23-A16(LBA Addressing)							

Drive/Head Register

The Drive/Head register is used to specify the selected drive of a pair of drives sharing a set of registers.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
X	LBA	X	DRV	HS3	HS2	HS1	HS0
				LBA27	LBA26	LBA25	LBA24

Field	function
X	Undefined . “0” or “1”.
LBA	This bit is “0” for CHS addressing and “1” for Logical Block addressing.
DRV	This bit is number of the drive which the host has selected. When DRV is cleared, Drive0 is selected. When DRV is set, Drive1 is selected. The card is selected to be Drive0 or to be Drive1 using the “Copy” field of the PC Card Socket Copy Register.
HS3-0 LBA27-24	HS3-0 of the head number in CHS addressing or LBA27-24 of the Logical Block Number in LBA addressing.

Status and Alternate Status Registers

The Status register and the Alternate Status register return the card status when read by the host. Reading the Status register clears a pending interrupt request while reading the Alternate Status register does not. The Status register and the Alternate Status register are read only registers.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

Field	function
BSY	This bit is set when the card internal operation is executing. When this bit is set to “1”, other bits in this register are invalid.
DRDY	DRDY indicates whether the card is capable of performing card operations.
DWF	This bit, if set, indicates a write fault has occurred.
DSC	This bit is set when the drive seek complete.
DRQ	This bit is set when the information can be transferred between the host and Data register.
CORR	This bit is set when a correctable data error has been occurred and the data has been corrected.
IDX	This bit is always set to “0”.
ERR	This bit is set when the previous command has ended in some type of error. The error information is set in the other Status register bits or Error register. This bit is cleared by the next command.

Command Register

The Command register contains the command code being sent to the device. Command execution begins immediately after this register is written. The Command register is a write only register.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
Command							

Device Control Register

This register is used to control the card interrupt request and to issue a soft reset to the card. The Device Control register is a write only register.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
X	X	X	X	1	SRST	nIEN	0

Field	function
X	don’t care.
1	This bit is set to “1”.
SRST	This bit is set to “1” in order to force the card to perform a Command Block Reset operation. This does not change the Card Configuration registers as a Hardware Reset does. The card remains in Reset until this bit is reset to “0”.
nIEN	This bit is used for enabling IREQ#. When this bit is set to “0”, IREQ# is enabled. When this bit is set to “1”, IREQ# is disabled.
0	This bit is set to “0”.

Drive Address Register

This register is provided for compatibility with the AT disk drive interface.

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
X	nWTG	nHS3-0				nDS1	nDS0

Field	function
X	This bit is unknown.
nWTG	This bit is set to “0” when a Flash write operation is in progress, otherwise it is set to “1”.
nHS3-0	These bits is the negative value of Head Select bits in Drive/Head register.
nDS1	This bit is set to “0” when Slave drive is active and selected.
nDS0	This bit is set to “0” when Master drive is active and selected.

ATA Command Specifications

This table summarizes the ATA command set with the paragraphs. Following shows the support commands and command codes which are written in command registers.

Command	Code	FR	SC	SN	CY	DR	HD
Check Power Mode	98h, E5h					y	
Execute Drive Diagnostic	90h					y	
Erase Sector(s)	C0h		y	y	y	y	y
Format Track	50h		y		y	y	y
Identify Drive	ECh					y	
Idle	97h, E3h		y			y	
Idle Immediate	95h, E1h					y	
Initialize Drive Parameters	91h		y			y	y
Read Buffer	E4h					y	
Read DMA	C8h,C9h		y	y	y	y	y
Read Long Sector	22h, 23h			y	y	y	y
Read Multiple	C4h		y	y	y	y	y
Read Sector(s)	20h, 21h		y	y	y	y	y
Read Verify Sector(s)	40h, 41h		y	y	y	y	y
Recalibrate	1xh					y	
Request Sense	03h					y	
Seek	7xh			y	y	y	y
Set Features	EFh	y	y			y	
Set Multiple mode	C6h		y			y	
Set Sleep Mode	99h, E6h					y	
Standby	96h, E2h					y	
Standby Immediate	94h, E0h					y	
Translate Sector	87h		y	y	y	y	y
Wear Level	F5h					y	
Write Buffer	E8h					y	
Write DMA	CAh,CBh		y	y	y	y	y
Write Long Sector	32h, 33h			y	y	y	y
Write Multiple	C5h		y	y	y	y	y
Write Multiple without Erase	CDh		y	y	y	y	y
Write Sector(s)	30h, 31h		y	y	y	y	y
Write Sector without Erase	38h		y	y	y	y	y
Write Verify	3Ch		y	y	y	y	y

FR : Feature Register, SC : Sector Count Register,
SN : Sector Number Register, CY : Cylinder Low/High Register,
DR Drive bit of Drive/Head Register, HD : Head No. of Drive/Head Register,

Check Power Mode(98h, E5h)
This command checks the power mode.

Execute Drive Diagnostic(90h)
This command performs the internal diagnostic tests implemented by the card.

Erase Sector(s)(C0h)
This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command.

Format Track(50h)
This command writes the desired head and cylinder of the selected drive with a FFh pattern.

Identify Drive(ECh)
This command enables the host to receive parameter information from the card. (Refer to the Identify Drive Information table.)

Idle(97h, E3h)
This command causes the card to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled.

Idle Immediate(95h, E1h)
This command causes the card to set BSY, enter the idle mode, clear BSY and generate an interrupt.

Initialize Drive Parameters(91h)
This command allows the host to alter the number of sectors per track and the number of heads per cylinder.

Read Buffer(E4h)
This command enables the host to read the current contents of the card's sector buffer.

Read DMA(C8h,C9h)
This command enables the host to read the sector data by the Multiword DMA protocol.

Read Long Sector(22h, 23h)
This command is similar to the Read Sector(s) command except the contents of the Sector Count register are ignored and only one sector is read. The 512 data bytes and 4 ECC bytes are read into the buffer(with no ECC correction) and then transferred to the host.

Read Multiple(C4h)
This command performs similarly to the Read Sector(s) command. Interrupt are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Read Sector(s)(20h, 21h)
This command transfers data from the card to the host. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers, and proceeds for the number of sectors specified in the Sector Count register.

Read Verify Sector(s)(40h, 41h)
This command is identical to the Read Sector(s) command, except that DRQ is not asserted, and no data is transferred to the host.

Recalibrate(1xh)
Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Request Sense(03h)
This command requests extended error information for the previous command.

Seek(7xh)
This command is supported for backward compatibility. Although this command has no actual function, it does perform a range check of valid track, and posts an IDNF error if the Head or Cylinder specified are out of bounds.

Set Features(EFh)
This command is used by the host to establish or select certain features.

Set Multiple Mode(C6h)
This command enables the card to perform Read and Write Multiple operations and establishes the block count for these commands. This card supports 1 sector block size.

Set Sleep Mode(99h, E6h)
This command causes the card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

Standby(96h, E2h)
This command causes the card to set BSY, enter the Standby mode, clear BSY and generate an interrupt.

Standby Immediate(94h, E0h)
This command causes the card to set BSY, enter the Standby mode, clear BSY and generate an interrupt.

Translate Sector(87h)
This command allows the host to know the number of times an user sector has been erased and programmed. This card doesn't support the Hot Count value.

Wear Leveling(F5h)
Although this command is supported for backward compatibility, it has no actual function. The card will always return good status at the completion of this command.

Write Buffer(E8h)
This command enables the host to overwrite contents of the card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfers 512 bytes.

Write DMA(CAh, CBh)
This command enables the host to write sector data by the Multiword DMA protocol.

Write Long Sector(32h, 33h)
This command is similar to the Write Sector(s) except the contents of the Sector Count register are ignored and only one sector is written. The 512 data bytes and 4 ECC bytes are transferred from the host and then written from the buffer to the flash.

Write Multiple(C5h)
This command is similar to the Write Sector(s) command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

Write Multiple without Erase(CDh)
This command is similar to the Write Multiple command. The sectors should be pre-erased with the Erase Sector command before this command is issued. If the sector is not pre-erased, Write Multiple command operation will occur.

Write Sector(s)(30h, 31h)
This command transfers data from the host to the card. Data transfer starts at the sector specified by the Cylinder, Head, and Sector Number registers, and proceeds for the number of sectors specified in the Sector Count register.

Write Sector without Erase(CDh)
This command is similar to the Write Sector(s) command. The sectors should be pre-erased with the Erase Sector command before this command is issued. If the sector is not pre-erased, Write Sector command operation will occur.

Write Verify(3Ch)
This command is similar to the Write Sector(s) command, except each sector is verified immediately after being written.

Identify Drive Information

Word Address	Data	Description		
0	848Ah	General configuration bit-significant information		
		15	1	Non-rotating disk drive
		14	0	Format speed tolerance gap not required
		13	0	Track offset option not available
		12	0	Data strobe offset option not available
		11	0	Rotational speed tolerance is < 0.5%
		10	1	Disk transfer rate > 10Mbs
		9	0	10Mbs <= Disk transfer rate > 5Mbs
		8	0	Disk transfer rate <= 5Mbs
		7	1	Removable cartridge drive
		6	0	Not a fixed drive
		5	0	Spindle motor control option not implemented
		4	0	Head switch time > 15us
		3	1	Not MFM encoded
		2	0	Not soft sectored
		1	1	Hard sectored
		0	0	Reserved
1	xxxxh	Number of Cylinders		
2	0000h	Reserved		
3	000xh	Number of Heads		
4	0000h	Number of unformatted bytes per track		
5	0200h	Number of unformatted bytes per sector		
6	0020h	Number of sectors per track		
7-8	xxxxh, xxxxh	Number of sectors per card (word 7 = MSW, word 8 = LSW)		
9	0000h	Reserved		
10-19	2020h	Reserved		
20	0001h	Buffer type: Single ported, single-sector, w/o read cache		
21	0001h	Buffer size, in 512 byte increments		
22	0004h	ECC length used on Read and Write Long command		
23-26	xxxxh	Firmware revision, 8 ASCII characters		
27-46	xxxxh	Model number, 40 ASCII characters.		
47	0001h	Maximum Block Count=1 for Read/write Multiple commands		
48	0000h	Cannot perform doubleword I/O		
49	0300h	Capabilities		
50	0000h	Reserved		
51	0200h	PIO timing cycle timing mode 2		
52	0000h	Reserved		
53	0003h	Words 54-58 are valid(bit0), words 64-70 are valid(bit1).		
54	xxxxh	Number of Current Cylinders		
55	xxxxh	Number of Current Heads		
56	xxxxh	Number of Current Sectors per Track		
57	xxxxh	LSW of the Current Capacity in Sectors		
58	xxxxh	MSW of the Current Capacity in Sectors		
59	010xh	Current Setting for Block Count for R/W Multiple commands		
60	xxxxh	LSW of the total number of user addressable LBA mode		
61	xxxxh	MSW of the total number of user addressable LBA mode		
62	0000h	Reserved		
63	0007h	Multiword DMA mode2 supported		
64	0003h	Advanced PIO modes supported		
65	0078h	Minimum Multiword DMA transfer cycle time (120ns)		
66	0078h	Manufacturer's recommended Multiword DMA transfer cycle (120ns)		
67	00F0h	Minimum PIO transfer cycle time with out flow control (240ns)		
68	0078h	Minimum PIO transfer cycle time with IORDY (120ns)		
69-255	0000h	Reserved		

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage	With respect to GND	-0.3~6.2	V
V_i	Input voltage		-0.3~V_{DD}+0.3	V
V_o	Output voltage		-0.3~V_{DD}+0.3	V
P_d	Power dissipation	T_a = 25 °C	1.2	W
T_{opr}	Operating temperature		0~60	°C
T_{stg}	Storage temperature		-10~80	°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}(5V)	V_{DD} Supply voltage	4.5	5.0	5.5	V
GND	System ground		0		V
V_{IH}	High input voltage	0.7V_{DD}		V_{DD}	V
V_{IL}	Low input voltage	0		0.8	V

DC ELECTRICAL CHARACTERISTICS (Ta=0~60°C, V_{DD}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
				4.5V		5.5V	
V_{OH}	High output voltage	I_{OH}=4mA(4.5V)	INTRQ, INPACK#, DASP#, PDIAG#	0.8V_{DD}		-	V
		I_{OH}=8mA(4.5V)	the other outputs				
V_{OL}	Low output voltage	I_{OL}=-4mA(4.5V)	INTRQ, INPACK#, DASP#, PDIAG#	-		0.4	V
		I_{OL}=-8mA(4.5V)	the other outputs				
I_{OZ}	Output current in off state	CS0# = CS1# = V_{IH}	DD15-DD0	-		±10	µA
I_{CCR}	Active supply current (Read)	Output open			70	110	mA
I_{CCW}	Active supply current (Write)				100	140	mA
I_{CCS}	Standby current (Auto power down)	CS0# = CS1# = V_{DD} DD15-DD0 = GND Other inputs = V_{DD} or GND			2.0	4.0	mA
I_{CCD}	Sleep current (Sleep command)	CS0# = CS1# = V_{DD} DD15-DD0 = GND Other inputs = V_{DD} or GND			500	800	µA

DC ELECTRICAL CHARACTERISTICS(Continued)

Symbol	Parameter	Test Condition		Limits			Unit
				Min.	Typ.	Max.	
				4.5V		5.5V	
I_{IH}	High input current	$V_{IN}=V_{DD}$		-10		+10	µA
I_{IL}	Low input current	V_{IN}=GND	CS0#, CS1#, DIOR#, DIOW#, DA2-DA0, DD15-DD0	-10		+10	µA
			RESET#, DASP#, PDIAG#	-30		-100	
			CSEL	-10		-50	

CAPACITANCE

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I=GND, Vi=25mVrms, f=1 MHz, Ta=25°C			45	pF
C_O	Output capacitance	V_O=GND, Vo=25mVrms, f=1 MHz, Ta=25°C			45	

Note : These parameters are not 100% tested.

AC ELECTRICAL CHARACTERISTICS

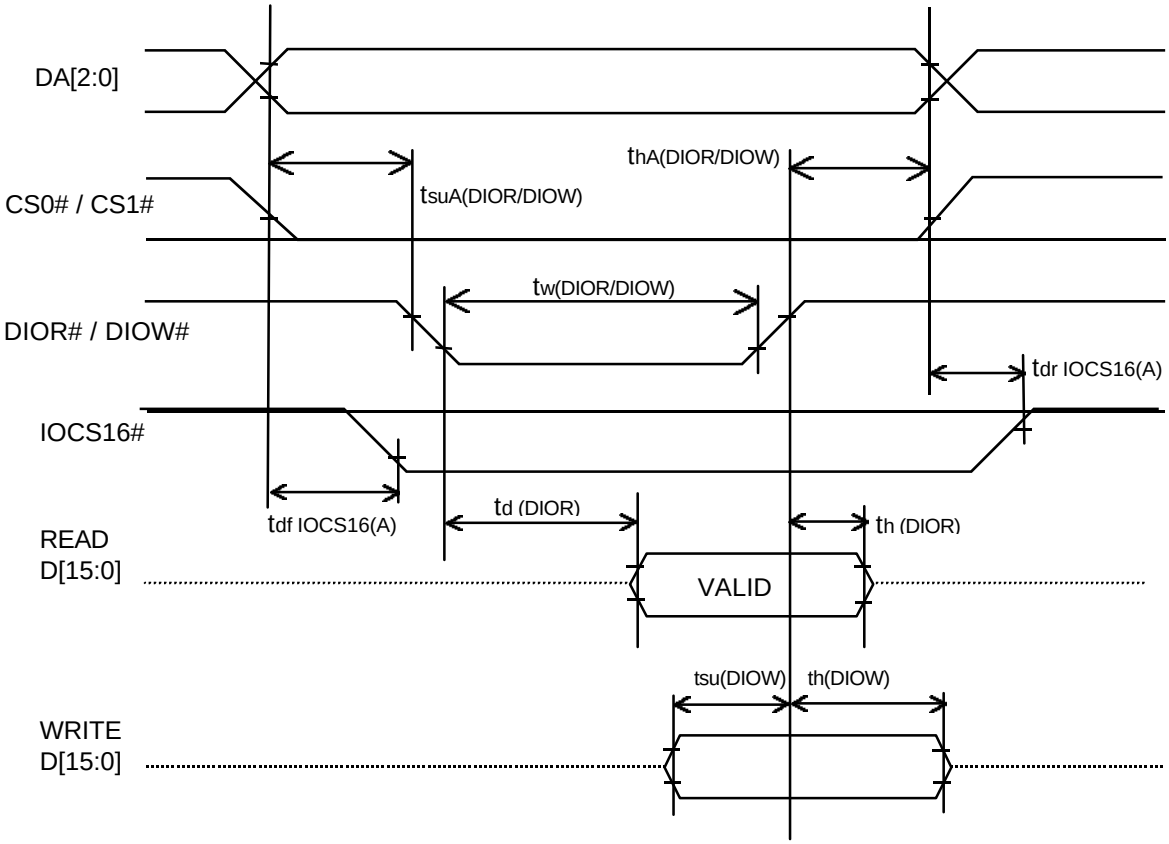
PIO READ /WRITE TIMING

Symbol	Parameter	Limit		Unit
		Min	Max	
tsuA(DIOR / DIOW)	Address Setup before **DIOR# / DIOW#** *	25		ns
thA(DIOR / DIOW)	Address Hold following **DIOR# / DIOW#** *	10		ns
tw(DIOR / DIOW)	**DIOR# / DIOW#** Width Time	70		ns
td(DIOR)	Data Delay after **DIOR#**		50	ns
th(DIOR)	Data Hold following **DIOR#**	5		ns
tsu(DIOW)	Data Setup before **DIOW#**	20		ns
th(DIOW)	Data Hold after **DIOW#**	10		ns
tdfIOCS16(A)	**IOCS16#** Delay Falling from Address *		35	ns
tdrIOCS16(A)	**IOCS16#** Delay Rising from Address *		35	ns

The maximum load on **IOCS16#** are 1 LSTTL with 50 pF total load.

* "Address" includes DA2-DA0 and CS0#, CS1#.

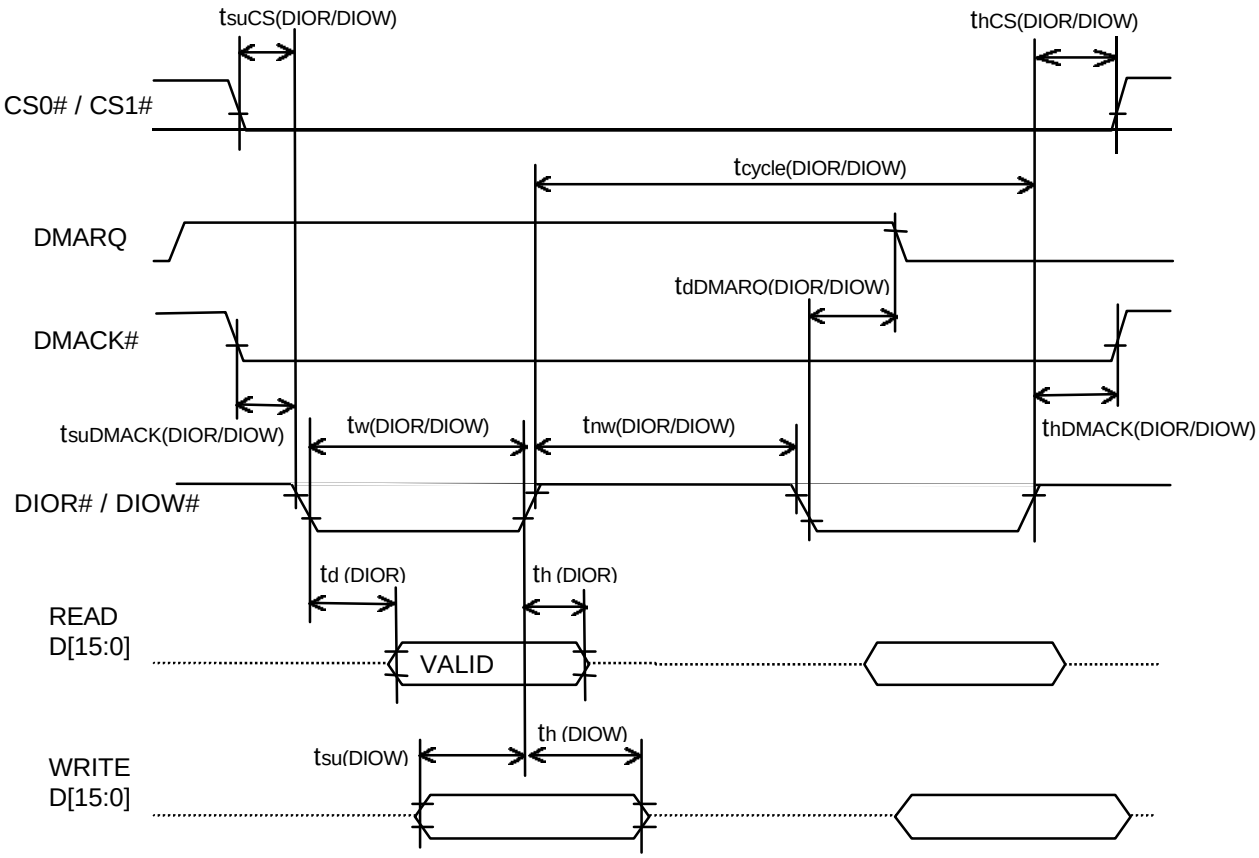
I/O READ / WRITE TIMING DIAGRAM



Multiword DMA TIMING

Symbol	Parameter	Limit		Unit
		Min	Max	
tsuCS(DIOR / DIOW)	CS0#, CS1# Setup before **DIOR# / DIOW#**	25		ns
thCS(DIOR / DIOW)	CS0#, CS1# Hold following **DIOR# / DIOW#**	10		ns
tw(DIOR / DIOW)	**DIOR# / DIOW#** Width Time	70		ns
tnw(DIOR / DIOW)	**DIOR# / DIOW#** negate pulse Width Time	35		ns
tcycle(DIOR / DIOW)	**DIOR# / DIOW#** Cycle Time	120		ns
td(DIOR)	Data Delay after **DIOR#**		50	ns
th(DIOR)	Data Hold following **DIOR#**	5		ns
tsu(DIOW)	Data Setup before **DIOW#**	20		ns
th(DIOW)	Data Hold after **DIOW#**	10		ns
tsuDMACK(DIOR / DIOW)	DMACK# Setup Time before **DIOR#** / **DIOW#**	0		ns
thDMACK(DIOR / DIOW)	DMACK# Hold Time following **DIOR#** / **DIOW#**	5		ns
tdDMARQ(DIOR / DIOW)	DMARQ negate delay time from **DIOR#** / **DIOW#**		35	ns

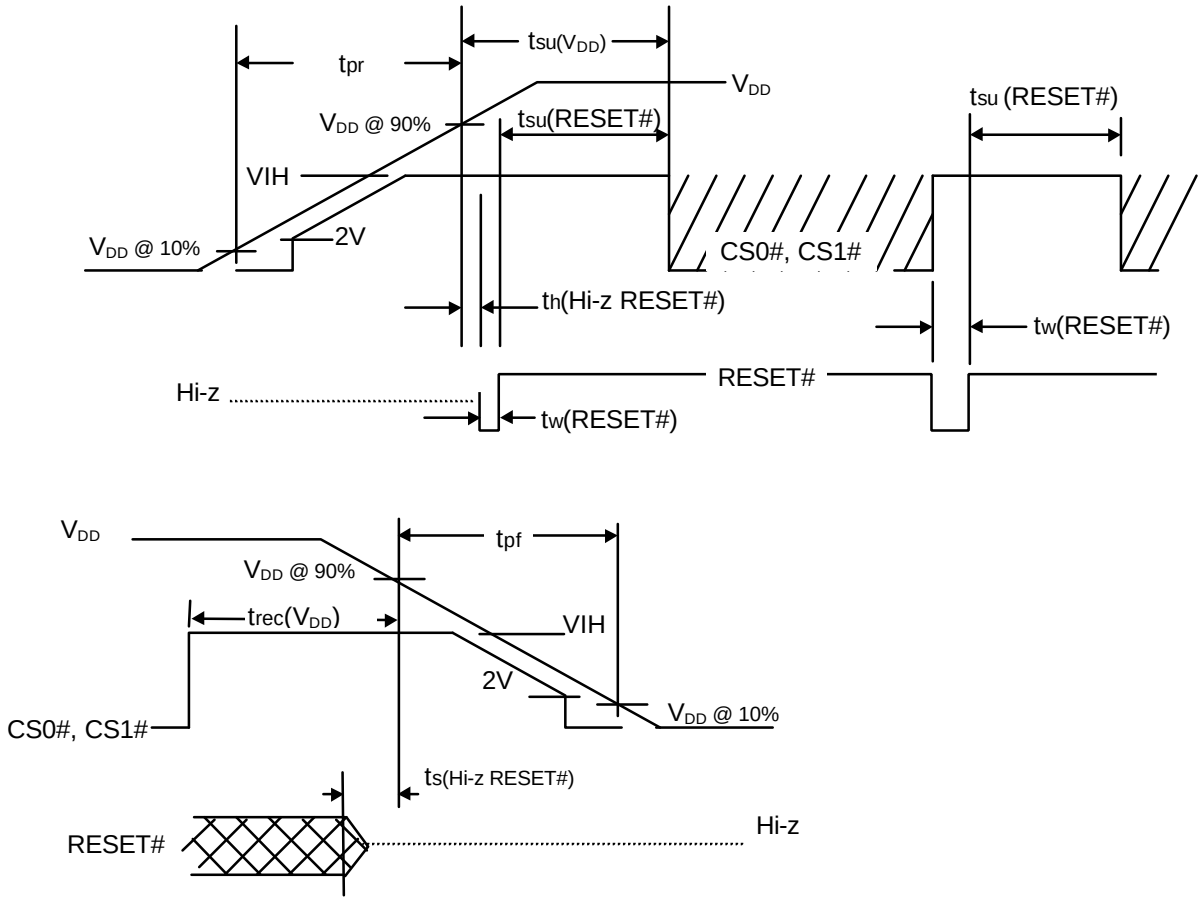
Multiword DMA TIMING DIAGRAM



RECOMMENDED POWER UP/DOWN CONDITIONS (Ta=0~60°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vi(CS)	CS input voltage	0V≤ V_{DD} <2V	0		V_{DD}	V
		2V≤ V_{DD} <V_{IH}	V_{DD}-0.1	V_{DD}	V_{DD}+0.1	V
		V_{IH} ≤ V_{DD}	V_{IH}		V_{DD}+0.1	V
tsu(V_{DD})	CS setup time		20			ms
tsu(RESET#)	RESET# setup time		20			ms
trec(V_{DD})	CS recover time		1			µs
tpr	V_{DD} rising time	10%→90% of V_{DD}	0.1		100	ms
tpf	V_{DD} falling time	90% of V_{DD}→10%	3		300	ms
tw(RESET#)	RESET# width		10			µs
th(Hi-zRESET#)			1			ms
ts(Hi-zRESET#)			0			ms

POWER UP/DOWN TIMING DIAGRAM



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