

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## DESCRIPTION

The MH2M365CXJ/CNXJ is 2097152-word x 36-bits dynamic RAM. This consists of four industry standard 1M x 16 dynamic RAMs in SOJ and two industry 1M x 4 dyanmic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module, suitable for easy interchange or addition of modules.

## FEATURES

| Type name         | RAS access time (max.ns) | CAS access time (max.ns) | Address access time (max.ns) | Cycle time (min.ns) | Power dissipation (typ.mW) |
|-------------------|--------------------------|--------------------------|------------------------------|---------------------|----------------------------|
| MH2M365CXJ/CNXJ-5 | 50                       | 13                       | 25                           | 90                  | 2137                       |
| MH2M365CXJ/CNXJ-6 | 60                       | 15                       | 30                           | 110                 | 1767                       |
| MH2M365CXJ/CNXJ-7 | 70                       | 20                       | 35                           | 130                 | 1537                       |

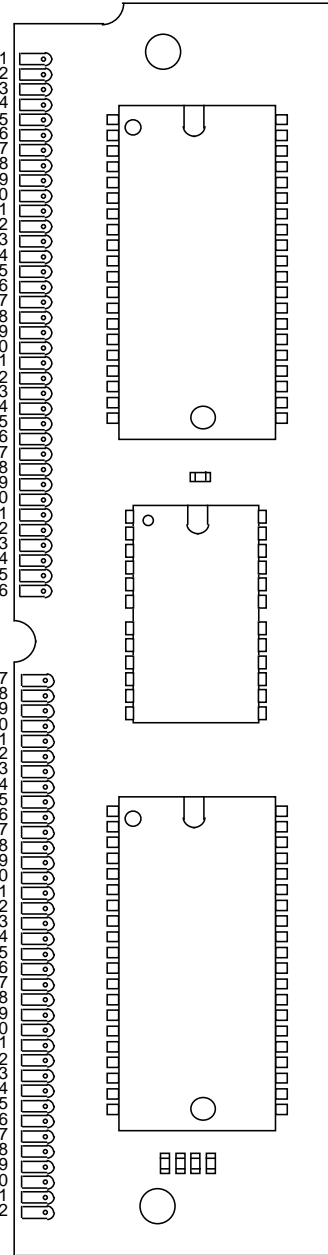
- 72pin single in-line package
- Single 5.0V ± 10% supply
- Low stand-by power dissipation  
33mW (Max) ----- CMOS Input level
- Low operating power dissipation  
MH2M365CXJ/CNXJ- 5 ----- 2.69W (Max)  
MH2M365CXJ/CNXJ- 6 ----- 2.22W (Max)  
MH2M365CXJ/CNXJ- 7 ----- 1.92W (Max)
- Hyper-page mode ,  $\overline{\text{RAS}}$ -only refresh ,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, Hidden refresh capabilities
- All inputs and output directly TTL compatible  
1024 refresh cycles every 16.4ms (A<sub>0</sub> ~ A<sub>9</sub>)

## APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

## PIN CONFIGURATION (TOP VIEW) [Double side]

|                               |                               |    |
|-------------------------------|-------------------------------|----|
| 1.Vss                         | 37.MP1                        | 1  |
| 2.DQ0                         | 38.MP3                        | 2  |
| 3.DQ16                        | 39.Vss                        | 3  |
| 4.DQ1                         | 40.CAS0                       | 4  |
| 5.DQ17                        | 41. $\overline{\text{CAS}}$ 2 | 5  |
| 6.DQ2                         | 42. $\overline{\text{CAS}}$ 3 | 6  |
| 7.DQ18                        | 43. $\overline{\text{CAS}}$ 1 | 7  |
| 8.DQ3                         | 44.RAS0                       | 8  |
| 11.NC                         | 45.RAS1                       | 9  |
| 10.Vcc                        | 46.NC                         | 10 |
| 11.NC                         | 47.W                          | 11 |
| 12.A0                         | 48.NC                         | 12 |
| 13.A1                         | 49.DQ8                        | 13 |
| 14.A2                         | 50.DQ24                       | 14 |
| 15.A3                         | 51.DQ9                        | 15 |
| 16.A4                         | 52.DQ25                       | 16 |
| 17.A5                         | 53.DQ10                       | 17 |
| 18.A6                         | 54.DQ26                       | 18 |
| 19.NC                         | 55.DQ11                       | 19 |
| 20.DQ4                        | 56.DQ27                       | 20 |
| 21.DQ20                       | 57.DQ12                       | 21 |
| 22.DQ5                        | 58.DQ28                       | 22 |
| 23.DQ21                       | 59.Vcc                        | 23 |
| 24.DQ6                        | 60.DQ29                       | 24 |
| 25.DQ22                       | 61.DQ13                       | 25 |
| 26.DQ7                        | 62.DQ30                       | 26 |
| 27.DQ23                       | 63.DQ14                       | 27 |
| 28.A7                         | 64.DQ31                       | 28 |
| 29.NC                         | 65.DQ15                       | 29 |
| 30.Vcc                        | 66.NC                         | 30 |
| 31.A8                         | 67.PD1                        | 31 |
| 32.A9                         | 68.PD2                        | 32 |
| 33. $\overline{\text{RAS}}$ 3 | 69.PD3                        | 33 |
| 34. $\overline{\text{RAS}}$ 2 | 70.PD4                        | 34 |
| 35.MP2                        | 71.NC                         | 35 |
| 36.MP0                        | 72.Vss                        | 36 |



Outline 72N9J-C

|     |     |     |     |
|-----|-----|-----|-----|
|     | - 5 | - 6 | - 7 |
| PD1 | NC  | NC  | NC  |
| PD2 | NC  | NC  | NC  |
| PD3 | Vss | NC  | Vss |
| PD4 | Vss | NC  | NC  |

NC: NO CONNECTION

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## FUNCTION

in addition to normal read, write, a number of other functions, e.g., hyper page mode, RAS only refresh,

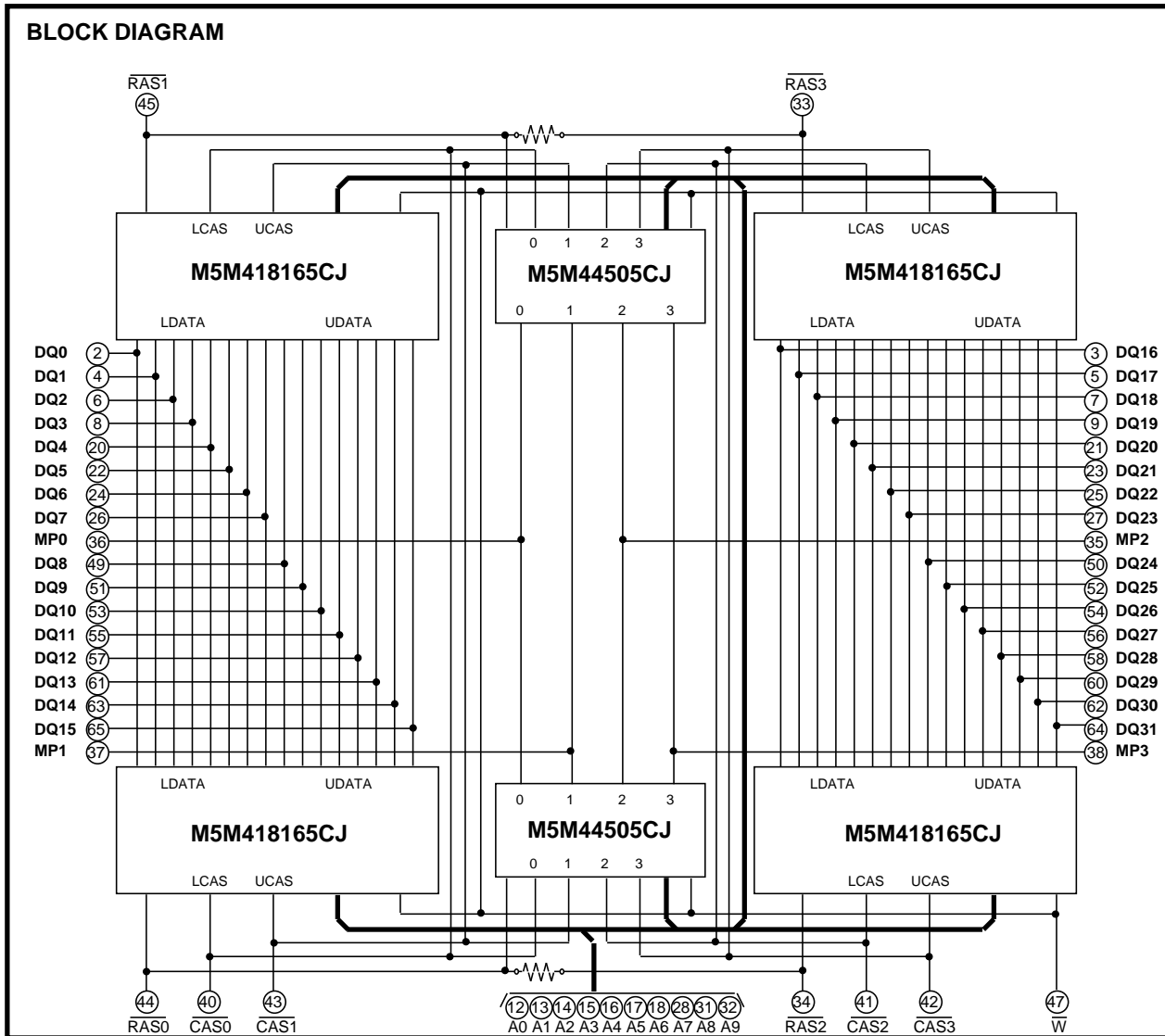
The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

| Operation              | Inputs |     |     |             |                | Input/Output |        |
|------------------------|--------|-----|-----|-------------|----------------|--------------|--------|
|                        | RAS    | CAS | W   | Row address | Column address | Input        | Output |
| Read                   | ACT    | ACT | NAC | APD         | APD            | OPN          | VLD    |
| Early write            | ACT    | ACT | ACT | APD         | APD            | VLD          | OPN    |
| RAS-only refresh       | ACT    | NAC | DNC | APD         | DNC            | DNC          | OPN    |
| Hidden refresh         | ACT    | ACT | NAC | APD         | DNC            | OPN          | VLD    |
| CAS before RAS refresh | ACT    | ACT | DNC | DNC         | DNC            | DNC          | OPN    |
| Standby                | NAC    | DNC | DNC | DNC         | DNC            | DNC          | OPN    |

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

## BLOCK DIAGRAM



## MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## ABSOLUTE MAXIMUM RATINGS

| Symbol           | Parameter             | Conditions                      | Ratings   | Unit |
|------------------|-----------------------|---------------------------------|-----------|------|
| V <sub>cc</sub>  | Supply voltage        | With respect to V <sub>ss</sub> | -1 ~ 7    | V    |
| V <sub>I</sub>   | Input voltage         |                                 | -1 ~ 7    | V    |
| V <sub>O</sub>   | Output voltage        |                                 | -1 ~ 7    | V    |
| I <sub>O</sub>   | Output current        |                                 | 50        | mA   |
| P <sub>d</sub>   | Power dissipation     | T <sub>a</sub> =25°C            | 6000      | mW   |
| T <sub>opr</sub> | Operating temperature |                                 | 0 ~ 70    | °C   |
| T <sub>stg</sub> | Storage temperature   |                                 | -40 ~ 125 | °C   |

RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub>=0 ~ 70 °C, unless otherwise noted) (Note 1)

| Symbol          | Parameter                            | Limits |     |     | Unit |
|-----------------|--------------------------------------|--------|-----|-----|------|
|                 |                                      | Min    | Nom | Max |      |
| V <sub>cc</sub> | Supply voltage                       | 4.5    | 5.0 | 5.5 | V    |
| V <sub>ss</sub> | Supply voltage                       | 0      | 0   | 0   | V    |
| V <sub>IH</sub> | High-level input voltage, all inputs | 2.4    |     | 6.0 | V    |
| V <sub>IL</sub> | Low-level input voltage, all inputs  | -1     |     | 0.8 | V    |

Note 1 : All voltage values are with respect to V<sub>ss</sub>ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>cc</sub>=5.0V ± 10%, V<sub>ss</sub>=0V, unless otherwise noted) (Note 2)

| Symbol                | Parameter   | Test conditions   | Limits   |     |                 | Unit |
|-----------------------|---|---|--|-----|-----------------|------|
|                       |   |   | Min  | Typ | Max             |      |
| V <sub>OH</sub>       | High-level output voltage   | I <sub>OH</sub> =-5.0mA   | 2.4  |     | V <sub>cc</sub> | V    |
| V <sub>OL</sub>       | Low-level output voltage  | I <sub>OL</sub> =4.2mA  | 0  |     | 0.4             | V    |
| I <sub>OZ</sub>       | Off-state output current  | Q floating 0V V <sub>OUT</sub> 5.5V                             | -20  |     | 20              | μA   |
| I <sub>I</sub>        | Input current   | 0V V <sub>IN</sub> 6 V, Other inputs pins=0V                    | -60  |     | 60              | μA   |
| I <sub>CC1</sub> (AV) | Average supply current from V <sub>cc</sub> operating<br>(Note 3,4,5)                                       | MH2M365C -5   | R <sub>AS</sub> , C <sub>AS</sub> cycling<br>t <sub>RC</sub> =t <sub>WC</sub> =min.<br>output open |     | 491             | mA   |
|                       |   | MH2M365C -6   |  |     | 406             |      |
|                       |   | MH2M365C -7   |  |     | 351             |      |
| I <sub>CC2</sub>      | Supply current from V <sub>cc</sub> , stand-by (Note 6)   | R <sub>AS</sub> =C <sub>AS</sub> =V <sub>IH</sub> , output open |  |     | 12              | mA   |
|                       |   | R <sub>AS</sub> =C <sub>AS</sub> V <sub>cc</sub> -0.2 V         |  |     | 6               |      |
| I <sub>CC3</sub> (AV) | Average supply current from V <sub>cc</sub> refreshing<br>(Note 3,5)  | MH2M365C -5   | R <sub>AS</sub> cycling, C <sub>AS</sub> =V <sub>IH</sub><br>t <sub>RC</sub> =min.<br>output open  |     | 491             | mA   |
|                       |   | MH2M365C -6   |  |     | 406             |      |
|                       |   | MH2M365C -7   |  |     | 351             |      |
| I <sub>CC4</sub> (AV) | Average supply current from V <sub>cc</sub> Hyper-Page-Mode<br>(Note 3,4,5)                                 | MH2M365C -5   | R <sub>AS</sub> =V <sub>IL</sub> , C <sub>AS</sub> cycling<br>t <sub>RC</sub> =min.<br>output open |     | 461             | mA   |
|                       |   | MH2M365C -6   |  |     | 366             |      |
|                       |   | MH2M365C -7   |  |     | 311             |      |
| I <sub>CC6</sub> (AV) | Average supply current from V <sub>cc</sub> C <sub>AS</sub> before R <sub>AS</sub> refresh mode<br>(Note 3) | MH2M365C -5   | C <sub>AS</sub> before R <sub>AS</sub> refresh cycling<br>t <sub>RC</sub> =min.<br>output open     |     | 471             | mA   |
|                       |   | MH2M365C -6   |  |     | 391             |      |
|                       |   | MH2M365C -7   |  |     | 341             |      |

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>CC1</sub> (AV), I<sub>CC3</sub> (AV) and I<sub>CC4</sub> (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.4: I<sub>CC1</sub> (AV) and I<sub>CC4</sub> (AV) are dependent on output loading. Specified values are obtained with the output open.5: Column Address can be changed once or less while R<sub>AS</sub>=V<sub>IL</sub> and C<sub>AS</sub>=V<sub>IH</sub>.

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted)

| Symbol              | Parameter                              | Test conditions  | Limits |     |     | Unit |
|---------------------|--|--|--------|-----|-----|------|
|                     |  |  | Min    | Typ | Max |      |
| C <sub>i(A)</sub>   | Input capacitance, address inputs      | V <sub>i</sub> =V <sub>ss</sub><br>f=1MHz<br>V <sub>i</sub> =25mVrms |        |     | 45  | pF   |
| C <sub>i(W)</sub>   | Input capacitance, write control input |  |        |     | 57  | pF   |
| C <sub>i(RAS)</sub> | Input capacitance, RAS input           |  |        |     | 36  | pF   |
| C <sub>i(CAS)</sub> | Input capacitance, CAS input           |  |        |     | 43  | pF   |
| C <sub>i/O</sub>    | Input/Output capacitance, data ports   |  |        |     | 29  | pF   |

## SWITCHING CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted, see notes 6,14,15)

| Symbol           | Parameter                                       | Limits      |     |             |     |             |     | Unit |
|------------------|---|-------------|-----|-------------|-----|-------------|-----|------|
|                  |   | MH2M365C -5 |     | MH2M365C -6 |     | MH2M365C -7 |     |      |
|                  |   | Min         | Max | Min         | Max | Min         | Max |      |
| t <sub>CAC</sub> | Access time from CAS (Note 7,8)                 |             | 13  |             | 15  |             | 20  | ns   |
| t <sub>RAC</sub> | Access time from RAS (Note 7,9)                 |             | 50  |             | 60  |             | 70  | ns   |
| t <sub>AA</sub>  | Column address access time (Note 7,10)          |             | 25  |             | 30  |             | 35  | ns   |
| t <sub>CPA</sub> | Access time from CAS precharge (Note 7,11)      |             | 30  |             | 35  |             | 40  | ns   |
| t <sub>OHc</sub> | Output hold time from CAS                       | 5           |     | 5           |     | 5           |     | ns   |
| t <sub>OHr</sub> | Output hold time from RAS (Note 13)             | 5           |     | 5           |     | 5           |     | ns   |
| t <sub>CLZ</sub> | Output low impedance time from CAS low (Note 7) | 5           |     | 5           |     | 5           |     | ns   |
| t <sub>WEZ</sub> | Output disable time after WE high (Note 12)     |             | 13  |             | 15  |             | 20  | ns   |
| t <sub>OFF</sub> | Output disable time after CAS high (Note 12,13) |             | 13  |             | 15  |             | 20  | ns   |
| t <sub>REZ</sub> | Output disable time after RAS high (Note 12,13) |             | 13  |             | 15  |             | 20  | ns   |

Note 6: An initial pause of 500µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 16.4 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V<sub>OH</sub>=2.4V(I<sub>OH</sub>=-5mA) / V<sub>OL</sub>=0.4V(I<sub>OL</sub>=-4.2mA) load 100pF.

The reference levels for measuring of output signal are 2.0V(V<sub>OH</sub>) and 0.8V(V<sub>OL</sub>).

8: Assumes that t<sub>RCd</sub> t<sub>RCd(max)</sub> and t<sub>ASC</sub> t<sub>ASC(max)</sub> and t<sub>CP</sub> t<sub>CP(max)</sub>.

9: Assumes that t<sub>RCd</sub> t<sub>RCd(max)</sub> and t<sub>RAD</sub> t<sub>RAD(max)</sub>. If t<sub>RCd</sub> or t<sub>RAD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by amount that t<sub>RCd</sub> exceeds the value shown.

10: Assumes that t<sub>RAD</sub> t<sub>RAD(max)</sub> and t<sub>ASC</sub> t<sub>ASC(max)</sub>.

11: Assumes that t<sub>CP</sub> t<sub>CP(max)</sub> and t<sub>ASC</sub> t<sub>ASC(max)</sub>.

12: t<sub>WEZ(max)</sub>, t<sub>OFF(max)</sub> and t<sub>REZ(max)</sub> defines the time at which the output achieves the high impedance state ( I<sub>out</sub> I ± 10 µA ) and is not reference to V<sub>OH(min)</sub> or V<sub>OL(max)</sub>.

13: Output is disabled after both RAS and CAS go to high.

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## TIMING REQUIREMENTS (For Read, Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted See notes 14,15)

| Symbol | Parameter   | Limits      |      |             |      |             |      | Unit |
|--------|---|-------------|------|-------------|------|-------------|------|------|
|        |   | MH2M365C -5 |      | MH2M365C -6 |      | MH2M365C -7 |      |      |
|        |   | Min         | Max  | Min         | Max  | Min         | Max  |      |
| tREF   | Refresh cycle time                                |             | 16.4 |             | 16.4 |             | 16.4 | ms   |
| tRP    | RAS high pulse width                              | 30          |      | 40          |      | 50          |      | ns   |
| tRCD   | Delay time, RAS low to CAS low (Note16)           | 18          | 37   | 20          | 45   | 20          | 50   | ns   |
| tCRP   | Delay time, CAS high to RAS low                   | 5           |      | 5           |      | 5           |      | ns   |
| tRPC   | Delay time, RAS high to CAS low                   | 0           |      | 0           |      | 0           |      | ns   |
| tCPN   | CAS high pulse width                              | 8           |      | 10          |      | 10          |      | ns   |
| tRAD   | Column address delay time from RAS low (Note17)   | 13          | 25   | 15          | 30   | 15          | 35   | ns   |
| tASR   | Row address setup time before RAS low             | 0           |      | 0           |      | 0           |      | ns   |
| tASC   | Column address setup time before CAS low (Note18) | 0           | 10   | 0           | 13   | 0           | 13   | ns   |
| tRAH   | Row address hold time after RAS low               | 8           |      | 10          |      | 10          |      | ns   |
| tCAH   | Column address hold time after CAS low            | 8           |      | 10          |      | 10          |      | ns   |
| tDZC   | Delay time, data to CAS low (Note19)              | 0           |      | 0           |      | 0           |      | ns   |
| tRDD   | Delay time, RAS high to data (Note20)             | 13          |      | 15          |      | 20          |      | ns   |
| tCDD   | Delay time, CAS high to data (Note20)             | 13          |      | 15          |      | 20          |      | ns   |
| tT     | Transition time (Note21)                          | 1           | 50   | 1           | 50   | 1           | 50   | ns   |

Note 14: The timing requirements are assumed  $t_r = 3ns$ .

15:  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals.

16:  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is less than  $t_{RCD(max)}$ , access time is  $t_{RAC}$ . If  $t_{RCD}$  is greater than  $t_{RCD(max)}$ , access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .

17:  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD}$ ,  $t_{RAD(max)}$  and  $t_{ASC}$ ,  $t_{ASC(max)}$ , access time is controlled exclusively by  $t_{AA}$ .

18:  $t_{ASC(max)}$  is specified as a reference point only. If  $t_{RCD}$ ,  $t_{RCD(max)}$  and  $t_{ASC}$ ,  $t_{ASC(max)}$ , access time is controlled exclusively by  $t_{CAC}$ .

19:  $t_{DZC}$  must be satisfied.

20: Either  $t_{RDD}$  or  $t_{CDD}$  must be satisfied.

21:  $t_r$  is measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ .

## Read and Refresh Cycles

| Symbol | Parameter                               | Limits      |       |             |       |             |       | Unit |
|--------|---|-------------|-------|-------------|-------|-------------|-------|------|
|        |   | MH2M365C -5 |       | MH2M365C -6 |       | MH2M365C -7 |       |      |
|        |   | Min         | Max   | Min         | Max   | Min         | Max   |      |
| tRC    | Read cycle time                         | 90          |       | 110         |       | 130         |       | ns   |
| tRAS   | RAS low pulse width                     | 50          | 10000 | 60          | 10000 | 70          | 10000 | ns   |
| tCAS   | CAS low pulse width                     | 8           | 10000 | 10          | 10000 | 13          | 10000 | ns   |
| tCSH   | CAS hold time after RAS low             | 40          |       | 48          |       | 55          |       | ns   |
| tRSH   | RAS hold time after CAS low             | 13          |       | 15          |       | 20          |       | ns   |
| tRCS   | Read Setup time before CAS low          | 0           |       | 0           |       | 0           |       | ns   |
| tRCH   | Read hold time after CAS high (Note 22) | 0           |       | 0           |       | 0           |       | ns   |
| tRRH   | Read hold time after RAS high (Note 22) | 10          |       | 10          |       | 10          |       | ns   |
| tRAL   | Column address to RAS hold time         | 25          |       | 30          |       | 35          |       | ns   |
| tCAL   | Column address to CAS hold time         | 13          |       | 18          |       | 23          |       | ns   |

Note 22: Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## Write Cycle (Early Write)

| Symbol           | Parameter                               | Limits      |       |             |       |             |       | Unit |
|------------------|---|-------------|-------|-------------|-------|-------------|-------|------|
|                  |   | MH2M365C -5 |       | MH2M365C -6 |       | MH2M365C -7 |       |      |
|                  |   | Min         | Max   | Min         | Max   | Min         | Max   |      |
| t <sub>WC</sub>  | Write cycle time                        | 90          |       | 110         |       | 130         |       | ns   |
| t <sub>RAS</sub> | RAS low pulse width                     | 50          | 10000 | 60          | 10000 | 70          | 10000 | ns   |
| t <sub>CAS</sub> | CAS low pulse width                     | 8           | 10000 | 10          | 10000 | 13          | 10000 | ns   |
| t <sub>CSH</sub> | CAS hold time after RAS low             | 40          |       | 48          |       | 55          |       | ns   |
| t <sub>RSH</sub> | RAS hold time after CAS low             | 13          |       | 15          |       | 20          |       | ns   |
| t <sub>WCS</sub> | Write setup time before CAS low         | 0           |       | 0           |       | 0           |       | ns   |
| t <sub>WCH</sub> | Write hold time after CAS low           | 8           |       | 10          |       | 13          |       | ns   |
| t <sub>WP</sub>  | Write pulse width                       | 8           |       | 10          |       | 13          |       | ns   |
| t <sub>DS</sub>  | Data setup time before CAS low or W low | 0           |       | 0           |       | 0           |       | ns   |
| t <sub>DH</sub>  | Data hold time after CAS low or W low   | 8           |       | 10          |       | 13          |       | ns   |

## Hyper page Mode Cycle (Read, Early Write, Hi-Z control by $\overline{W}$ ) (Note 25)

| Symbol            | Parameter  | Limits      |        |             |        |             |        | Unit |
|-------------------|--|-------------|--------|-------------|--------|-------------|--------|------|
|                   |  | MH2M365C -5 |        | MH2M365C -6 |        | MH2M365C -7 |        |      |
|                   |  | Min         | Max    | Min         | Max    | Min         | Max    |      |
| t <sub>HPC</sub>  | Hyper page mode read/write cycle time                | 20          |        | 25          |        | 30          |        | ns   |
| t <sub>DOH</sub>  | Output hold time from $\overline{CAS}$ low           | 5           |        | 5           |        | 5           |        | ns   |
| t <sub>RAS</sub>  | RAS low pulse width for read write cycle (Note24)    | 65          | 100000 | 77          | 100000 | 92          | 100000 | ns   |
| t <sub>CP</sub>   | CAS high pulse width (Note25)                        | 8           | 13     | 10          | 16     | 13          | 16     | ns   |
| t <sub>CPRH</sub> | RAS hold time after $\overline{CAS}$ precharge       | 30          |        | 35          |        | 40          |        | ns   |
| t <sub>CHOL</sub> | Hold time to maintain the data Hi-Z until CAS access | 7           |        | 7           |        | 7           |        | ns   |
| t <sub>WPE</sub>  | $\overline{W}$ Pulse Width (Hi-Z control)            | 7           |        | 7           |        | 7           |        | ns   |

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

24: t<sub>RAS(min)</sub> is specified as two cycles of CAS input are performed.

25: t<sub>CP(max)</sub> is specified as a reference point only.

## CAS before RAS Refresh Cycle (Note 26)

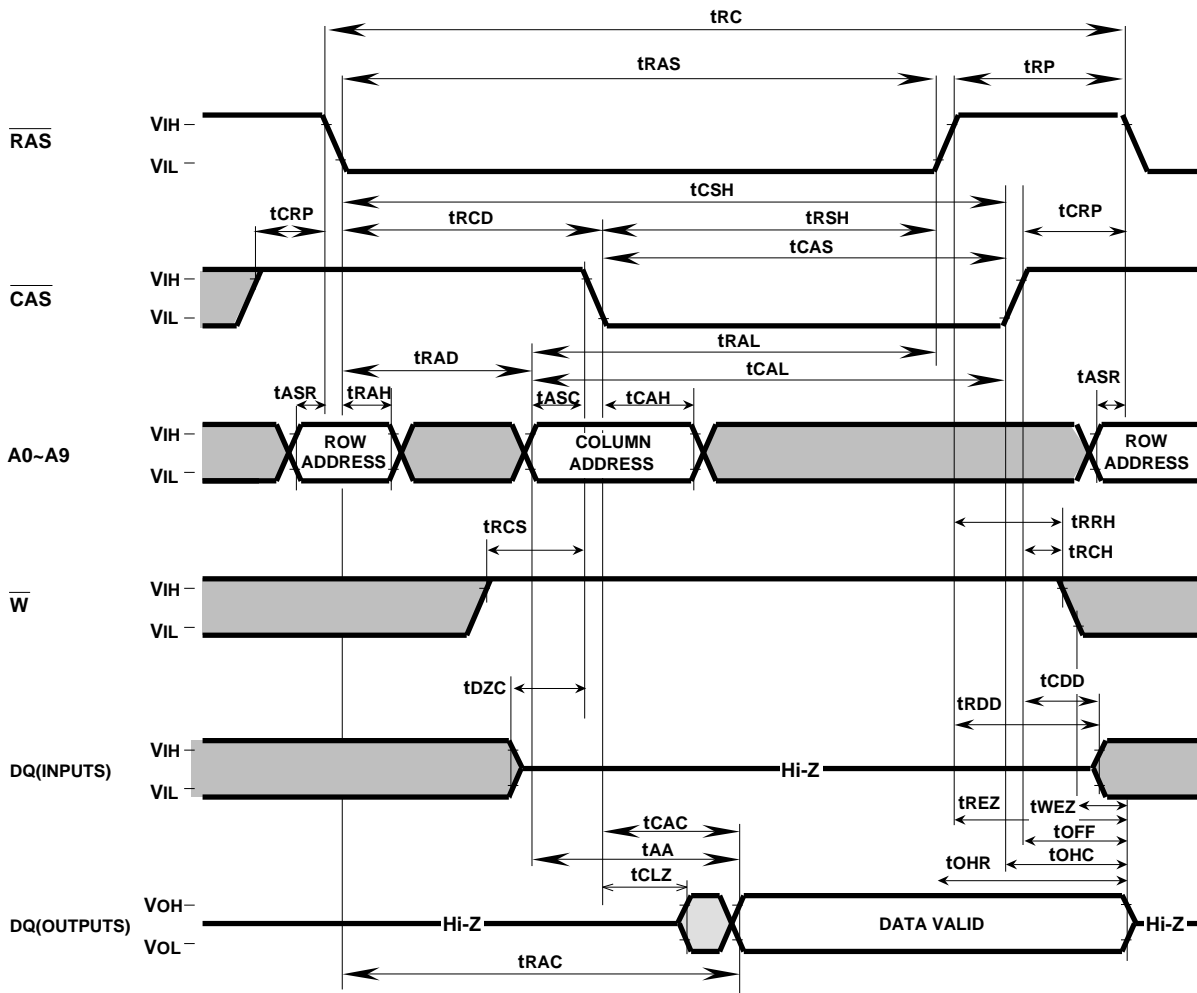
| Symbol           | Parameter                     | Limits      |     |             |     |             |     | Unit |
|------------------|-------------------------------|-------------|-----|-------------|-----|-------------|-----|------|
|                  |                               | MH2M365C -5 |     | MH2M365C -6 |     | MH2M365C -7 |     |      |
|                  |                               | Min         | Max | Min         | Max | Min         | Max |      |
| t <sub>CSR</sub> | CAS setup time before RAS low | 5           |     | 5           |     | 5           |     | ns   |
| t <sub>CHR</sub> | CAS hold time after RAS low   | 10          |     | 10          |     | 15          |     | ns   |

Note 26: Eight or more  $\overline{CAS}$  before  $\overline{RAS}$  cycles instead of eight  $\overline{RAS}$  cycles are necessary for proper operation of  $\overline{CAS}$  before  $\overline{RAS}$  refresh mode.

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## Timing Diagrams (Note 27) Read Cycle



Note 27

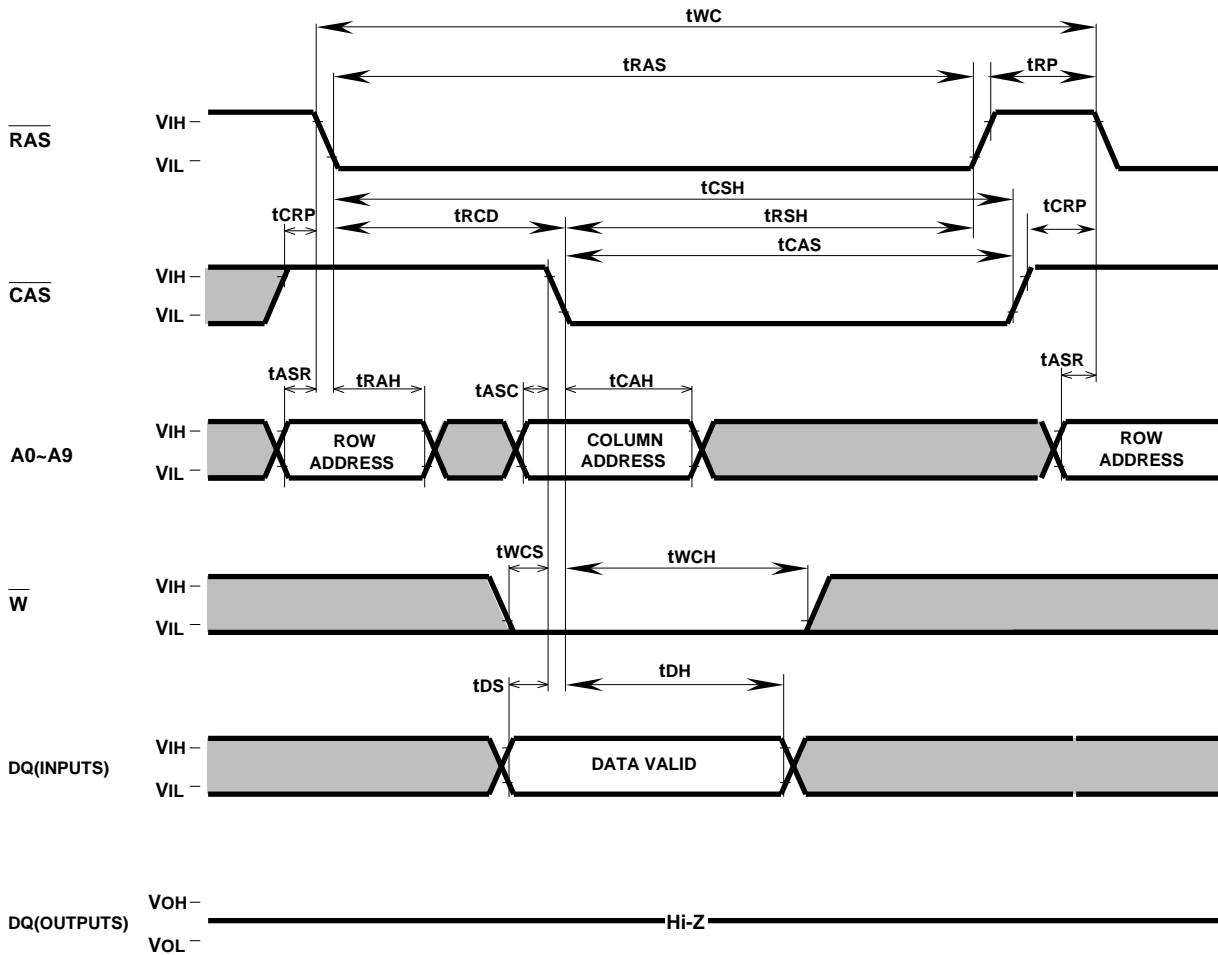


Indicates the don't care input.  
 $V_{IH(min)}$   $V_{IN}$   $V_{IH(max)}$  or  
 $V_{IL(min)}$   $V_{IN}$   $V_{IL(max)}$   
 Indicates the invalid output.

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## Early Write Cycle



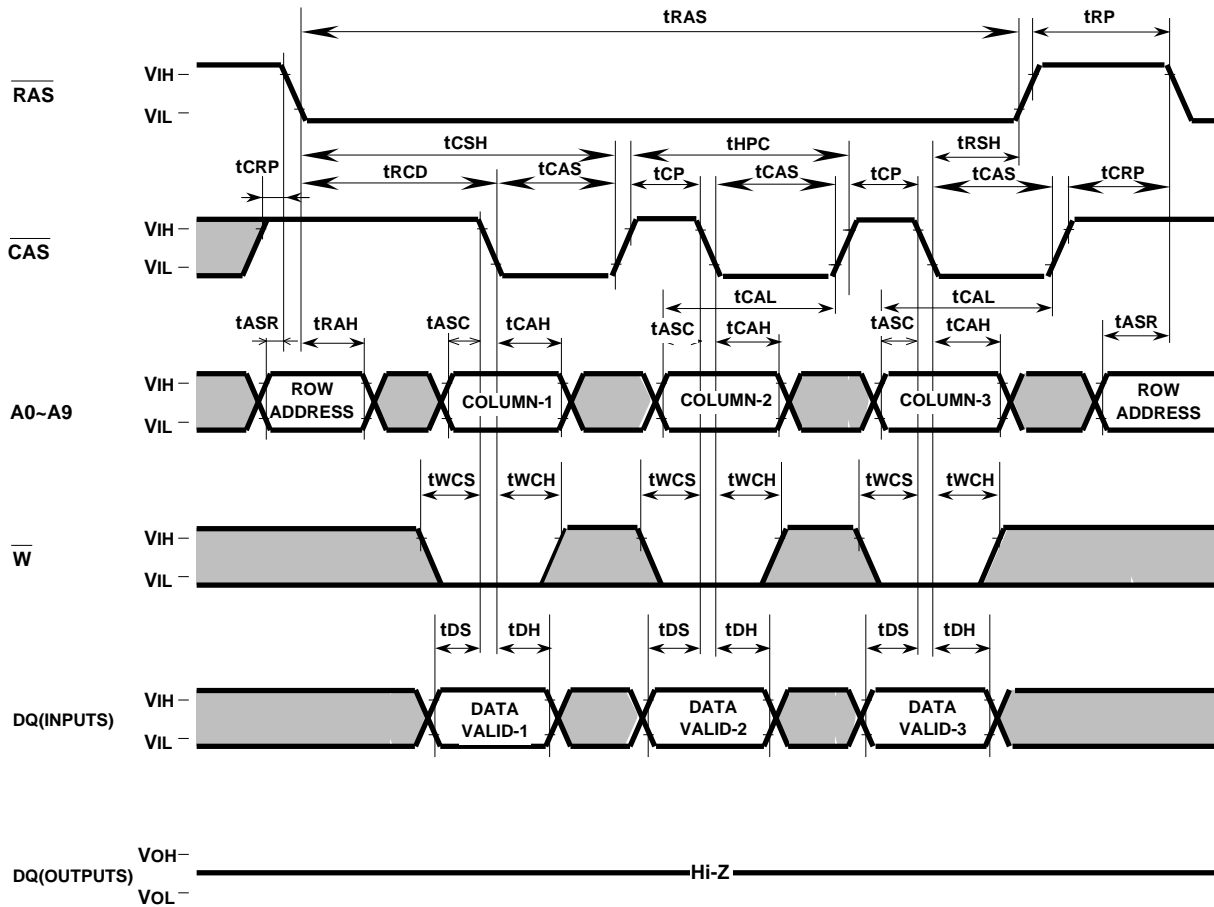




# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## Hyper Page Mode Early Write Cycle

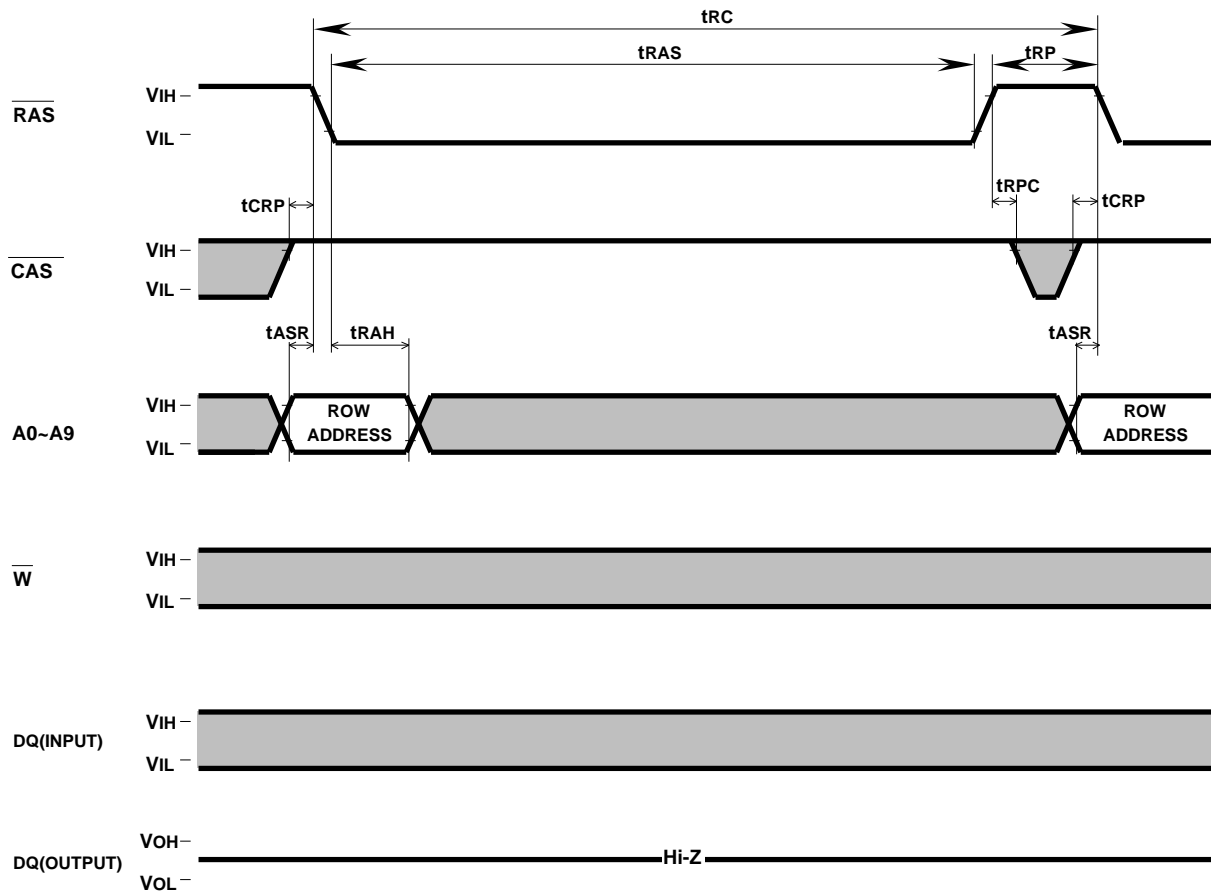




# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

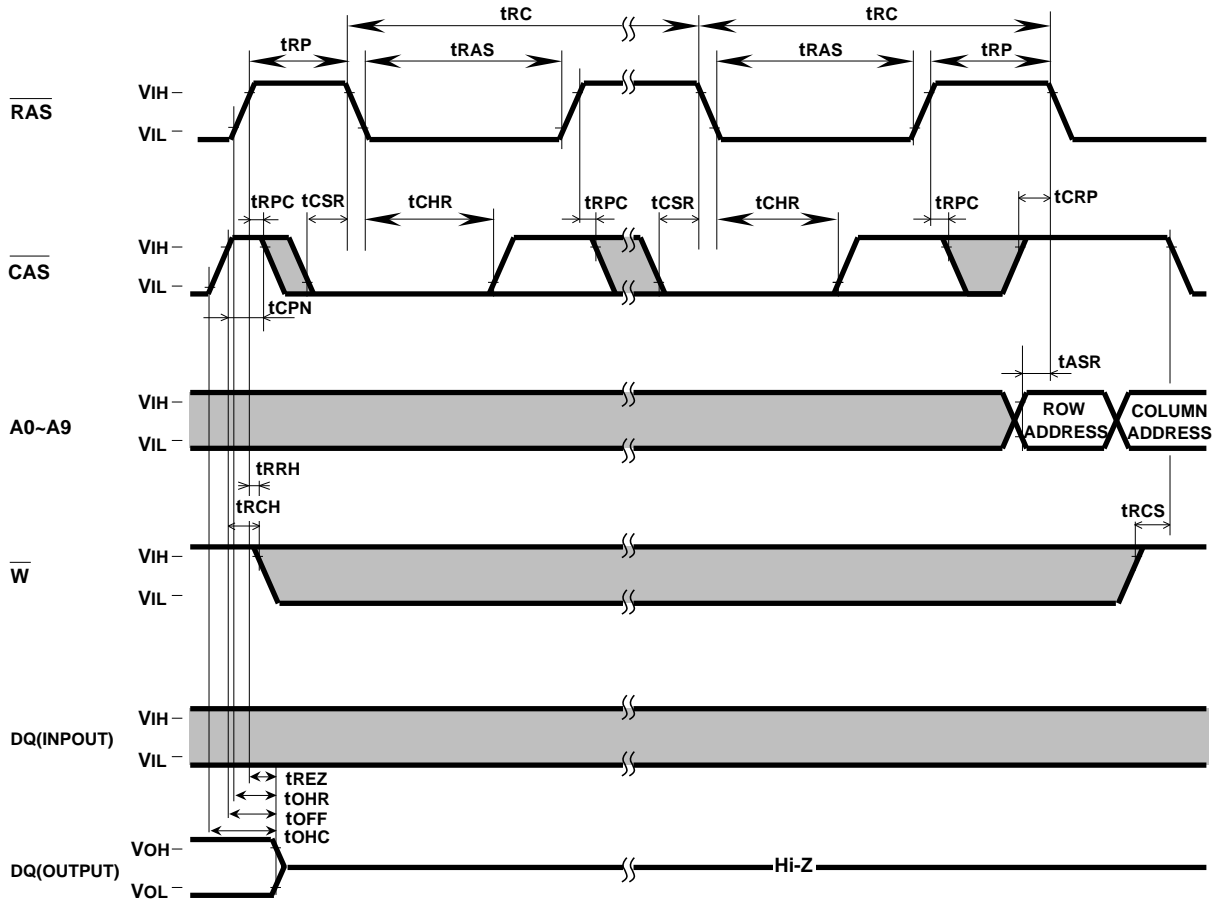
## RAS-only Refresh Cycle



# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

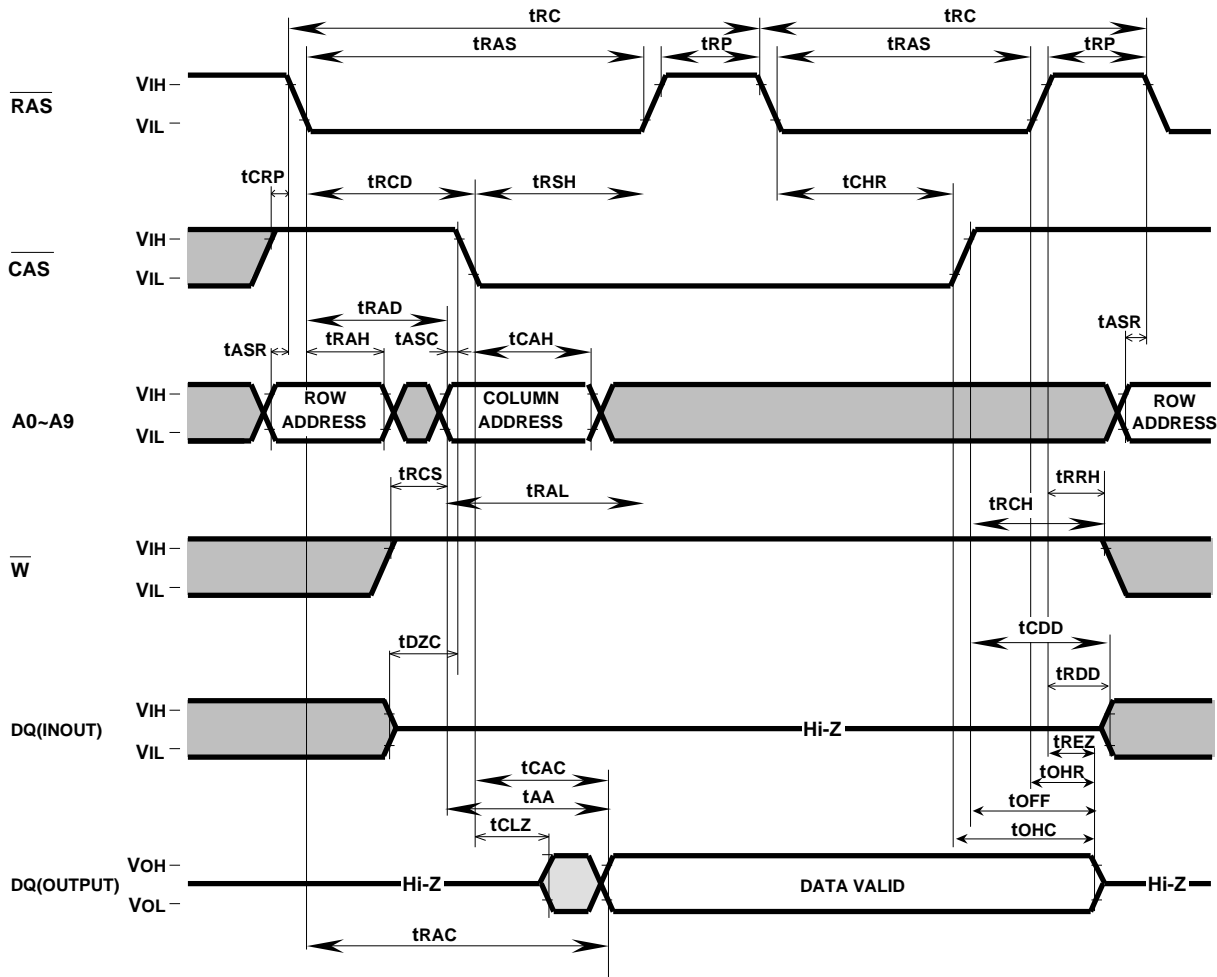
## CAS before RAS Refresh Cycle



# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## Hidden Refresh Cycle (Read) (Note 28)



Note 28: Early write cycle is applicable instead of read cycle.  
Timing requirements and output state are the same as that of each cycle shown above.

# MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT ( 2097152-WORD BY 36-BIT ) DYNAMIC RAM

## 72pin DRAM Module Outline

