

MHR Series

9x14 mm, 5.0 Volt, HCMOS/TTL, Clock Oscillator



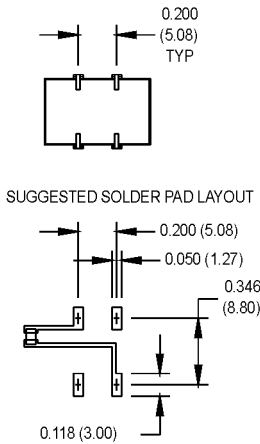
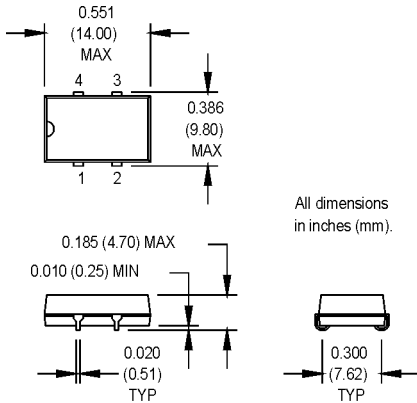
Ordering Information

00.0000
MHz

MHR 1 3 T A J -R

Product Series
 Temperature Range
 1: 0°C to +70°C 2: -40°C to +85°C
 6: -20°C to +70°C
 Stability
 3: ±100 ppm 4: ±50 ppm
 6: ±25 ppm * 8: ±20 ppm
 Output Type
 F: Fixed T: Tristate
 Symmetry/Logic Compatibility
 A: 40/60 TTL/HCMOS (Standard for 1.000 to 50.000 MHz)
 *B: 45/55 TTL
 *C: 45/55 HCMOS
 F: 40/60 TTL (50.001 to 67.000 MHz)
 G: 40/60 HCMOS (50.001 to 80.000 MHz)
 Package/Lead Configurations
 J: J Lead
 RoHS Compliance
 Blank: non-RoHS compliant part
 -R: RoHS compliant part
 Frequency (customer specified)

* Consult factory regarding availability of "B" and "C" symmetry codes, and "8" stability code.



NOTE: A capacitor of value 0.01 μF or greater between Vdd and Ground is recommended.

Pin Connections

PIN	FUNCTION
1	N/C or Tristate
2	Ground
3	Output
4	+Vdd

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	1		80	MHz	
Operating Temperature	T _A	(See Ordering Information)				
Storage Temperature	T _s	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				
Aging						
1st Year		-5		+5	ppm	
Thereafter (per year)		-5		+5	ppm	
Input Voltage	V _{dd}	4.5	5.0	5.5	V	
Input Current	I _{dd}			30	mA	1.000 to 40.000 MHz
				50	mA	40.001 to 50.000 MHz
				55	mA	50.001 to 80.000 MHz
Output Type						HCMOS/TTL
Load						See Note 1
1 to 50 MHz		10 TTL or 50 pF				
50.001 to 67 MHz		5 TTL or 30 pF				
67.001 to 80 MHz		15 pF				
Symmetry (Duty Cycle)		(See Ordering Information)				
Logic "1" Level	V _{oh}	90% V _{dd}			V	HCMOS Load
		V _{dd} -0.5			V	TTL Load
Logic "0" Level	V _{ol}			10% V _{dd}	V	HCMOS Load
				0.5	V	TTL Load
Output Current				±12	mA	
Rise/Fall Time	Tr/Tf					See Note 3
1 to 40 MHz				10	ns	
40.001 to 50 MHz				8	ns	
50.001 to 80 MHz				6	ns	
Tristate Function		Input Logic "1" or floating; output active Input Logic "0"; output disables to high-Z				
Start up Time				10	ms	
Random Jitter	R _j		5	12	ps RMS	1-Sigma

1. TTL load - See load circuit diagram #1. HCMOS load - See load circuit diagram #2.
2. Symmetry is measured at 1.4 V with TTL load, and at 50% V_{dd} with HCMOS load.
3. Rise/fall times are measured between 0.5 V and 2.4 V for TTL load, and between 10% and 90% V_{dd} for HCMOS load.

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