ML4819*

Power Factor and PWM Controller "Combo"

GENERAL DESCRIPTION

The ML4819 is a complete boost mode Power factor Controller (PFC) which also contains a PWM controller. The PFC circuit is similar to the ML4812 while the PWM controller can be used for current or voltage mode control for a second stage converter. Since the PWM and PFC circuits share the same oscillator, synchronization of the two stages is inherent. The outputs of the controller IC provide high current (>1A peak) and high slew rate to quickly charge and discharge MOSFET gates. Special care has been taken in the design of the ML4819 to increase system noise immunity.

The PFC section is of the peak current sensing boost type, using a current sense transformer or current sensing MOSFETs to non-dissipatively sense switch current. This gives the system overall efficiency over average current sensing control method.

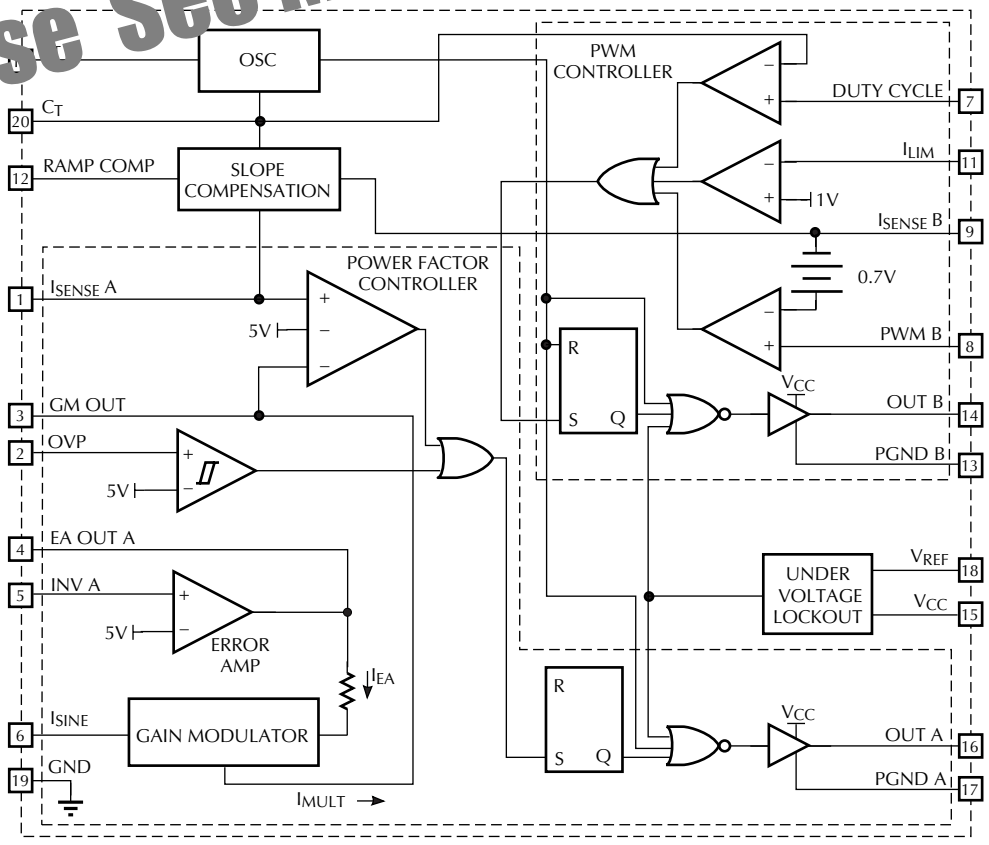
The PWM section includes cycle by cycle current limiting, precise duty cycle limiting for single ended converters, and slope compensation.

FEATURES

- Two 1A peak current totem-pole output drivers
- Precision buffered 5V reference (±1%)
- Large oscillator amplitude for better noise immunity
- Precision duty cycle limit for PWM section
- Current input gain modulator improves noise immunity
- Programmable Ramp Compensation circuit
- Over-Voltage comparator helps prevent output "runaway"
- Wide common mode range in current sense compensators for better noise immunity
- Under-Voltage Lockout circuit with 6V hysteresis

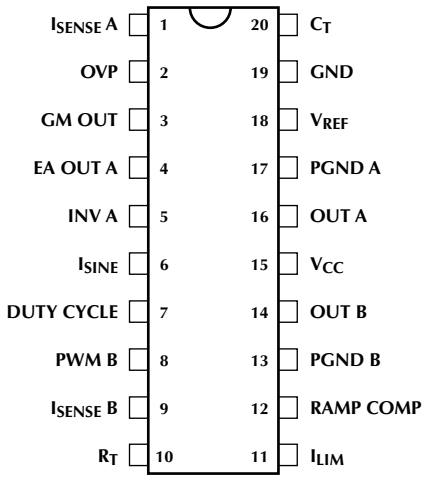
* Some Packages Are Obsolete

BLOCK DIAGRAM



PIN CONFIGURATION

ML4819
20-Pin PDIP



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	I_{SENSE} A	Input form the PFC current sense transformer to the PWM comparator (+). Current Limit occurs when this point reaches 5V.
2	OVP	Input to Over-Voltage comparator.
3	GM OUT	Output of Gain Modulator. A resistor to ground on this pin converts the current to a voltage.
4	EA OUT A	Output of error amplifier.
5	INV A	Inverting input to error amplifier.
6	I_{SINE}	Current Multiplier input.
7	DUTY CYCLE	PWM controller duty cycle is limited by setting this pin to a fixed voltage.
8	PWM B	Error voltage feedback input.
9	I_{SENSE} B	Input for Current Sense resistor for current mode operation or for Oscillator ramp for voltage mode operation.
10	R_T	Oscillator timing resistor pin. A 5V source across this resistor sets the charging current for C_T
11	I_{LIM}	Cycle by cycle PWM current limit. Exceeding 1V threshold on this pin terminates the PWM cycle.
12	RAMP COMP	Buffered output from the Oscillator Ramp (C_T). A resistor to ground sets a current, 1/2 of which is sourced on pins 9 and 11.
13	GND B	Return for the high current totem pole output of the PWM controller.
14	OUT B	PWM controller totem pole output.
15	V_{CC}	Positive Supply for the IC.
16	OUT A	PFC controller totem pole output.
17	GND A	Return for the high current totem pole output of the PFC controller.
18	V_{REF}	Buffered output for the 5V voltage reference
19	GND	Analog signal ground.
20	C_T	Timing Capacitor for the Oscillator.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Voltage (V_{CC}) 35V
Output Current, Source or Sink (RAMP COMP)
DC 1.0A
Output Energy (capacitive load per cycle) 5µJ
Multiplier I_{SINE} Input (I_{SINE}) 1.2mA
Error Amp Sink Current (GM OUT) 10mA
Oscillator Charge Current 2mA
Analog Inputs (ISENSE A, EA OUT A, INV A)
..... –0.3V to 5.5V
Junction Temperature ..... 150·C
Storage Temperature Range ..... –65·C to 150·C
Lead Temperature (soldering 10 sec.) ..... 260·C
Thermal Resistance (θ_{JA})
Plastic DIP or SOIC ..... 60·C/W

OPERATING CONDITIONS

Temperature Range
ML4819C ..... 0·C to 70·C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, R_T = 14kΩ, C_T = 1000pF, T_A = Operating Temperature Range, V_{CC} = 15V (Notes 1, 2).

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Initial Accuracy	T_J = 25·C	90	97	104	kHz
Voltage Stability	12V < V_{CC} < 18V		0.2		%
Temperature Stability			2		%
Total Variation	Line, temp.	88		106	kHz
Ramp Valley			0.9		V
Ramp Peak			4.3		V
R_T Voltage		4.8	5.0	5.2	V
Discharge Current (PWM B open)	T_J = 25·C, $V_{OUT\ A}$ = 2V	7.5	8.4	9.3	mA
	$V_{OUT\ A}$ = 2V	7.2	8.4	9.5	mA
DUTY CYCLE LIMIT COMPARATOR					
Input Offset Voltage		–15		15	mV
Input Bias Current			–2	–10	µA
Duty Cycle	$V_{DUTY\ CYCLE}$ = $V_{REF/2}$	43	45	49	%
REFERENCE					
Output Voltage	T_J = 25·C, I_O = 1mA	4.95	5.00	5.05	V
Line Regulation	12V < V_{CC} < 25V		2	20	mV
Load Regulation	1mA < I_O < 20mA		8	25	mV
Temperature Stability			0.4		%
Total Variation	Line, load, temperature	4.9		5.1	V
Output Noise Voltage	10Hz to 10kHz		50		µV
Long Term Stability	T_J = 125·C, 1000 hours, (Note 1)		5	25	mV
Short Circuit Current	V_{REF} = 0V	–30	–85	–180	mA
ERROR AMPLIFIER					
Input Offset Voltage		–15		15	mV
Input Bias Current			–0.1	–1.0	µA
Open Loop Gain	1 < $V_{EA\ OUT\ A}$ < 5V	60	75		dB
PSRR	12V < V_{CC} < 25V	60	90		dB
Output Sink Current	$V_{EA\ OUT\ A}$ = 1.1V, $V_{INV\ A}$ = 5.2V	2	12		mA
Output Source Current	$V_{EA\ OUT\ A}$ = 5.0V, $V_{INV\ A}$ = 4.8V	–0.5	–1.0		mA

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIER (continued)					
Output High voltage	$I_{EA\ OUT\ A}$ = –0.5mA, $V_{INV\ A}$ = 4.8V	6.5	7.0		V
Output Low Voltage	$I_{EA\ OUT\ A}$ = 2mA, $V_{INV\ A}$ = 5.2V		0.7	1.0	V
Unity Gain Bandwidth			1.0		MHz
GAIN MODULATOR					
I_{SINE} Input Voltage	I_{SINE} = 500µA	0.4	0.7	0.9	V
Output Current (GM OUT)	I_{SINE} = 500µA, INV A = V_{REF} –20mV	460	495	505	µA
	I_{SINE} = 500µA, INV A = V_{REF} + 20mV		0	10	µA
	I_{SINE} = 1mA, INV A = V_{REF} – 20mV	900	990	1005	µA
Bandwidth			200		kHz
PSRR	12V < V_{CC} < 25V		70		dB
SLOPE COMPENSATION CIRCUIT					
RAMP COMP Voltage			$V_{C(T)}$ – 1		V
I_{OUT} (I_{SENSE} A or I_{SENSE} B)	$I_{RAMP\ COMP}$ = 100µA (Note 3)	45	48	51	µA
OVP COMPARATOR					
Input Offset Voltage	Output Off	–15		15	mV
Hysteresis	Output On	100	120	140	mV
Input Bias Current			–0.3	–3	µA
Propagation Delay			150		ns
I_{SENSE} COMPARATORS					
Input Common Mode Range		–0.2		5.5	V
Input Offset Voltage	I_{SENSE} A	–15		15	mV
	I_{SENSE} B	0.4	0.7	0.9	V
Input Bias Current			–3	–10	µA
Input Offset Current		–3	0	3	µA
Propagation Delay			150		ns
I_{LIMIT} (A) Trip Point	V_{OVP} = 5.5V	4.8	5	5.2	V
I_{LIM} COMPARATOR					
I_{LIMIT} Trip Point		.95	1.0	1.05	V
Input Bias Current			–2	–10	µA
Propagation Delay			150		ns
OUTPUT DRIVERS					
Output Voltage Low	I_{OUT} = –20mA		0.1	0.4	V
	I_{OUT} = –200mA		1.6	2.2	V
Output Voltage High	I_{OUT} = 20mA	13	13.5		V
	I_{OUT} = 200mA	12	13.4		V
Output Voltage Low in UVLO	I_{OUT} = –1mA, V_{CC} = 8V		0.1	0.8	V
Output Rise/Fall Time	C_L = 1000pF		50		ns

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
UNDER-VOLTAGE LOCKOUT					
Start-Up Threshold		15	16	17	V
Shut-Down Threshold		9	10	11	V
V_{REF} Good Threshold			4.4		V
SUPPLY					
Supply Current	Start-Up, V_{CC} = 14V		0.6	1.2	mA
	Operating, T_J = 25·C		25	35	mA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
Note 2: V_{CC} is raised above the Start-Up Threshold first to activate the IC, then returned to 15V.
Note 3: PWM comparator bias currents are subtracted from this reading.

FUNCTIONAL DESCRIPTION

OSCILLATOR

The ML4819 oscillator charges the external capacitor (C_T) with a current (I_{SET}) equal to $5/R_{SET}$. When the capacitor voltage reaches the upper threshold, the comparator changes state and the capacitor discharges to the lower threshold through Q1. While the capacitor is discharging, the clock provides a high pulse.

The oscillator period can be described by the following relationship:

$$t_{OSC} = t_{RAMP} + t_{DEADTIME}$$

where:

$$t_{RAMP} = \frac{C(\text{Ramp Valley to Peak})}{I_{SET}}$$

and:

$$t_{DEADTIME} = \frac{C(\text{Ramp Valley to Peak})}{8.4mA - I_{SET}}$$

The maximum duty cycle of the PWM section can be limited by setting a threshold on pin 7. when the C_T ramp is above the threshold at pin 7, the PWM output is held off and the PWM flip-flop is set:

$$D_{LIMIT} \cong \frac{D_{OSC} \times (V_{PIN7} - 0.9)}{3.4}$$

where:

D_{LIMIT} = Desired duty cycle limit
D_{OSC} = Oscillator duty cycle

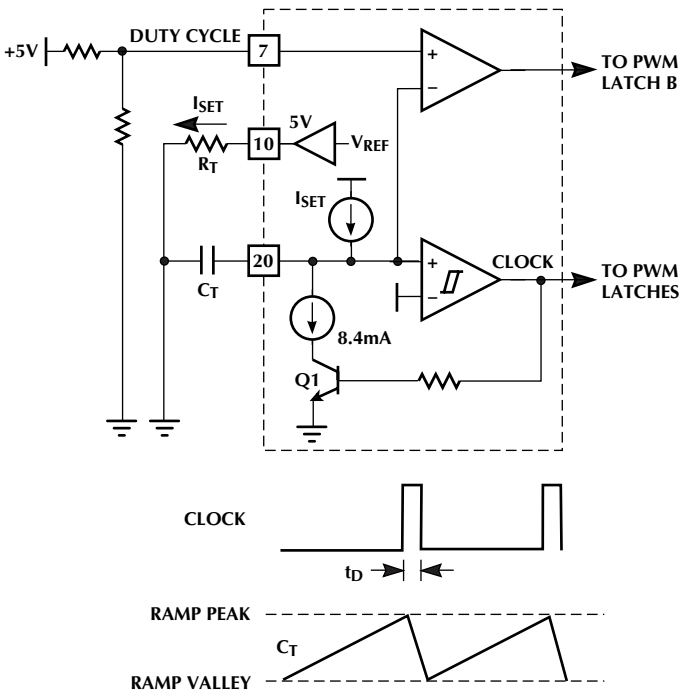


Figure 1. Oscillator Block Diagram

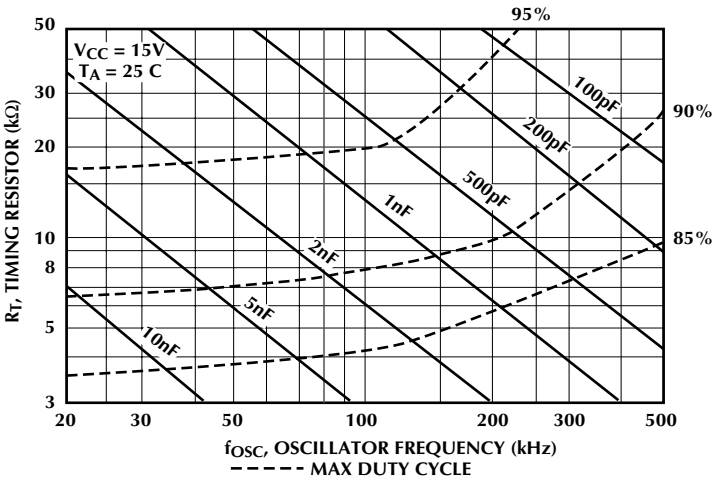


Figure 2. Oscillator Timing Resistance vs. Frequency

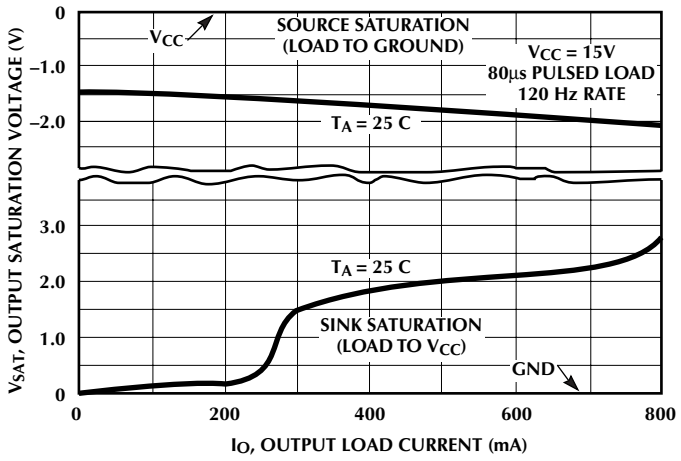


Figure 3. Output Saturation Voltage vs. Output Current

ERROR AMPLIFIER

The ML4819 error amplifier is a high open loop gain, wide bandwidth amplifier.

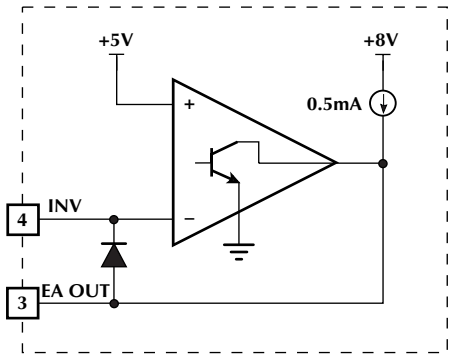


Figure 4. Error Amplifier Configuration

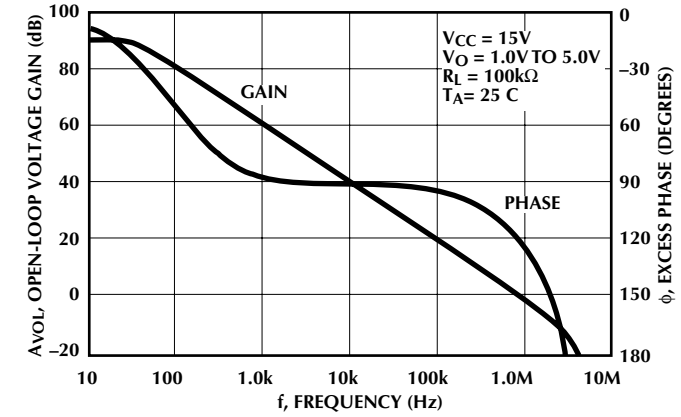


Figure 5. Error Amplifier Open-Loop Gain and Phase vs Frequency

GAIN MODULATOR

The ML4819 gain modulator is a linear current input multiplier to provide high immunity to the disturbances caused by high power switching. The rectified line input sine wave is converted to a current via a dropping resistor. In this way, small amounts of ground noise produce an insignificant effect on the reference to the PWM comparator.

The output of the gain modulator is a current of the form:

I_{OUT} is proportional to $I_{SINE} \propto I_{EA}$

where I_{SINE} is the current in the dropping resistor, and I_{EA} is a current proportional to the output of the error amplifier. When the error amplifier is saturated high, the output of the gain modulator is approximately equal to the I_{SINE} input current.

The gain modulator output current is converted into the reference voltage for the PWM comparator through a resistor to ground on the gain modulator output. The gain modulator output is clamped to 5V to provide current limiting.

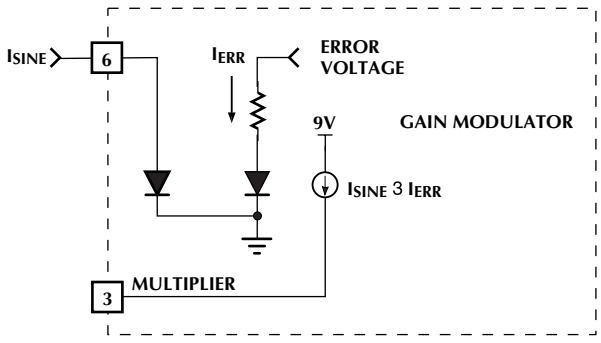


Figure 6. Gain Modulator Block Diagram

SLOPE COMPENSATION

Slope compensation is accomplished by adding 1/2 of the current flowing out of pin 12 to pin 1 (for the PFC section and pin 9 (for the PWM section). The amount of slope compensation is equal to ($I_{RAMP\ COMP}/2$) ∞ R_L where R_L is the impedance to GND on pin 1 or pin 9. Since most of the PWM applications will be limited to 50% duty cycle, slope compensation should not be needed for the PWM section. This can be defeated by using a low impedance load to the current sense on pin 9.

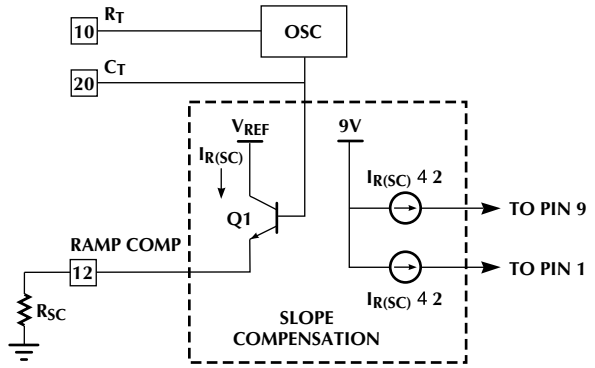


Figure 7. Slope Compensation Circuit

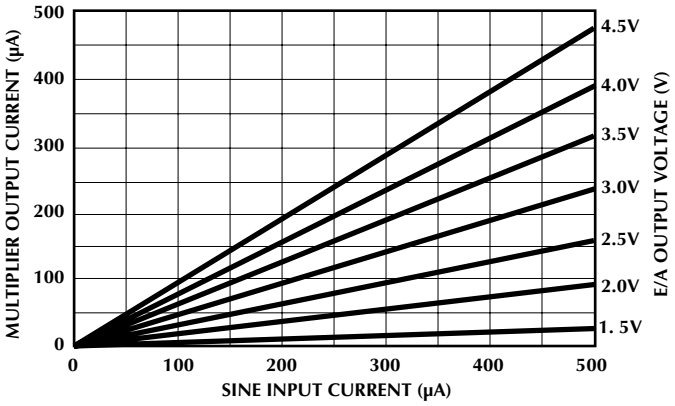


Figure 8. Gain Modulator Linearity

UNDER VOLTAGE LOCKOUT

On power-up the ML4819 remains in the UVLO condition; output low and quiescent current low. The IC becomes operational when V_{CC} reaches 16V. When V_{CC} drops below 10V, the UVLO condition is imposed. During the UVLO condition, the 5V V_{REF} pin is "off", making it usable as a status flag.

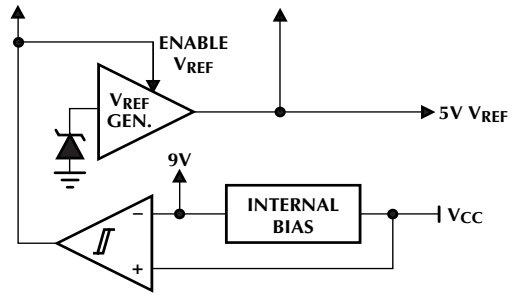


Figure 9. Under-Voltage Lockout Block Diagram

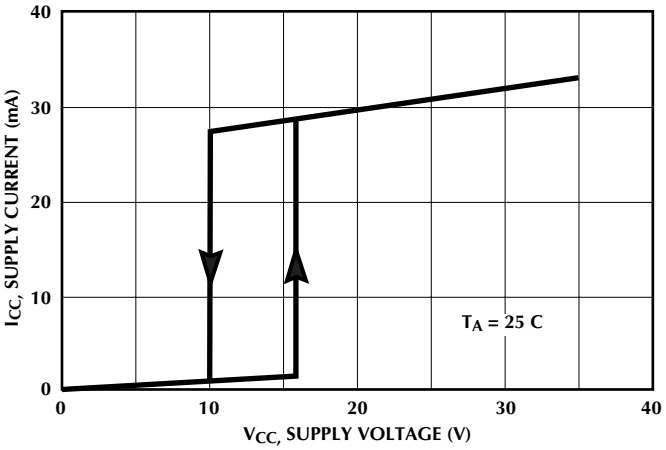


Figure 10a. Total Supply Current vs. Supply Voltage

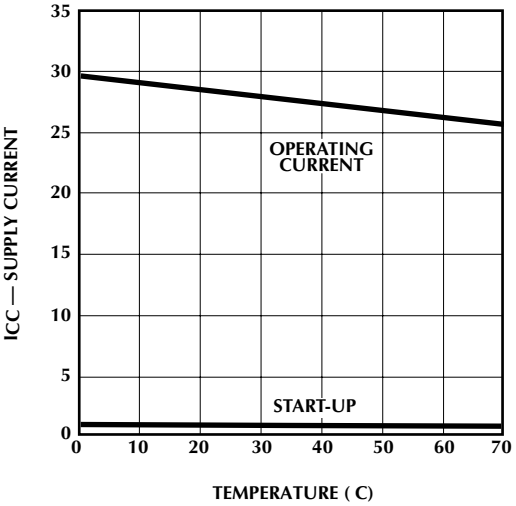


Figure 10b. Supply Current (I_{CC}) vs. Temperature

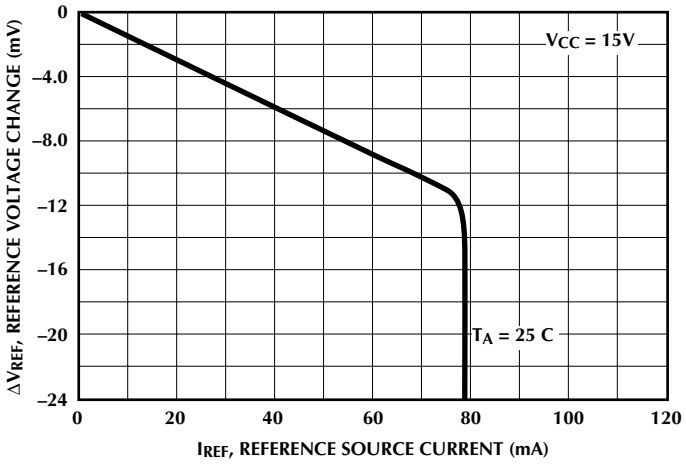


Figure 11. Reference Load Regulation

APPLICATIONS

POWER FACTOR SECTION

The power factor section in the ML4819 is similar to the power factor section in the ML4812 with the exception of the operation of the slope compensation circuit. Please refer to the ML4812 data sheet for more information.

The following calculations refer to Figure 12 in this data sheet. The component designators in the equations below refer to the following components in Figure 12:

R_T = R16, C_T = C6.

INPUT INDUCTOR (L1) SELECTION

The central component in the regulator is the input boost inductor. The value of this inductor controls various critical operational aspects of the regulator. If the value is too low, the input current distortion will be high and will result in low power factor and increased noise at the input. This will require more input filtering. In addition, when the value of the inductor is low the inductor dries out (runs out of current) at low currents. Thus the power factor will decrease at lower power levels and/or higher line voltages. If the inductor value is too high, then for a given operating current the required size of the inductor core will be large and/or the required number of turns will be high. So a balance must be reached between distortion and core size.

One more condition where the inductor can dry out is analyzed below where it is shown to be maximum duty cycle dependent.

For the boost converter at steady state:

$$V_{OUT} = \frac{V_{IN}}{1 - D_{ON}} \quad (1)$$

Where D_{ON} is the duty cycle $[T_{ON}/(T_{ON} + T_{OFF})]$. The input boost inductor will dry out when the following condition is satisfied:

$$V_{IN}(t) < V_{OUT} \times \left[1 - D_{ON(MAX)}\right] \quad (2)$$

or

$$V_{INDRY} = \left[1 - D_{ON(MAX)}\right] \times V_{OUT} \quad (3)$$

V_{INDRY}: Voltage where the inductor dries out.
V_{OUT}: Output dc voltage.

Effectively, the above relationship shows that the resetting volt-seconds are more than setting volt-seconds. In energy transfer terms this means that less energy is stored in the inductor during the ON time than it is asked to deliver during the OFF time. The net result is that the inductor dries out.

The recommended maximum duty cycle is 95% at 100KHz to allow time for the input inductor to dump its energy to the output capacitors.

For example:

if: V_{OUT} = 380V and
$D_{ON(MAX)}$ = 0.95

then substituting in (3) yields V_{INDRY} = 20V. The effect of drying out is an increase in distortion at low input voltages.

For a given output power, the instantaneous value of the input current is a function of the input sinusoidal voltage waveform. As the input voltage sweeps from zero volts to its maximum value and back, so does the current.

The load of the power factor regulator is usually a switching power supply which is essentially a constant power load. As a result, an increase in the input voltage will be offset by a decrease in the input current.

By combining the ideas set forth above, some ground rules can be obtained for the selection and design of the input inductor:

Step 1: Find minimum operating current.

$$I_{IN(MIN)PEAK} = \frac{1.414 \times P_{IN(MIN)}}{V_{IN(MAX)}} \quad (4)$$

$V_{IN(MAX)}$ = 260V

$P_{IN(MIN)}$ = 50W

then:

$I_{IN(MIN)PEAK}$ = 0.272A

Step 2: Choose a minimum current at which point the inductor current will be on the verge of drying out. For this example 40% of the peak current found in step 1 was chosen.

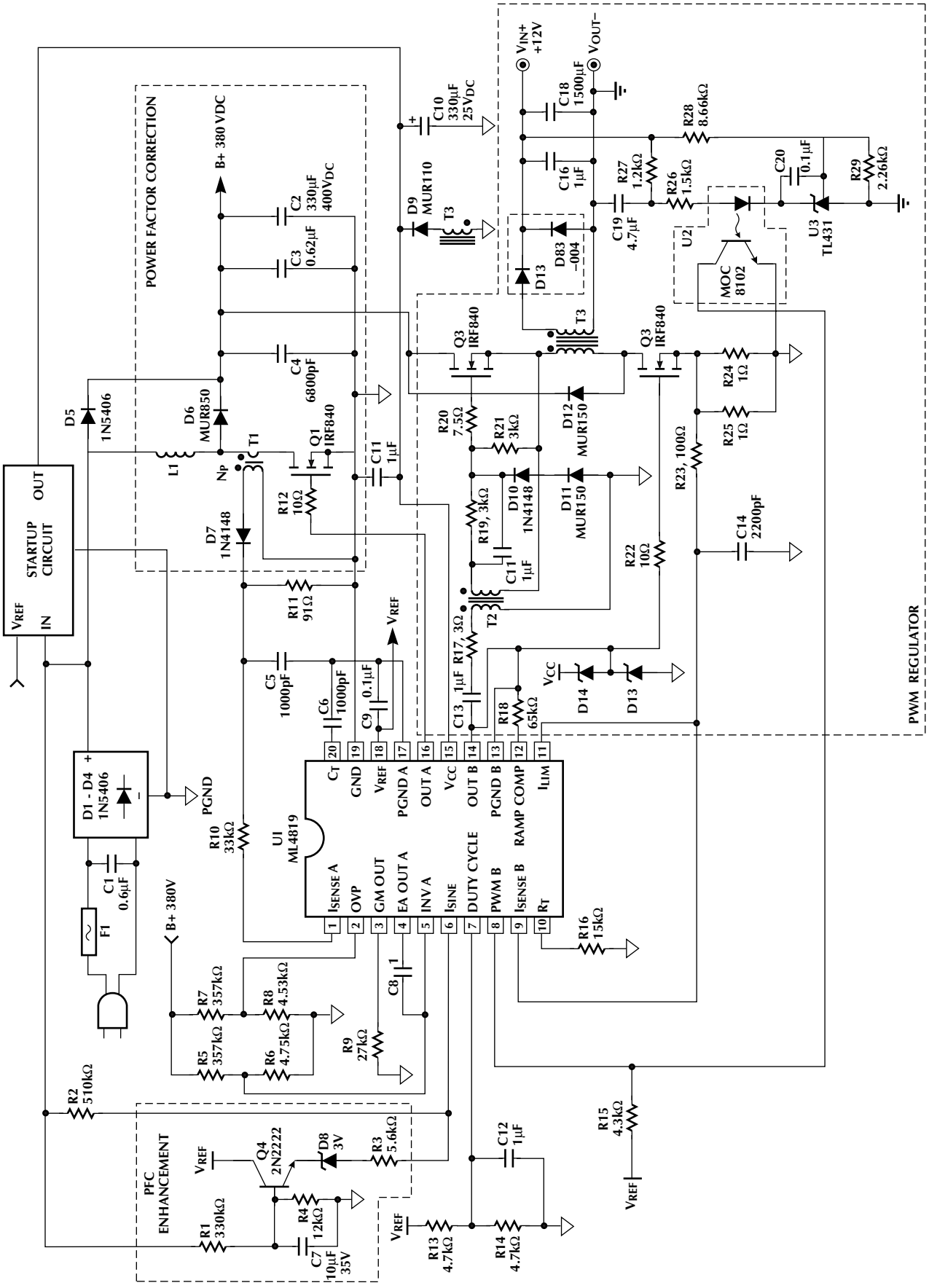


Figure 12. Typical Application, 180W Power Factor Corrected 12V Output Power Supply

then: I_{LDRY} = 100mA

Step 3: The value of the inductance can now be found using previously calculated data.

$$L1 = \frac{V_{INDRY} \times D_{ON(MAX)}}{I_{L(DRY)} \times f_{OSC}} = \frac{20V \times 0.95}{100mA \times 100kHz} = 2mH \quad (5)$$

The inductor can be allowed to decrease in value when the current sweeps from minimum to maximum value. This allows the use of smaller core sizes. The only requirement is that the ramp compensation must be adequate for the lower inductance value of the core so that there is adequate compensation at high current.

Step 4: The presence of the ramp compensation will change the dry out point, but the value found above can be considered a good starting point. Based on the amount of power factor correction the value of L1 can be optimized after a few iterations.

Gapped Ferrites, Molypermalloy, and Powdered Iron cores are typical choices for core material. The core material selected should have a high saturation point and acceptable losses at the operating frequency.

One ferrite core that is suitable at around 200W is the #4229PL00-3C8 made by Ferroxcube. This ungapped core will require a total gap of 0.180" for this application.

OSCILLATOR COMPONENT SELECTION

The oscillator timing components can be calculated by using the following expression:

$$f_{OSC} = \frac{1.36}{R_T \times C_T} \quad (6)$$

For example:

Step 1: At 100kHz with 95% duty cycle T_{OFF} = 500ns calculate C_T using the following formula:

$$C_T = \frac{t_{OFF} \times I_{DIS}}{V_{OSC}} = 1000pF \quad (7)$$

Step 2: Calculate the required value of the timing resistor.

$$R_T = \frac{1.36}{f_{OSC} \times C_T} = \frac{1.36}{100kHz \times 1000pF} = 13.6k\Omega. \text{ Choose } R_T = 14k\Omega. \quad (8)$$

CURRENT SENSE AND SLOPE (RAMP) COMPENSATION COMPONENT SELECTION

Slope compensation in the ML4819 is provided internally. A current equal to $V_{CT}/2(R18)$ is added to I_{SENSE} A (pin 1). this is converted to a voltage by R10, adding slope to the sensed current through T1. The amount of slope compensation should be at least 50% of the downslope of the inductor current during the off time as reflected on pin 1. Note that slope compensation is a requirement only if the inductor current is continuous and the duty cycle is more than 50%. The highest inductor downslope is found at the point of inductor discontinuity:

$$\frac{di_L}{dt} = \frac{V_B - V_{IN\,DRY}}{L} = \frac{380V - 20V}{2mH} = 0.18\ A/\mu s \quad (9)$$

The downslope as reflected to the input of the PWM comparator is given by:

$$S_{PWM} = \frac{V_B - V_{IN\,DRY}}{L1} \times \frac{R_{11}}{N_C} \quad (10)$$

Where N_C is the turns ratio of the current transformer (T1) used. In general, current transformers simplify the sensing of switch currents, especially at high power levels where the use of sense resistors is complicated by the amount of power they have to dissipate. Normally the primary side of the transformer consists of a single turn and the secondary consists of several turns of either enameled magnet wire or insulated wire. The diameter of the ferrite core used in this example is 0.5" (SPANG/Magnetics F41206-TC). The rectifying diode at the output of the current transformer can be a 1N4148 for secondary currents up to 75mA average.

Current-sensing MOSFETs or resistive sensing can also be used to sense the switch current. In these cases, the sensed signal has to be amplified to the proper level before it is applied to the ML4819.

The value of the ramp compensation (SC_{PWM}) as seen at pin 1 is:

$$SC_{PWM} = \frac{2.5 \times R_9}{R_{16} \times C_6 \times R_{18}} \quad (11)$$

The required value for R_{18} can therefore be found by equating:

$$SC_{PWM} = A_{SC} \times S_{PWM}$$

where A_{SC} is the amount of slope compensation and solving for R_{18}.

The value of R_9 (pin 3) depends on the selection of R_2 (pin 6).

$$R_2 = \frac{V_{IN(MAX)PEAK}}{I_{SINE\ (PEAK)}} = \frac{260 \times 1.414}{0.72mA} = 510k\Omega \quad (12)$$

$$R_9 > \frac{V_{CLAMP} \times R_2}{V_{IN(MIN)PEAK}} = \frac{4.8 \times 510k\Omega}{80 \times 1.414} = 22k\Omega \quad (13)$$

Choose R9 = 27kΩ

The peak of the inductor current can be found approximately by:

$$I_{LPEAK} = \frac{1.414 \times P_{OUT}}{V_{IN\ (MIN)\ RMS}} = \frac{1.414 \times 200}{90} = 3.14A \quad (14)$$

Next select N_C, which depends on the maximum switch current. Assume 4A for this example. N_C is 80 turns.

$$R_{11} = \frac{V_{CLAMP} \times N_C}{I_{LPEAK}} = \frac{4.9 \times 80}{4} = 100\Omega \quad (15)$$

Where R_{11} is the sense resistor, and V_{CLAMP} is the current clamp at the inverting input of the PWM comparator. This clamp is internally set to 5V. In actual application it is a good idea to assume a value less than 5V to avoid unwanted current limiting action due to component tolerances. In this application V_{CLAMP} was chosen as 4.8V.

Having calculated R_{11} the value S_{PWM} and of R_{18} can now be calculated:

$$S_{PWM} = \frac{380V - 20}{2mH} \times \frac{100}{80} = 0.225V/\mu s$$

$$R_{18} = \frac{2.5 \times R_9}{A_{SC} \times S_{PWM} \times R_T \times C_T}$$

$$R_{18} = \frac{2.5 \times 28.8k}{0.7 \times (0.225 \times 10^6) \times 14k\Omega \times 1nF} \cong 30k\Omega \quad (16)$$

Choose R18 = 33kΩ

The following values were used in the calculation:

R_9 = 27kΩ	A_{SC} = 0.7
R_T = 14kΩ	C_T = 1nF

VOLTAGE REGULATION COMPONENTS

The values of the voltage regulation loop components are calculated based on the operating output voltage. Note that voltage safety regulations require the use of sense resistors that have adequate voltage rating. As a rule of thumb if 1/4W through-hole resistors are used, two of them should be put in series. The input bias current of the error amplifier is approximately 0.5µA, therefore the current available from the voltage sense resistors should be significantly higher than this value. Since two 1/4W resistors have to be used the total power rating is 1/2W. The operating power is set to be 0.4W then with 380V output voltage the value can be calculated as follows:

$$R_5 = (380V)^2 / 0.4W = 360k\Omega \quad (17)$$

Choose two 178kΩ, 1% connected in series.

Then R6 can be calculated using the formula below:

$$R_6 = \frac{V_{REF} \times R_5}{V_B - V_{REF}} = \frac{5V \times 356k\Omega}{380V - 5V} = 4.747k\Omega \quad (18)$$

Choose 4.75kΩ, 1%. One more critical component in the voltage regulation loop is the feedback capacitor for the error amplifier. The voltage loop bandwidth should be set such that it rejects the 120Hz ripple which is present at the output. If this ripple is not adequately attenuated it will cause distortion on the input current waveform. Typical bandwidths range anywhere from a few Hertz to 15Hz. The main compromise is between transient response and distortion. The feedback capacitor can be calculated using the following formula:

$$C_8 = \frac{1}{3.142 \times R_5 \times BW}$$

$$C_8 = \frac{1}{3.142 \times 356k\Omega \times 2Hz} = 0.44\mu F \quad (19)$$

OVERVOLTAGE PROTECTION (OVP) COMPONENTS

The OVP loop should be set so that there is no interaction with the voltage control loop. Typically it should be set to a level where the power components are safe to operate. Ten to fifteen volts above V_{OUT} seems to be adequate. This sets the maximum transient output voltage to about 395V.

By choosing the high voltage side resistor of the OVP circuit the same way as above i.e. R_7 = 356K then R_8 can be calculated as:

$$R_8 = \frac{V_{REF} \times R_7}{V_{OVP} - V_{REF}} = \frac{5V \times 356k\Omega}{395V - 5V} = 4.564k\Omega \qquad (20)$$

Choose 4.53kΩ, 1%.

Note that R_5, R_6, R_7 and R_8 should be tight tolerance resistors such as 1% or better.

OFF-LINE START-UP AND BIAS SUPPLY GENERATION

The Start-Up circuit in Figure 12 can be either a "bleed resistor" (39kΩ, 2W) or the circuit shown in Figure 13. The bleed resistor method offers advantage of simplicity and lowest cost, but may yield excessive turn-on delay at low line.

When the voltage on pin 15 (V_{CC}) exceeds 16V, the IC starts up. The energy stored on the C21 supplies the IC with running power until the supplemental winding on T3 can provide the power to sustain operation.

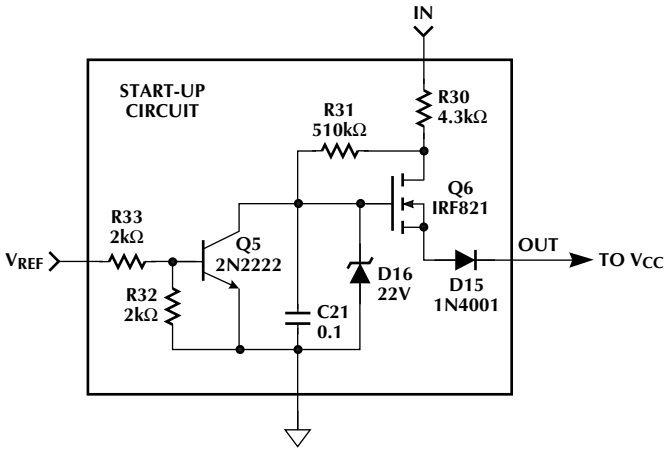


Figure 13. Start-Up Circuit

ENHANCEMENT CIRCUIT

The power factor enhancement circuit (inside the dotted lines) in Figure 11 is described in Application Note 11. It improves the power factor and lowers the input current harmonics. Note that the circuit meets IEC1000-3-2 specifications (with the enhancement circuit installed) on the harmonics by a large margin while correcting the input power factor to better than 0.99 under most steady state operating conditions.

PWM SECTION

The PWM section in Figure 12 is a two switch forward converter, shown in Figure 14 below for clarity. This fully clamped circuit eliminates the need for very high voltage MOSFETs. Flyback topology is also possible with the ML4819.

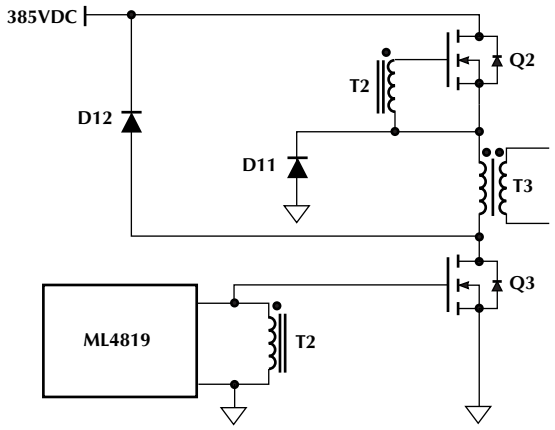


Figure 14. Two-Switch Forward Converter

This regulator (Figure 12) uses current mode control. Current is sensed through R24 and filtered for high frequency noise and leading edge transient through T23 and C14. The main regulation loop is through PWM B. The TL431 (U3) in the secondary serves as both the voltage reference and error amplifier. Galvanic isolation is provided by an optocoupler (U2) which provides a current command signal on pin 8. Loop compensation is provided by R29 and C20. The output voltage is set by:

$$V_{OUT} = 2.5\left(1 + \frac{R_{29}}{R_{28}}\right) \qquad (21)$$

The control loop is compensated using standard compensation techniques.

Current is limited to a threshold of 2A (1V on R24). The duty cycle is limited in this circuit to below 50% to prevent transformer (T3) core saturation. The maximum duty cycle limit of 45% is set using a threshold of $V_{REF}/2$ on pin 7.

the circuit in Figure 12 can be modified for voltage mode operation by utilizing the slope current which appears on pin 9 as show in figure 15 below.

The ramp amplitude appearing on pin 9 will be:

$$V_R = \frac{I_{R18}}{2} \times R(V) \qquad (22)$$

where R18 is the slope compensation resistor. Since this circuit operates with a constant input voltage (as supplied by the PFC section) voltage feed-forward is unnecessary.

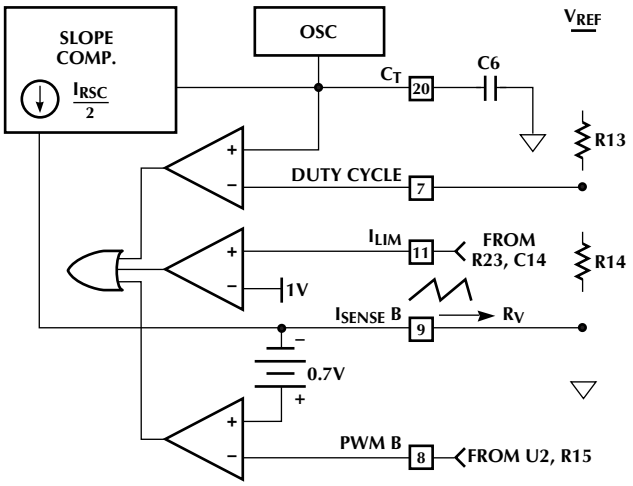


Figure 15. Voltage Mode Configuration

CONSTRUCTION AND LAYOUT TIPS

High frequency power circuits require special care during breadboard construction and layout. Double sided printed circuit boards with ground plane on one side are highly recommended. All critical switching leads (power FET, output diode, IC output and ground leads, bypass capacitors) should be kept as small as possible. This is to minimize both the transmission and pickup of switching noise.

There are two kinds of noise coupling; inductive and capacitive. As the name implies inductive coupling is due to fast changing (high di/dt) circulating switching currents. The main source is the loop formed by Q1, D6, and
C3–C4. Therefore this loop should be as small as possible, and the above capacitors should be good, high frequency types.

The second form of noise coupling is due to fast changing voltages (high dv/dt). The main source in this case is the drain of the power FET. The radiated noise in this case can be minimized by insulating the drain of the FET from the heatsink and then tying the heatsink to the source of the FET with a high frequency capacitor.

The IC has two ground pins named PWR GND and Signal GND. These two pins should be connected together with a very short lead at the printed circuit board exit point. In general grounding is very important and ground loops should be avoided. Star grounding schemes are preferred.

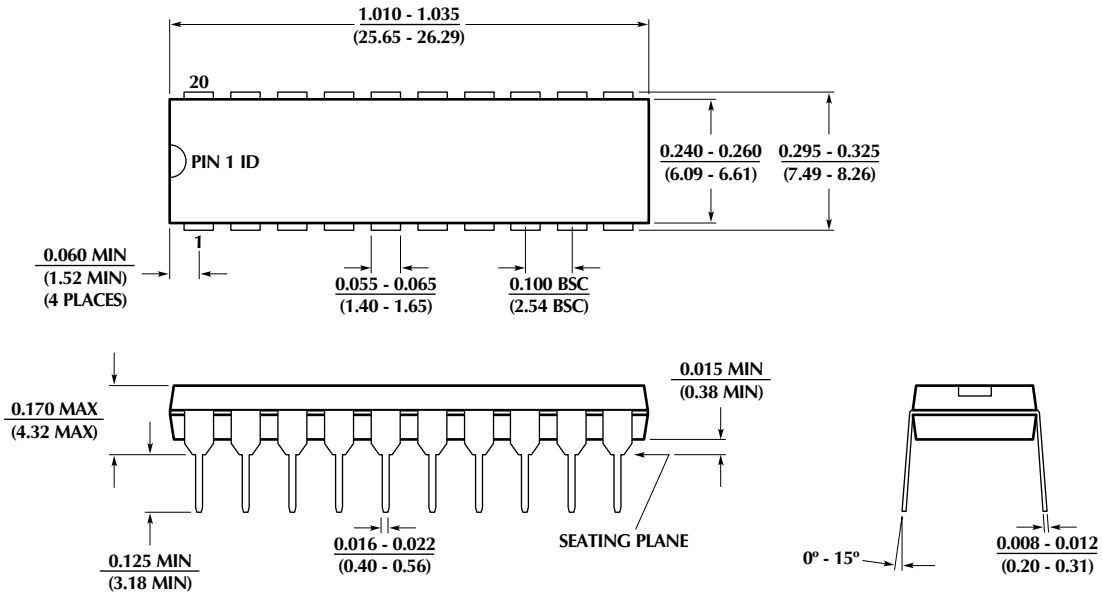
Component Values/Bill of Materials for Figure 12

Reference	Description
C1, C3	0.6µF, 630V Film (250 VAC)
C2	330µF 25V Electrolytic
C4	6800pF 1KV Ceramic
C5, C6	1000pF
C7	10µF 35V
C8, C11, C13, C15, C16	1µF Ceramic
C9, C20, C21	0.1µF Ceramic
C10	1500µF 25V Electrolytic
C12, C17	1µF Ceramic
C14	2200 pF
C18	1500µF 16V Electrolytic
C19	4.7µF
D1- D5	1N5406
D6	MUR850
D7, D10	1N4148
D8	3V Zener diode or 4 x 1N4148 in series
D9	MUR110
D11, D12	MUR150
D13	D83-004K
D15	1N4001
D16, D14	1N5818 or 1N5819
F1	5A, 250V, 3AG
L1	2mH, 4A I_{PEAK} Core: Ferroxcube 4229-3CB 150 Turns #24 AWG 0.150" gap
L2	10µH Core: Spang OF 43019 UG00 8 Turns #15AWG gap 0.05"
Q1-Q3	IRF840
Q4, Q5	2N2222
Q6	IRF821
R1	330ký
R2, R31	510ký
R3	5.6ký

Reference	Description
R4	12ký
R5, R7	357ký, 1%
R6	4.57ký, 1%
R8	4.53ký, 1%
R9	27ký
R10, R18	33ký
R11	91ý
R12, R22	10ý
R13, R14	4.7ký
R15	4.3ký
R16	15ký
R17	3 ý
R20	7.5ý
R21,R19	3ký
R23	100ý
R24, R25	1 ý
R26	1.5ký
R27	1.2ký
R28	8.66ký, 1%
R29	2.26ký, 1%
R30	2ký, 1W
R32, R33	2ký
T1	Spang F41206-TC or Siemens B64290-K45-X27 or X830 or Ferroxcube 768T188-38 N_S = 80, N_P = 1
T2	Same core as T1 $N_S = N_P$ = 15 bifilar
T3	Core: Ferroxcube 4229-3C8 Pri. 44 Turns #18 Litz wire Sec. 4 Turns of copper strip Aux. 2 Turns #24 AWG
U2	MOC8102
U3	TL431

PHYSICAL DIMENSIONS inches (millimeters)

Package: P20
20-Pin PDIP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4819CP	0°C to 70°C	Molded DIP (P20)
ML4819CS (Obsolete)	**0°C to 70°C**	**Molded SOIC (S20)**

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