

# IC for System Reset (with built-in watchdog timer) Monolithic IC MM1136

March 27, 2000

## Outline

These ICs were developed to drive low voltage batteries, and have a watchdog timer with built-in microcomputer reset voltage detection circuit and low battery detection circuit.

A single reference voltage is used for low battery voltage detection and microcomputer reset voltage detection, so detection voltage difference is uniform ( $\approx 0.2V$ ). Further, there is a built-in watchdog timer for operation diagnosis, which prevents the system from running wild by generating an intermittent reset pulse during system mis-operation.

## Features

1. Accurate voltage drop detection voltage
  1. Low battery detection                      3.4V $\pm$ 3%
  2. Power supply voltage detection        3.2V $\pm$ 3%
  3. Detection voltage error                0.2V $\pm$ 20mV    1-2
  4. Hysteresis Both                         50mV typ.
2. Watchdog function stop pin (can be made to function only as reset IC during V<sub>CC</sub> rise)
3. Low current consumption                150 $\mu$ A typ.

## Package

SOP-8C (MM1136XF)

## Applications

1. 3V cordless telephones
2. Various types of small, handy equipment

## Series Table

Model	V <sub>SLB</sub>	V <sub>SLR</sub>	T <sub>PR</sub>	T <sub>WD</sub>	T <sub>WR</sub>
MM1136	3.4V	3.2V	100ms	100ms	2ms

\*C<sub>T</sub>=0.02 $\mu$ F

T<sub>PR</sub> : Reset hold time during V<sub>CC</sub> rise

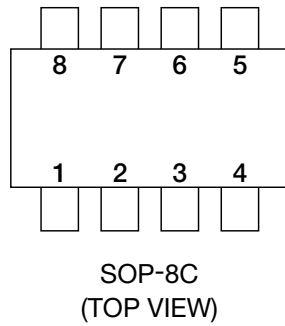
T<sub>WD</sub> : Timer monitoring time

T<sub>WR</sub> : Reset time

V<sub>SLB</sub> : Battery check detection voltage

V<sub>SLR</sub> : Reset detection voltage

Pin Assignment

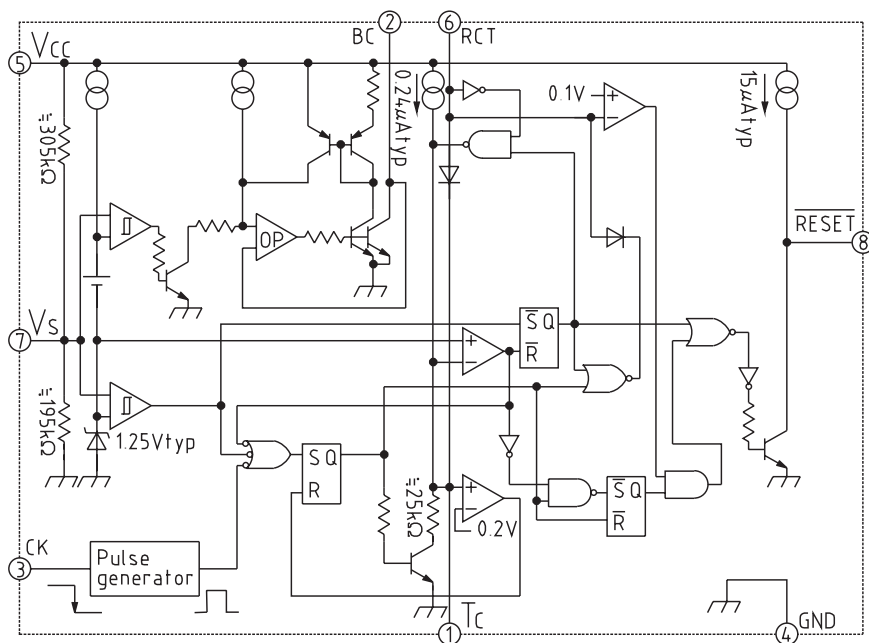


1	TC
2	BC (RESET)
3	CK
4	GND
5	V <sub>CC</sub>
6	RCT
7	V <sub>S</sub>
8	RESET

Pin Description

Pin No.	Pin name	Function
1	TC	T <sub>WD</sub> , T <sub>WR</sub> , T <sub>PR</sub> time setting pins.
2	BC (RESET)	Battery check output pin (RESET low level output) for 3.4V
3	CK	Clock input pin
4	GND	GND pin
5	V <sub>CC</sub>	Power supply voltage input pin
6	RCT	Watchdog timer stop pin Operation → OPEN, Stop → connect to GND
7	V <sub>S</sub>	Detection voltage fine adjustment pin
8	RESET	Reset output pin (low output)

Block Diagram



## Absolute Maximum Ratings


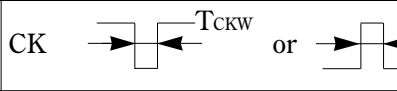
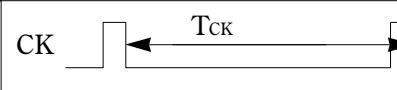
Item	Symbol	Rating	Units
Power supply voltage	V <sub>CC</sub> max.	-0.3~+7	V
Voltage applied to input pin	V <sub>IN</sub>	-0.3~V <sub>CC</sub> +0.3 (≦ +7)	V
Voltage applied to output pin	V <sub>OUT</sub>	-0.3~V <sub>CC</sub> +0.3 (≦ +7)	V
Allowable loss	P <sub>d</sub>	450	mW
Storage temperature	T <sub>STG</sub>	-40~+125	°C

## Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	V <sub>CC</sub>	+2.5~+6.5	V
RESET sync current	I <sub>OLR</sub>	0~1.5	mA
BC sync current	I <sub>OLC</sub>	0~1.5	mA
Clock input high level voltage	V <sub>CKH</sub>	1.4<	V
Clock input low level voltage	V <sub>CKL</sub>	<0.4	V
Clock monitoring time setting	T <sub>WD</sub>	1~1000	ms
Clock rise and fall times	t <sub>RCK</sub> , t <sub>FCK</sub>	<100	μs
Power supply voltage rise times	t <sub>RVCC</sub>	100<	μs
Power supply voltage fall times	t <sub>FVCC</sub>	50<	μs
TC pin capacitance	C <sub>T</sub>	0.002~2	μF
Operating temperature	T <sub>OP</sub>	-25~+75	°C

**Electrical Characteristics** (Except where noted otherwise, Ta=25°C, Vcc=3.8V)  
 (Except where noted otherwise, resistance unit is Ω)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Consumption current	I <sub>CC</sub>	No load		200	280	μA
RESET detection voltage	V <sub>SLR</sub>	V <sub>CC</sub> : High→Low R <sub>CT</sub> : GND, V <sub>TC</sub> =OPEN	3.10	3.20	3.30	V
Detection voltage temperature coefficient R	$\frac{\Delta V_{SR}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage R	V <sub>HYSR</sub>	V <sub>CC</sub> : Low→High R <sub>CT</sub> : GND, V <sub>TC</sub> =OPEN	25	50	100	mV
BC detection voltage	V <sub>SLB</sub>	V <sub>CC</sub> : High→Low, R <sub>LB</sub> =10k	3.30	3.40	3.50	V
Detection voltage temperature coefficient B	$\frac{\Delta V_{SB}}{\Delta T}$			±0.01	±0.05	%/°C
Hysteresis voltage B	V <sub>HYSB</sub>	V <sub>CC</sub> : Low→High, R <sub>LB</sub> =10k	25	50	100	mV
Detection voltage difference	$\Delta V_{SL}$	$\Delta V_{SL}=V_{SLB}-V_{SLR}$	0.18	0.20	0.22	V
CK input threshold	V <sub>TH</sub>		0.8	1.2	2	V
CK input current	I <sub>IH</sub>	V <sub>CK</sub> =3.8V		0	1	μA
	I <sub>IL</sub>	V <sub>CK</sub> =0.0V	-15	-6	-2	
Output voltage RH	V <sub>OHR</sub>	I <sub>RESET</sub> =-5μA	3.0	3.4		V
Output voltage BH	V <sub>OHB</sub>	R <sub>LB</sub> =10k	3.2	3.6		V
Output voltage RL	V <sub>OLR</sub>	I <sub>RESET</sub> =1mA, V <sub>CC</sub> =3.0V		0.3	0.5	V
Output voltage BL	V <sub>OLB</sub>	I <sub>BC</sub> =5mA, V <sub>CC</sub> =3.0V		0.3	0.5	V
Output sync current R	I <sub>OLR</sub>	V <sub>RESET</sub> =0.5V, V <sub>CC</sub> =3.0V	1	2		mA
Output sync current B	I <sub>OLB</sub>	V <sub>BC</sub> =0.5V, V <sub>CC</sub> =3.0V	5	10		mA
Output source current R	I <sub>OHR</sub>	V <sub>RESET</sub> =3.4V	8	15		μA
C <sub>T</sub> charge current	I <sub>CT1</sub>	V <sub>TC</sub> =1.0V during watchdog timer operation	-0.48	-0.24	-0.16	μA
	I <sub>CT2</sub>	V <sub>TC</sub> =1.0V during power ON reset operation	-0.48	-0.24	-0.16	μA
Minimum operating power supply voltage to ensure $\overline{\text{RESET}}$	V <sub>CC</sub>	V <sub>RESET</sub> =0.4V I <sub>RESET</sub> =0.1mA		0.8	1.0	V

V <sub>CC</sub> input pulse width	T <sub>PI</sub>	V <sub>CC</sub> 	8			μs
CK input pulse width	T <sub>CKW</sub>	CK 	3			μs
CK input cycle	T <sub>CK</sub>	CK 	20			μs
Watchdog timer monitoring time *1	T <sub>WD</sub>	C <sub>T</sub> =0.02μF	50	100	150	ms
Watchdog timer reset time *2	T <sub>WR</sub>	C <sub>T</sub> =0.02μF	1	2	3	ms
Reset hold time for power supply rise *3	T <sub>PR</sub>	C <sub>T</sub> =0.02μF	50	100	150	ms
RESET delay time	t <sub>PDR</sub>	V <sub>CC</sub> : High → Low, R <sub>LR</sub> =10k, C <sub>LR</sub> =15pF		10		μs
BC delay time	t <sub>PDB</sub>	V <sub>CC</sub> : High → Low, R <sub>LB</sub> =4.7k, C <sub>LB</sub> =15pF		10		μs
RESET rise time	t <sub>RR</sub>	R <sub>LR</sub> =10k, C <sub>LR</sub> =15pF		10		μs
RESET fall time	t <sub>FR</sub>	R <sub>LR</sub> =10k, C <sub>LR</sub> =15pF		2		μs
BC rise time	t <sub>RB</sub>	R <sub>LB</sub> =4.7k, C <sub>LB</sub> =15pF		10		μs
BC fall time	t <sub>FB</sub>	R <sub>LB</sub> =4.7k, C <sub>LB</sub> =15pF		2		μs

Notes:

\*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output.

In other words, reset output is output if a clock pulse is not input during this time.

\*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

\*3 Reset hold time is the time from when V<sub>CC</sub> exceeds detection voltage (V<sub>SHR</sub>) during power ON reset until reset release (RESET output high).

\*4 Watchdog timer monitoring time (T<sub>WD</sub>), watchdog timer reset time (T<sub>WR</sub>) and reset hold time (T<sub>PR</sub>) during power supply rise can be changed by varying C<sub>T</sub> capacitance. The times are expressed by the following formulae.

$$T_{PR} \text{ (ms)} \cong 5000 \times C_T \text{ (}\mu\text{F)}$$

$$T_{WD} \text{ (ms)} \cong 5000 \times C_T \text{ (}\mu\text{F)}$$

$$T_{WR} \text{ (ms)} \cong 100 \times C_T \text{ (}\mu\text{F)}$$

Example : When C<sub>T</sub>=0.02μF

$$T_{PR} \cong 100\text{ms}$$

$$T_{WD} \cong 100\text{ms}$$

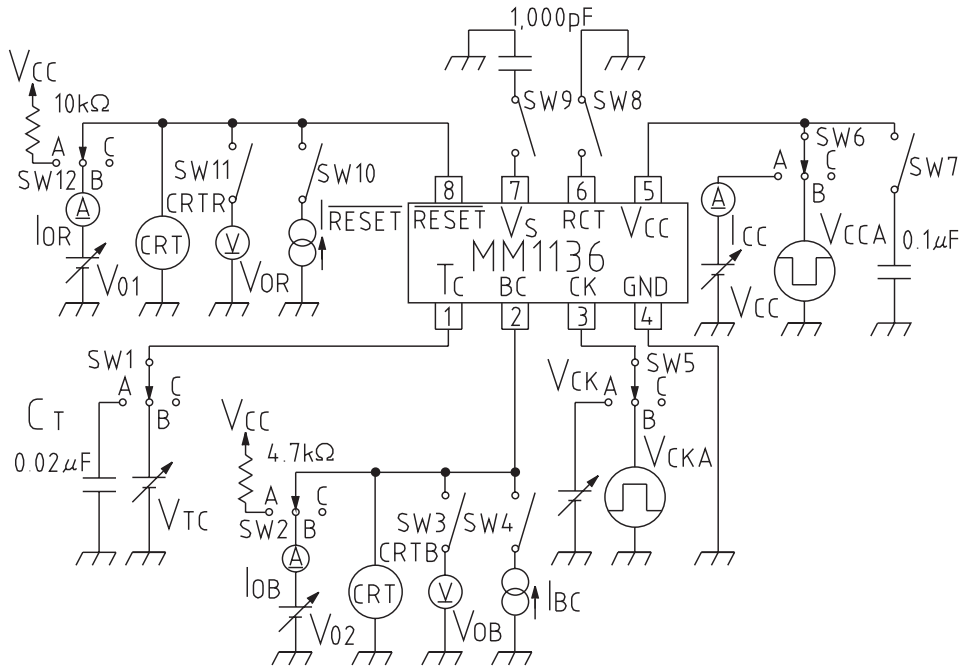
$$T_{WR} \cong 2\text{ms}$$

\*5 T<sub>WD</sub> can be varied by placing a resistor (1MEGΩ or more) between the RCT pin and V<sub>CC</sub>.

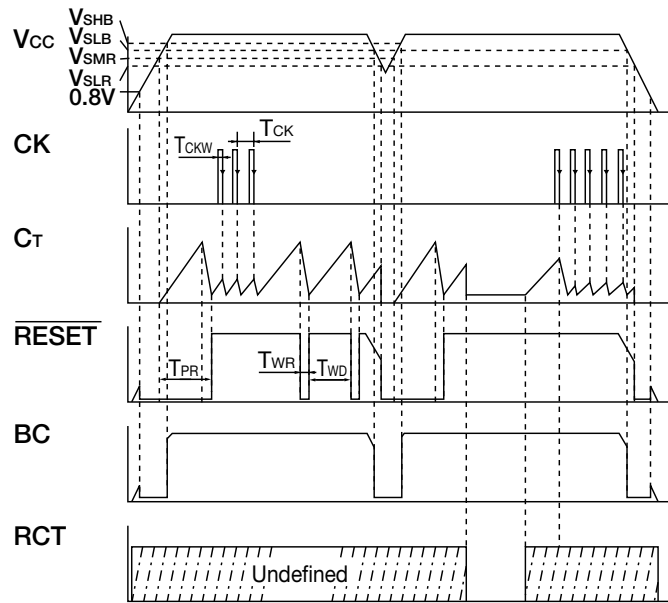
\*6 The voltage range when measuring output rise and fall time is 10~90%.

\*7 V<sub>CC</sub> rise time should be 100μs or more, and fall time should be 50μs or more.

Measuring Circuit



Timing Chart



Basic Circuit Diagram

