National Semiconductor

February 1988

# MM54C157/MM74C157 Quad 2-Input Multiplexers

## General Description

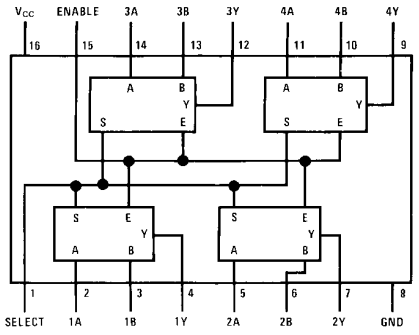
These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical ''0'' the four outputs assume the values as selected from the inputs. When the enable input is at logical ''1'', the outputs assume logical ''0''. Select decoding is done internally resulting in a single select input only.

## Features

| | |
|---|---|
| ■ Supply voltage range | 3V to 15V |
| ■ High noise immunity | 0.45 $V_{CC}$ (typ.) |
| ■ Low power | 50 nW (typ.) |
| ■ Tenth power TTL compatible | Drive 2 LPTTL loads |

## Logic & Connection Diagrams

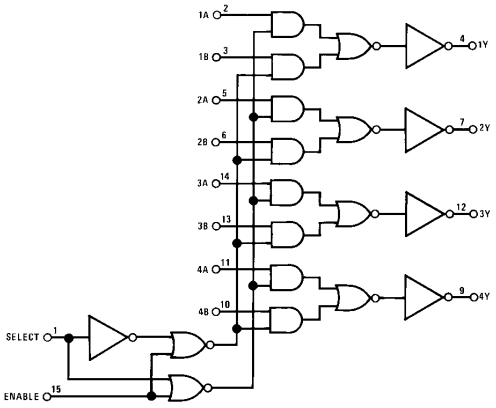
**Dual-In-Line Package**




TL/F/5894–2

**Top View**

**Order Number MM54C157 or MM74C157**

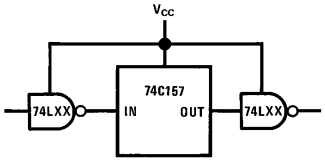



TL/F/5894–1

## Truth Table

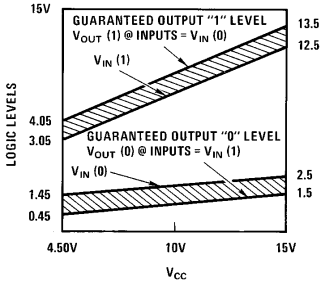
| Enable | Select | A | B | Output Y |
|---|---|---|---|---|
| 1 | X | X | X | 0 |
| 0 | 0 | 0 | X | 0 |
| 0 | 0 | 1 | X | 1 |
| 0 | 1 | X | 0 | 0 |
| 0 | 1 | X | 1 | 1 |

**74L Compatibility**




TL/F/5894–3

**Guaranteed Noise Margin as a Function of $V_{CC}$**




TL/F/5894–4

RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at Any Pin | $-0.3V$ to $V_{CC} + 0.3V$ |
| Operating Temperature Range | |
| MM54C157 | $-55°C$ to $+125°C$ |
| MM74C157 | $-40°C$ to $+85°C$ |
| Storage Temperature Range | $-65°C$ to $+150°C$ |
| Maximum $V_{CC}$ Voltage | 18V |
| Power Dissipation ($P_D$) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Operating $V_{CC}$ Range | 3V to 15V |
| Lead Temperature (Soldering, 10 sec.) | 260°C |

## DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 3.5<br>8.0 | | | V<br>V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | | 1.5<br>2.0 | V<br>V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | 4.5<br>9.0 | | | V<br>V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | | 0.5<br>1.0 | V<br>V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC} = 15V$ | | 0.005 | 1.0 | $\mu A$ |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC} = 15V$ | $-1.0$ | $-0.005$ | | $\mu A$ |
| $I_{CC}$ | Supply Current | $V_{CC} = 15V$ | | 0.05 | 60 | $\mu A$ |
| **CMOS TO TENTH POWER INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | 54C $V_{CC} = 4.5V$<br>74C $V_{CC} = 4.75V$ | $V_{CC} - 1.5$<br>$V_{CC} - 1.5$ | | | V<br>V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | 54C $V_{CC} = 4.5V$<br>74C $V_{CC} = 4.75V$ | | | 0.8<br>0.8 | V<br>V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage | 54C $V_{CC} = 4.5V$, $I_O = -360\ \mu A$<br>74C $V_{CC} = 4.75V$, $I_O = -360\ \mu A$ | 2.4<br>2.4 | | | V<br>V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | 54C $V_{CC} = 4.5V$, $I_O = 360\ \mu A$<br>74C $V_{CC} = 4.75V$, $I_O = 360\ \mu A$ | | | 0.4<br>0.4 | V<br>V |
| **OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)** | | | | | | |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 5V$, $V_{IN(0)} = 0V$<br>$T_A = 25°C$, $V_{OUT} = 0V$ | $-1.75$ | | | mA |
| $I_{SOURCE}$ | Output Source Current | $V_{CC} = 10V$, $V_{IN(0)} = 0V$<br>$T_A = 25°C$, $V_{OUT} = 0V$ | $-8.0$ | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC} = 5V$, $V_{IN(1)} = 5V$<br>$T_A = 25°C$, $V_{OUT} = V_{CC}$ | 1.75 | | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{CC} = 10V$, $V_{IN(1)} = 10V$<br>$T_A = 25°C$, $V_{OUT} = V_{CC}$ | 8.0 | | | mA |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

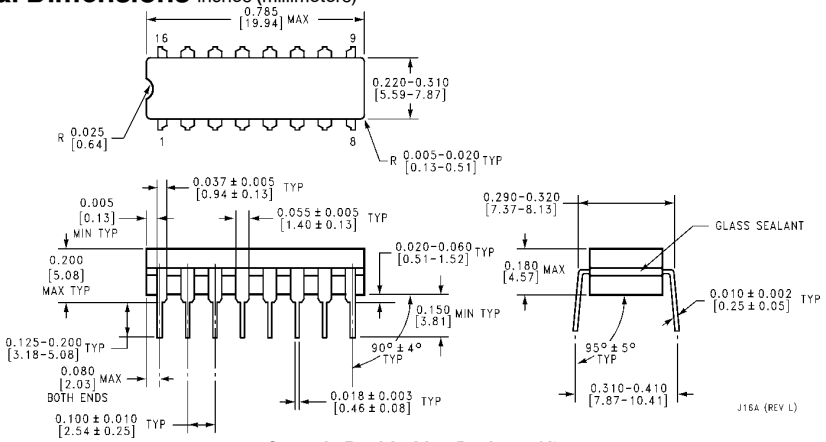
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay from Data to Output | $V_{CC} = 5.0V$<br>$V_{CC} = 10V$ | | 150<br>70 | 250<br>110 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay from Select to Output | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 180<br>80 | 300<br>130 | ns<br>ns |
| $t_{pd0}$, $t_{pd1}$ | Propagation Delay from Enable to Output | $V_{CC} = 5V$<br>$V_{CC} = 10V$ | | 180<br>80 | 300<br>130 | ns<br>ns |
| $C_{IN}$ | Input Capacitance | (Note 2) | | 5 | | pF |
| $C_{PD}$ | Power Dissipation Capacitance | (Note 3) | | 20 | | pF |

*AC Parameters are guaranteed by DC correlated testing.

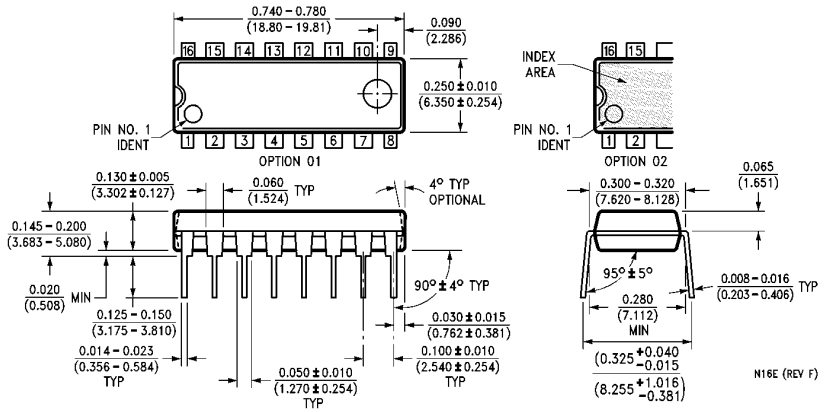
**Note 2:** Capacitance is guaranteed by periodic testing.

**Note 3:** $C_{PD}$ determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

## Physical Dimensions inches (millimeters)




**Ceramic Dual-In-Line Package (J)**
**Order Number MM54C157J or MM74C157J**
**NS Package Number J16A**




**Molded Dual-In-Line Package (N)**
**Order Number MM54C157N or MM74C157N**
**NS Package Number N16E**

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**National Semiconductor Corporation**
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

**National Semiconductor Europe**
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

**National Semiconductor Hong Kong Ltd.**
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

**National Semiconductor Japan Ltd.**
Tel: 81-043-299-2309
Fax: 81-043-299-2408