

## MM54C175/MM74C175 Quad D Flip-Flop

### General Description

The MM54C175/MM74C175 consists of four positive-edge triggered D type flip-flops implemented with monolithic CMOS technology. Both true and complemented outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

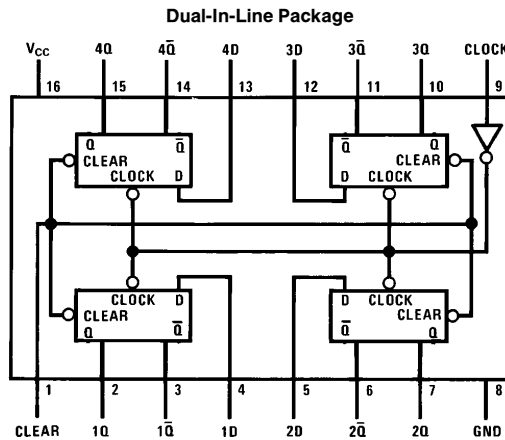
All inputs are protected from static discharge by diode clamps to  $V_{CC}$  and GND.

### Features

- Wide supply voltage range
- Guaranteed noise margin
- High noise immunity
- Low power TTL compatibility

3V to 15V  
1.0V  
0.45  $V_{CC}$  (typ.)  
Fan out of 2  
driving 74L

### Connection Diagram & Truth Table



TL/F/5900-1

Order Number MM54C175 or MM74C175

#### Each Flip-Flop

Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level  
L = Low level  
X = Irrelevant  
 $\uparrow$  = Transition from low to high level  
NC = No change

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin	-0.3V to $V_{CC}$ + 0.3V
Operating Temperature Range	
MM54C175	-55°C to +125°C
MM74C175	-40°C to +85°C

Storage Temperature Range	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating $V_{CC}$ Range	3V to 15V
Absolute Maximum $V_{CC}$	18V
Lead Temperature (Soldering, 10 seconds)	260°C

**DC Electrical Characteristics** Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>CMOS TO CMOS</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10 \mu A$ $V_{CC} = 10V, I_O = -10 \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10 \mu A$ $V_{CC} = 10V, I_O = 10 \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	$\mu A$
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		$\mu A$
$I_{CC}$	Supply Current	$V_{CC} = 15V$		0.05	300	$\mu A$
<b>CMOS/LPTTL INTERFACE</b>						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360 \mu A$ 74C, $V_{CC} = 4.75V, I_O = -360 \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360 \mu A$ 74C, $V_{CC} = 4.75V, I_O = 360 \mu A$			0.4 0.4	V V
<b>OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)</b>						
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 5V, T_A = 25^\circ C,$ $V_{OUT} = 0V$	-1.75	-3.3		mA
$I_{SOURCE}$	Output Source Current (P-Channel)	$V_{CC} = 10V, T_A = 25^\circ C,$ $V_{OUT} = 0V$	-8.0	-15		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 5V, T_A = 25^\circ C,$ $V_{OUT} = V_{CC}$	1.75	3.6		mA
$I_{SINK}$	Output Sink Current (N-Channel)	$V_{CC} = 10V, T_A = 25^\circ C,$ $V_{OUT} = V_{CC}$	8.0	16		mA

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

## AC Electrical Characteristics\* $T_A = 25^\circ\text{C}$ , $C_L = 50\text{ pF}$ , unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd}$	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\bar{Q}$	$V_{CC} = 5\text{V}$		190	300	ns
		$V_{CC} = 10\text{V}$		75	110	ns
$t_{pd}$	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		180 70	300 110	ns ns
$t_{pd}$	Propagation Delay Time to a Logical "1" from Clear to Q	$V_{CC} = 5\text{V}$ $V_{CC} = 10\text{V}$		230 90	400 150	ns ns
$t_S$	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5\text{V}$	100	45		ns
		$V_{CC} = 10\text{V}$	40	16		ns
$t_H$	Time After Clock Pulse that Data Must be Held	$V_{CC} = 5\text{V}$	0	-11		ns
		$V_{CC} = 10\text{V}$	0	-4		ns
$t_W$	Minimum Clock Pulse Width	$V_{CC} = 5.0\text{V}$		130	250	ns
		$V_{CC} = 10\text{V}$		45	100	ns
$t_W$	Minimum Clear Pulse Width	$V_{CC} = 5.0\text{V}$		120	250	ns
		$V_{CC} = 10\text{V}$		45	100	ns
$t_r$	Maximum Clock Rise Time	$V_{CC} = 5\text{V}$	15	450		$\mu\text{s}$
		$V_{CC} = 10\text{V}$	5.0	125		$\mu\text{s}$
$t_f$	Maximum Clock Fall Time	$V_{CC} = 5\text{V}$	15	50		$\mu\text{s}$
		$V_{CC} = 10\text{V}$	5.0	50		$\mu\text{s}$
$f_{MAX}$	Maximum Clock Frequency	$V_{CC} = 5\text{V}$	2.0	3.5		MHz
		$V_{CC} = 10\text{V}$	5.0	10		MHz
$C_{IN}$	Input Capacitance	Clear Input (Note 2)		10		pF
		Any Other Input		5.0		pF
$C_{PD}$	Power Dissipation Capacitance	Per Package (Note 3)		130		pF

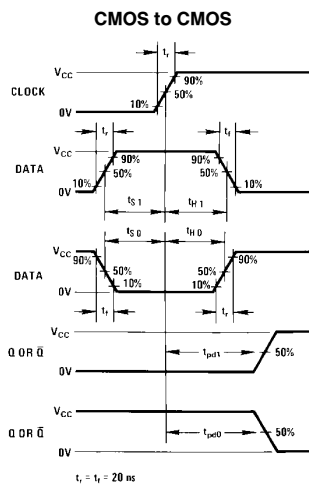
\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** Capacitance is guaranteed by periodic testing.

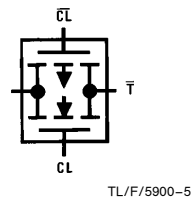
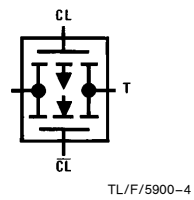
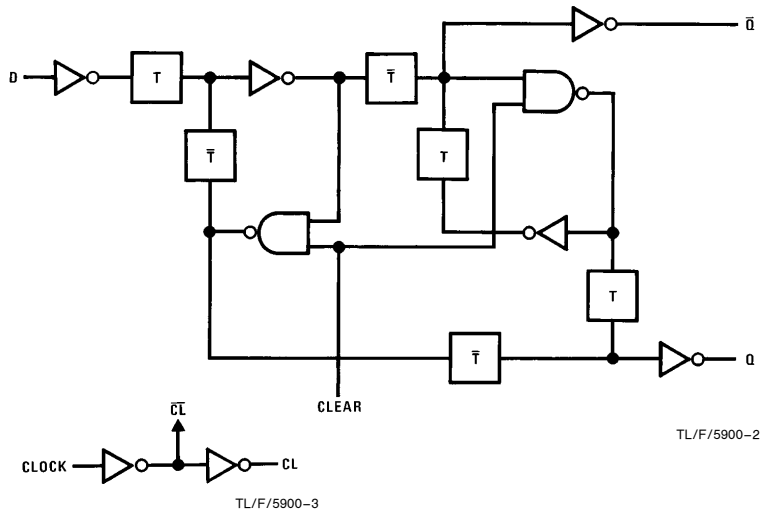
**Note 3:**  $C_{PD}$  determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

## Switching Time Waveforms

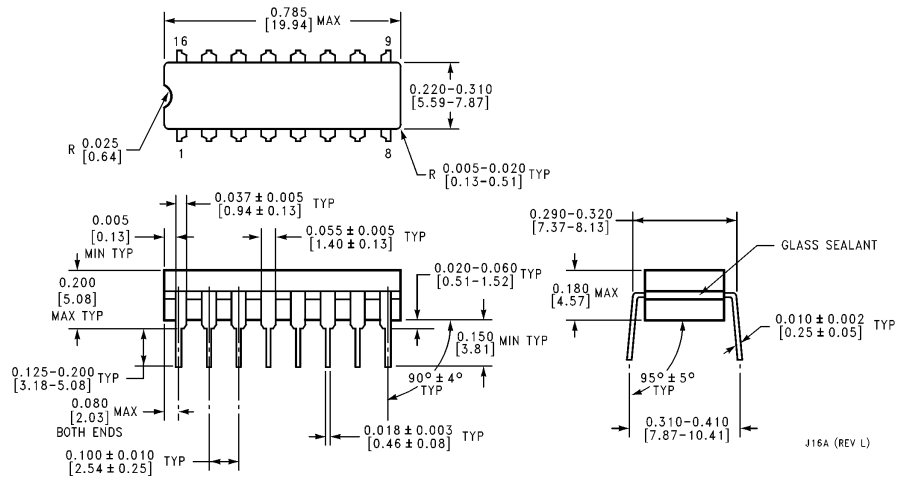


# Logic Diagram

Typical One of Four

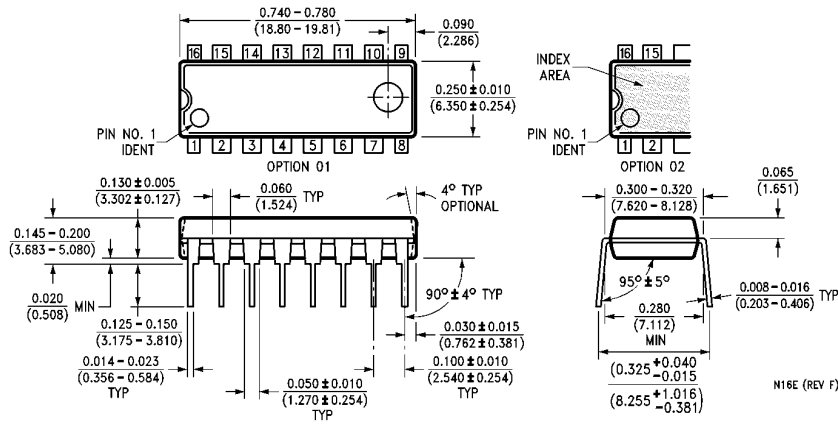


**Physical Dimensions** inches (millimeters)



**Ceramic Dual-In-Line Package (J)**  
**Order Number MM54C175J or MM74C175J**  
**NS Package Number J16A**

**Physical Dimensions** inches (millimeters) (Continued)



**Molded Dual-In-Line Package (N)**  
**Order Number MM54C175N or MM74C175N**  
**NS Package Number N16E**

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