National Semiconductor

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# MM54HC242/MM74HC242 Inverting Quad TRI-STATE® Transceiver MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

## General Description

These TRI-STATE bidirectional inverting and non-inverting buffers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances. These circuits possess the low power dissipation and high noise immunity associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LS-TTL loads.

The MM54HC243/MM74HC243 is a non-inverting buffer and the MM54HC242/MM74HC242 is an inverting buffer. Each device has one active high enable (GBA), and one active low enable ($\overline{G}$AB). GBA enables the A outputs and $\overline{G}$AB enables the B outputs. This device does not have Schmitt trigger inputs.

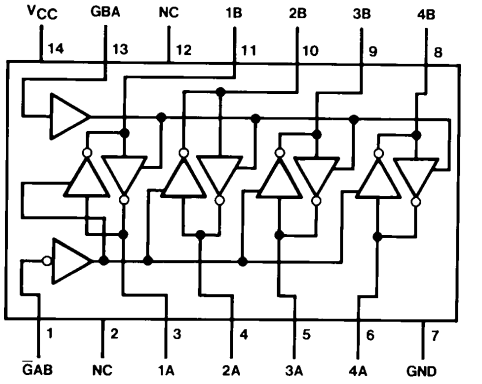
All inputs are protected from damage due to static discharge by diodes to $V_{CC}$ and ground.

## Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs
- Two way asynchronous communication
- High output current: 6 mA (74HC)
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 $\mu$A (74HC)

## Connection Diagrams

**Dual-In-Line Package**

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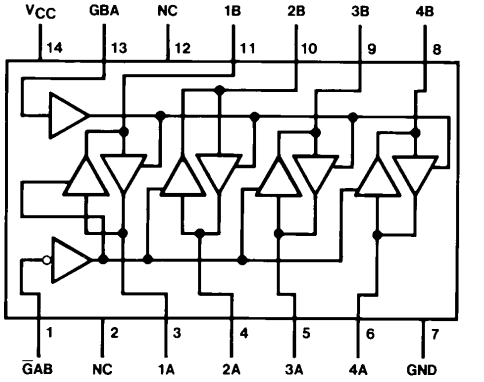
**Top View**
**Order Number MM54HC242 or MM74HC242**

**Dual-In-Line Package**

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**Top View**
**Order Number MM54HC243 or MM74HC243**

## Truth Tables

**'HC242**

| Control Inputs | | Data Port Status | |
|---|---|---|---|
| $\overline{G}$AB | GBA | A | B |
| H | H | $\overline{\text{OUTPUT}}$ | Input |
| L | H | Isolated | Isolated |
| H | L | Isolated | Isolated |
| L | L | Input | $\overline{\text{OUTPUT}}$ |

**'HC243**

| Control Inputs | | Data Port Status | |
|---|---|---|---|
| $\overline{G}$AB | GBA | A | B |
| H | H | OUTPUT | Input |
| L | H | Isolated | Isolated |
| H | L | Isolated | Isolated |
| L | L | Input | OUTPUT |

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## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5 to +7.0V |
| DC Input Voltage ($V_{IN}$) | −1.5 to $V_{CC}$ +1.5V |
| DC Output Voltage ($V_{OUT}$) | −0.5 to $V_{CC}$ +0.5V |
| Clamp Diode Current ($I_{IK}$, $I_{OK}$) | ±20 mA |
| DC Output Current, per pin ($I_{OUT}$) | ±35 mA |
| DC $V_{CC}$ or GND Current, per pin ($I_{CC}$) | ±70 mA |
| Storage Temperature Range ($T_{STG}$) | −65°C to +150°C |
| Power Dissipation ($P_D$) | |
| (Note 3) | 600 mW |
| S.O. Package only | 500 mW |
| Lead Temp. ($T_L$) (Soldering 10 seconds) | 260°C |

## Operating Conditions

| | | Min | Max | Units |
|---|---|---|---|---|
| Supply Voltage ($V_{CC}$) | | 2 | 6 | V |
| DC Input or Output Voltage ($V_{IN}$, $V_{OUT}$) | | 0 | $V_{CC}$ | V |
| Operating Temp. Range ($T_A$) | | | | |
| MM74HC | | −40 | +85 | °C |
| MM54HC | | −55 | +125 | °C |
| Input Rise or Fall Times | | | | |
| ($t_r$, $t_f$) | $V_{CC}$ = 2.0V | | 1000 | ns |
| | $V_{CC}$ = 4.5V | | 500 | ns |
| | $V_{CC}$ = 6.0V | | 400 | ns |

## DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = 25°C | 74HC $T_A$ = −40 to 85°C | 54HC $T_A$ = −55 to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $V_{IH}$ | Minimum High Level Input Voltage | | 2.0V | | 1.5 | 1.5 | V |
| | | | 4.5V | | 3.15 | 3.15 | V |
| | | | 6.0V | | 4.2 | 4.2 | V |
| $V_{IL}$ | Maximum Low Level Input Voltage** | | 2.0V | | 0.5 | 0.5 | V |
| | | | 4.5V | | 1.35 | 1.35 | V |
| | | | 6.0V | | 1.8 | 1.8 | V |
| $V_{OH}$ | Minimum High Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $\|I_{OUT}\| \leq$ 20 μA | 2.0V | 2.0 | 1.9 | 1.9 | V |
| | | | 4.5V | 4.5 | 4.4 | 4.4 | V |
| | | | 6.0V | 6.0 | 5.9 | 5.9 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $\|I_{OUT}\| \leq$ 6.0 mA | 4.5V | 4.2 | 3.98 | 3.84 | 3.7 V |
| | | $\|I_{OUT}\| \leq$ 7.8 mA | 6.0V | 5.7 | 5.48 | 5.34 | 5.2 V |
| $V_{OL}$ | Maximum Low Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $\|I_{OUT}\| \leq$ 20 μA | 2.0V | 0 | 0.1 | 0.1 | 0.1 V |
| | | | 4.5V | 0 | 0.1 | 0.1 | 0.1 V |
| | | | 6.0V | 0 | 0.1 | 0.1 | 0.1 V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $\|I_{OUT}\| \leq$ 6.0 mA | 4.5V | 0.2 | 0.26 | 0.33 | 0.4 V |
| | | $\|I_{OUT}\| \leq$ 7.8 mA | 6.0V | 0.2 | 0.26 | 0.33 | 0.4 V |
| $I_{IN}$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$ or GND | 6.0V | | ±0.1 | ±1.0 | ±1.0 μA |
| $I_{OZ}$ | Maximum TRI-STATE Output Leakage Current | $V_{OUT}$ = $V_{CC}$ or GND $\overline{G}AB$ = $V_{IH}$, GBA = $V_{IL}$ | 6.0V | | ±0.5 | ±5.0 | ±10 μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN}$ = $V_{CC}$ or GND $I_{OUT}$ = 0 μA | 6.0V | | 8.0 | 80 | 160 μA |

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5V and 4.5V respectively. (The $V_{IH}$ value at 5.5V is 3.85V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**$V_{IL}$ limits are currently tested at 20% of $V_{CC}$. The above $V_{IL}$ specification (30% of $V_{CC}$) will be implemented no later than Q1, CY'89.

## AC Electrical Characteristics (MM54HC242/MM74HC242)

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
|---|---|---|---|---|---|
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | $C_L=45$ pF | 12 | 18 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Output Enable Time to Active Output | $R_L=1k\Omega$ $C_L=45$ pF | 17 | 28 | ns |
| $t_{PHZ}$, $t_{PHL}$ | Maximum Output Disable Time from Active Output | $R_L=1\ k\Omega$ $C_L=5$ pF | 15 | 25 | ns |

## AC Electrical Characteristics (MM54HC242/MM74HC242, MM54HC243/MM74HC243)

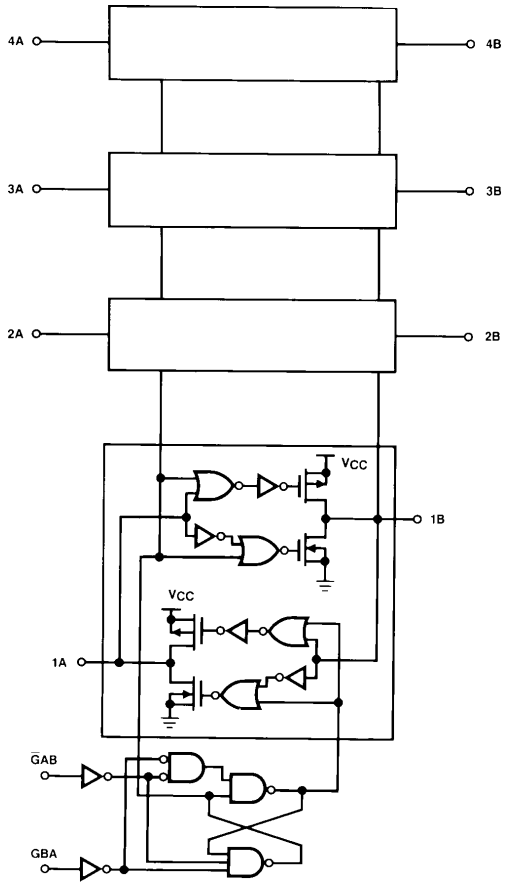
$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A=25°C$ | 74HC $T_A=-40$ to 85°C | 54HC $T_A=-55$ to 125°C | Units |
|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | |
| $t_{PHL}$, $t_{PLH}$ | Maximum Propagation Delay | $C_L=50$ pF | 2.0V | 55 | 100 | 126 | 149 | ns |
| | | $C_L=150$ pF | 2.0V | 80 | 150 | 190 | 224 | ns |
| | | $C_L=50$ pF | 4.5V | 12 | 20 | 25 | 30 | ns |
| | | $C_L=150$ pF | 4.5V | 22 | 30 | 38 | 45 | ns |
| | | $C_L=50$ pF | 6.0V | 11 | 17 | 21 | 25 | ns |
| | | $C_L=150$ pF | 6.0V | 18 | 26 | 32 | 38 | ns |
| $t_{PZH}$, $t_{PZL}$ | Maximum Output Enable Time to Active Output | $R_L=1\ k\Omega$ | | | | | | |
| | | $C_L=50$ pF | 2.0V | 75 | 150 | 189 | 224 | ns |
| | | $C_L=150$ pF | 2.0V | 100 | 200 | 252 | 298 | ns |
| | | $C_L=50$ pF | 4.5V | 15 | 30 | 38 | 45 | ns |
| | | $C_L=150$ pF | 4.5V | 30 | 40 | 50 | 60 | ns |
| | | $C_L=50$ pF | 6.0V | 13 | 26 | 32 | 38 | ns |
| | | $C_L=150$ pF | 6.0V | 17 | 34 | 43 | 51 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Maximum Output Disable Time from Active Output | $R_L=1\ k\Omega$ $C_L=50$ pF | 2.0V | 75 | 150 | 189 | 224 | ns |
| | | | 4.5V | 15 | 30 | 38 | 45 | ns |
| | | | 6.0V | 13 | 26 | 32 | 38 | ns |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Rise and Fall Time | | 2.0V | | 60 | 75 | 90 | ns |
| | | | 4.5V | | 12 | 15 | 18 | ns |
| | | | 6.0V | | 10 | 13 | 15 | ns |
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | (per buffer) | | | | | | |
| | | Outputs Disabled | | 12 | | | | pF |
| | | Outputs Enabled | | 50 | | | | pF |
| $C_{IN}$ | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |
| $C_{OUT}$ | Maximum Output Capacitance | | | 10 | 20 | 20 | 20 | pF |

**Note 5:** $C_{PD}$ determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

## Logic Diagrams

**MM54HC242/MM74HC242**

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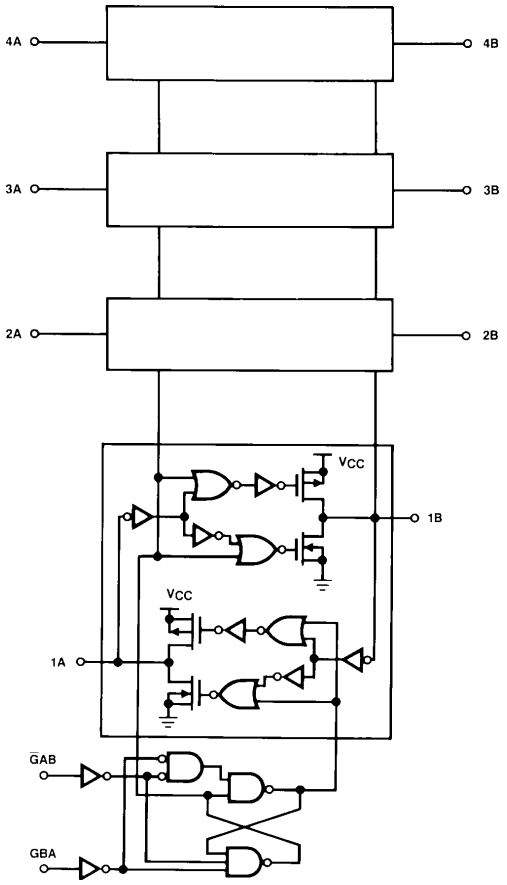
**MM54HC243/MM74HC243**

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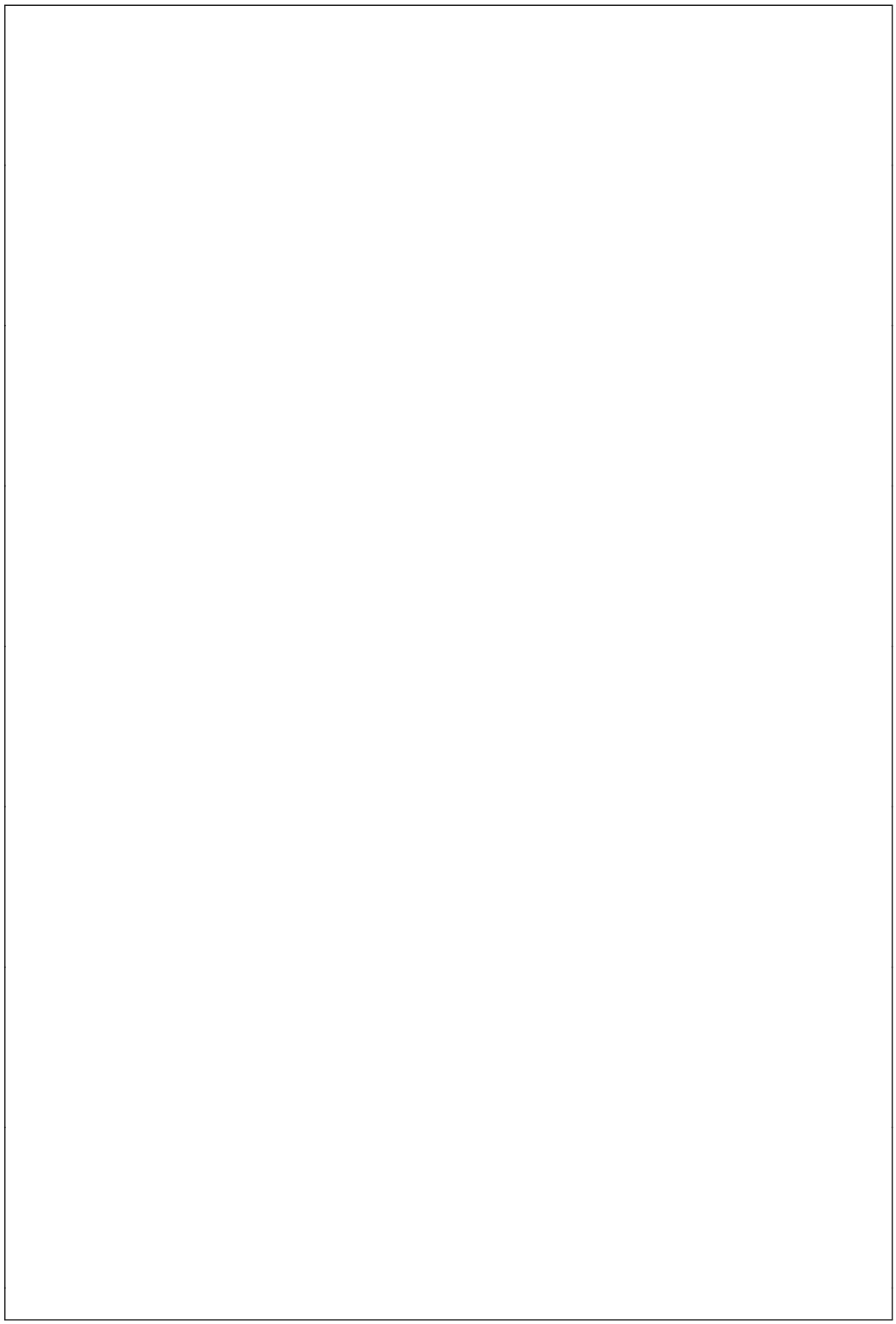
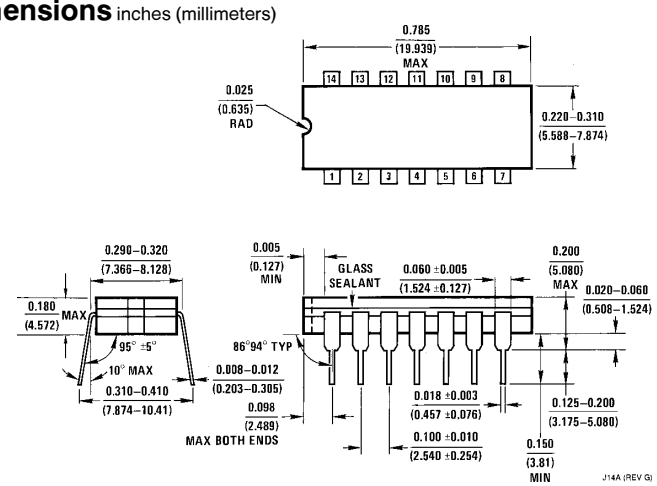
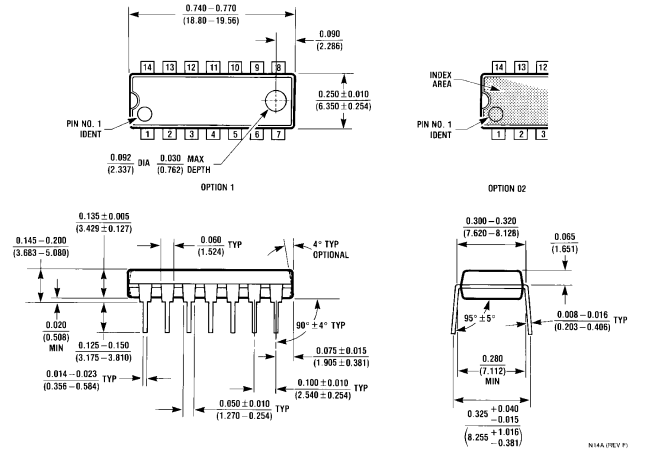


## Physical Dimensions inches (millimeters)




**Cavity Dual-In Line Package (J)**
**Order Number MM54HC242J, MM54HC243J, MM74HC242J or MM74HC243J**
**NS Package Number J14A**




**Molded Dual-In Line Package (N)**
**Order Number MM74HC242N or MM74HC243N**
**NS Package Number N14A**

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