

# 4BIT D-TYPE REGISTERS

## GENERAL DESCRIPTION

The MMC 4076 (intermediate or extended temperature range) are monolithic integrated circuit, available in 16-lead dual in-line plastic or ceramic package.

The MMC 4076 types are four-bit registers consisting of D-type flip-flops that feature three-state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

## FEATURES

- Three-state outputs
- Input disabled without gating the clock
- Gated output control lines for enabling or disabling the outputs.

## ABSOLUTE MAXIMUM RATINGS

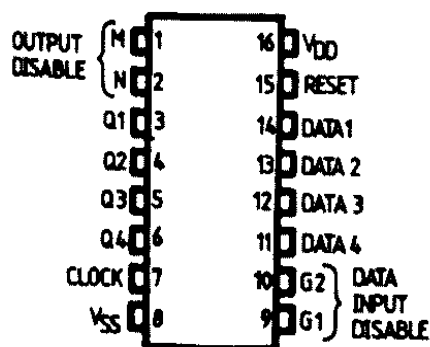
$V_{DD}^*$	Supply voltage: G and H types E and F types	-0.5 to 20 -0.5 to 18 -0.5 to $V_{DD}+0.5$	20 18 $V$	V
$V_i$	Input voltage	-0.5 to $V_{DD}+0.5$	$V$	V
$I_{i1}$	DC input current (any one input)		$\pm 10$	mA
$P_{tot}$	Total power dissipation (per package) Dissipation per output transistor for $T_A$ = full package-temperature range		200 100	mW mW
$T_A$	Operating temperature : G and H types E and F types	-55 to -40 to -65 to	125 85 150	$^{\circ}C$ $^{\circ}C$ $^{\circ}C$
$T_{stg}$	Storage temperature			

\* All voltage values are referred to  $V_{SS}$  pin voltage

## RECOMMENDED OPERATING CONDITIONS

$V_{DD}^*$	Supply voltage: G and H types E and F types	3 to 3 to	18 15	V V
$V_i$	Input voltage	0 to	$V_{DD}$	V
$T_A$	Operating temperature : G and H types E and F types	-55 to -40 to	125 85	$^{\circ}C$ $^{\circ}C$

## CONNECTION DIAGRAM



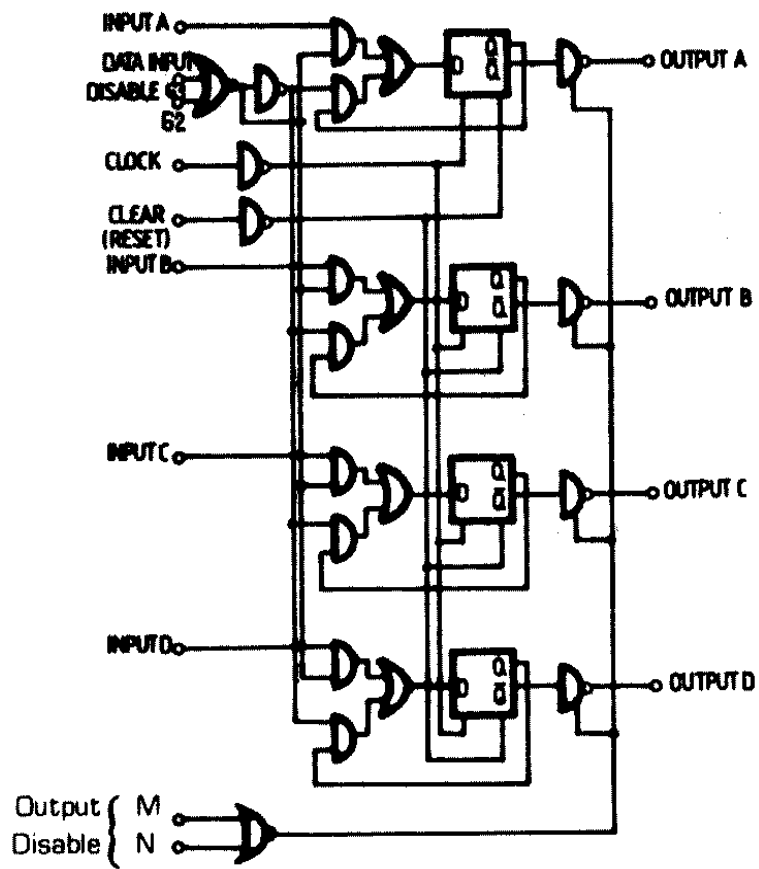
## TRUTH TABLE

Reset	Clock	Data Input Disable		Data	Next State Output	
		$G_1$	$G_2$	D	Q	
1	x	x	x	x	0	
0	0	x	x	x	Q	NC
0	0	1	x	x	Q	NC
0	0	x	1	x	Q	NC
0	0	0	0	1	1	
0	0	0	0	0	0	
0	1	x	x	x	Q	NC
0	1	x	x	x	Q	NC

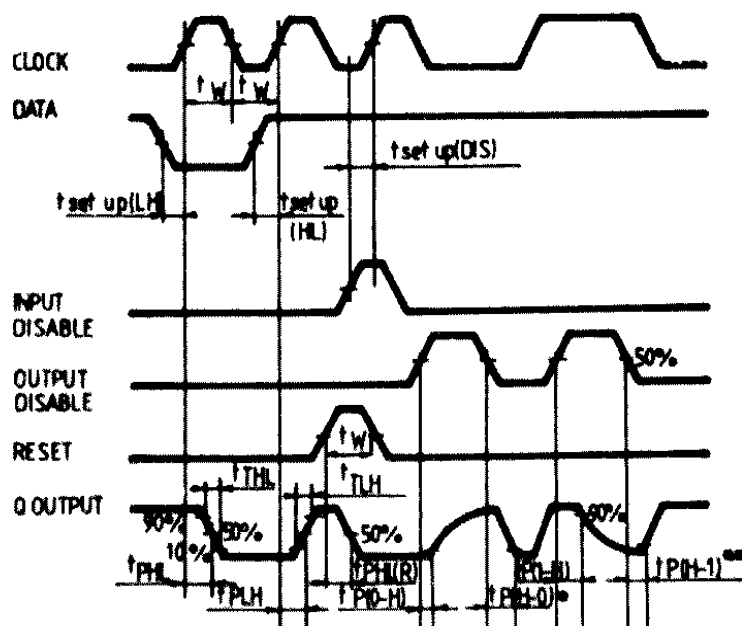
1 = High Level  
0 = Low Level

X = Don't Care  
NC = No Change

**LOGIC DIAGRAM**



**WAVEFORMS**



- \* Output tied to  $V_{DD}$  through 1 k $\Omega$
- \*\* Output tied to  $V_{SS}$  through 1 k $\Omega$

## STATIC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

PARAMETER		TEST CONDITIONS				VALUES						UNIT		
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>LOW</sub>		25°C			T <sub>HIGH</sub>			
						min.	max.	min.	typ	max.	min.		max.	
I <sub>L</sub>	Quiescent current	G, H types	0/ 5			5		5		0.04	5		150	$\mu$ A
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
	E, F types	0/ 5			5		20		0.04	20		150		
		0/10 0/15			10 15		40 80		0.04 0.04	40 80		300 600		
V <sub>OH</sub>	Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95		V	
		0/10		< 1	10	9.95		9.95			9.95			
		0/15		< 1	15	14.95		14.95			14.95			
V <sub>OL</sub>	Output low voltage	5 / 0		< 1	5		0.05			0.05		0.05	V	
		10/ 0		< 1	10		0.05			0.05		0.05		
		15/ 0		< 1	15		0.05			0.05		0.05		
V <sub>IH</sub>	Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
			1/9	< 1	10	7		7			7			
			1.5/13.5	< 1	15	11		11			11			
V <sub>IL</sub>	Input low voltage		4.5/0.5	< 1	5		1.5			1.5		1.5	V	
			9/1	< 1	10		3			3		3		
			13.5/1.5	< 1	15		4			4		4		
I <sub>OH</sub>	Output drive current	G, H types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15	mA	
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
	E, F types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1			
		0/ 5	4.6		5	-0.52		-0.44	-1		-0.36			
I <sub>OL</sub>	Output sink current	G, H types	0/ 5	0.4		5	0.64		0.51	1		0.36	mA	
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
			0/ 5	0.4		5	0.52		0.44	1		0.36		
	E, F types	0/10	0.5		10	1.3		1.1	2.6		0.9			
		0/15	1.5		15	3.6		3.0	6.8		2.4			
I <sub>IH</sub> , I <sub>IL</sub>	Input leakage current	G, H types	0/18	Any input		18		$\pm 0.1$		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$	$\mu$ A
		E, F types	0/15			15		$\pm 0.3$		$\pm 10^{-5}$	$\pm 0.3$		$\pm 1$	
I <sub>OH</sub>	3-state output	G, H types	0/18	0/18		18		$\pm 0.4$		$\pm 10^{-4}$	$\pm 0.4$		$\pm 12$	$\mu$ A
		E, F types	0/15	0/15		15		$\pm 1.0$		$\pm 10^{-4}$	$\pm 1.0$		$\pm 7.5$	

PARAMETER	TEST CONDITIONS				VALUES						UNIT	
	V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>O</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>LOW</sub> *		25°C			T <sub>HIGH</sub> *		
					Min.	Max.	Min.	Typ.	Max.	Min.		Max.
C <sub>I</sub> Input capacitance		Any input						5	7.5			pF

\* T<sub>LOW</sub> = -55°C for G, H devices; -40°C for E, F devices.

\* T<sub>HIGH</sub> = +125°C for G, H devices; +85°C for E, F devices.

The Noise Margin for both "1" and "0" level is:

1 V min. with V<sub>DD</sub> = 5 V

2 V min. with V<sub>DD</sub> = 10 V

2.5 V min. with V<sub>DD</sub> = 15 V

### DYNAMIC ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 kohm, typical temperature coefficient for all V<sub>DD</sub> values is 0.3%/°C, all input rise and fall times = 20 ns).

PARAMETER	TEST CONDITIONS	VALUES			UNIT	
		V <sub>DD</sub> (V)	min.	typ.		max.
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay time (clock to Q output)	5 10 15		300 125 90	600 250 180	ns
t <sub>PHL(R)</sub>	Propagation delay time (Reset)	5 10 15		230 100 75	460 200 150	ns
t <sub>PI1-HI</sub> t <sub>PI0-HI</sub>	3-state output 1 or 0 to high impedance	R <sub>L</sub> = 1 k $\Omega$ 5 10 15		150 75 60	300 150 120	ns
t <sub>PH-HI</sub> t <sub>PH-OI</sub>	3-state high impedance to 1 or 0 output	R <sub>L</sub> = 1 k $\Omega$ 5 10 15		150 75 60	300 150 120	ns
t <sub>TLH</sub> t <sub>THL</sub>	Transition time	5 10 15		100 50 40	200 100 80	ns
t <sub>w</sub>	Clock pulse width	5 10 15	200 100 80	100 50 40		ns
t <sub>w</sub>	Reset pulse width	5 10 15	120 50 40	60 25 20		ns
t <sub>setup</sub>	Data setup time	5 10 15	200 80 60	100 40 30		ns
t <sub>setup</sub>	Data input disable setup time	5 10 15	180 100 70	90 50 35		ns
f <sub>max</sub>	Maximum clock frequency	5 10 15	3 6 8	6 12 16		MHz
t <sub>r</sub> t <sub>f</sub>	Clock input rise or fall time	5 10 15	15 5 5			$\mu$ s