MP8820

8-Bit Analog-to-Digital Converter
with an 8-Channel MUX

FEATURES

- **Precision 7–Bit Plus Sign ADC**
- **8 Channel Analog Mux**
- **Single Reference to GND**
- **Input Referenced to User Supplied V_{MID}**
- **DNL= ±1/2 LSB, INL=± 1 LSB**
- **Single Supply: 5 V**
- **ESD Protection: 2000 V**

APPLICATIONS

- **Servo Control**
- **Low Cost Audio Control**
- **Voice Acquisition**

GENERAL DESCRIPTION

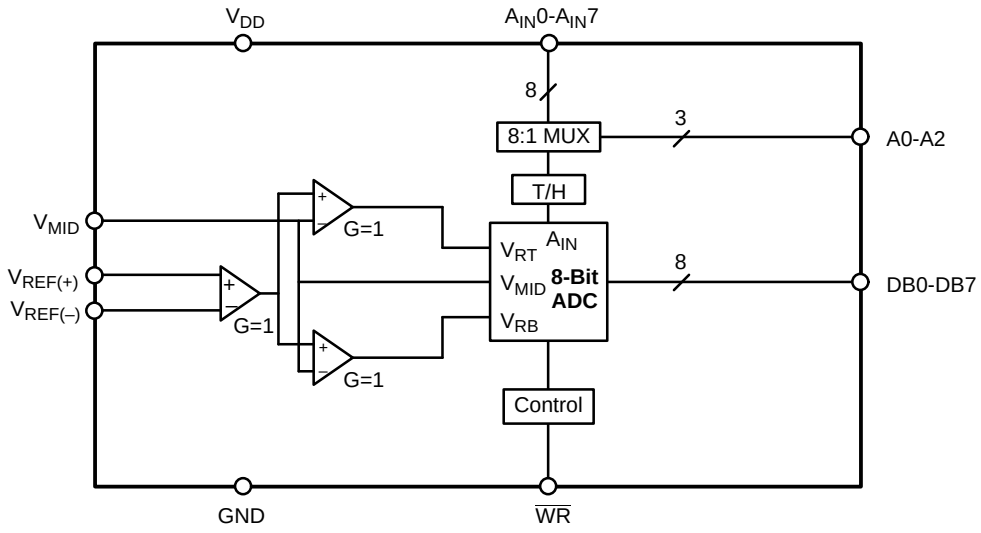
The MP8820 is a precision 1.6 MHz sampling 7-bit plus sign Analog-to-Digital Converter with an eight channel input mux and µP interface. The device has internal circuitry which receives the user supplied reference voltages $V_{REF(+)}$ and $V_{REF(–)}$, and generates the ADC reference voltages $V_{MID} \pm (V_{REF(+)} - V_{REF(–)})$. Since $V_{REF(+)}$ is internally buffered and $V_{REF(–)}$ is generally ground, this structure allows the user to easily generate an input range biased about a user-supplied V_{MID} from a grounded reference source.

The internal ADC reference voltages are capable of swinging to within 0.5 V of the supply rails, giving the MP8820 a wide range over which the effective channel gain can be adjusted.

The MP8820 uses a two-step flash conversion technique. The first section determines the sign and the 3 MSBs while the second segment converts the 4 LSBs. The ADC conversion begins when $\overline{WR}$ goes low and the data is valid 500 ns after the rising edge of $\overline{WR}$. The MP8820 operates from a single 5V supply and consumes only 175mW of power.

Specified for operation over the industrial (–40 to +85°C) temperature range, the MP8820 is available in Surface Mount (SOIC) and Shrunk Small Outline (SSOP) packages.

SIMPLIFIED BLOCK DIAGRAM

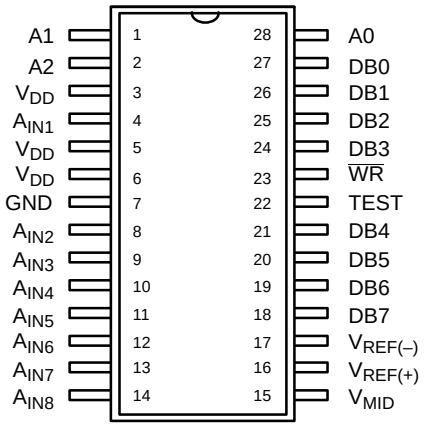


ORDERING INFORMATION

Package Type	Temperature Range	Part No.
SOIC	–40 to +85°C	MP8820AS
SSOP	–40 to +85°C	MP8820AQ

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



28 Pin SOIC (0.300") – S28
28 Pin SSOP – A28

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	A1	Analog Input Mux Address Bit 1
2	A2	Analog Input Mux Address Bit 2
3	V_{DD}	Positive Power Supply (5 V)
4	A_{IN0}	Analog Input 0
5	V_{DD}	Positive Power Supply (5 V)
6	V_{DD}	Positive Power Supply (5 V)
7	GND	Negative power supplies (0V)
8	A_{IN1}	Analog Input 1
9	A_{IN2}	Analog Input 2
10	A_{IN3}	Analog Input 3
11	A_{IN4}	Analog Input 4
12	A_{IN5}	Analog Input 5
13	A_{IN6}	Analog Input 6
14	A_{IN7}	Analog Input 7
15	V_{MID}	System Reference

PIN NO.	NAME	DESCRIPTION
16	$V_{REF(+)}$	Reference Voltage + Input Terminal
17	$V_{REF(–)}$	Reference Voltage – Input Terminal.
18	DB7 (MSB)	Data Output Bit 7
19	DB6	Data Output Bit 6
20	DB5	Data Output Bit 5
21	DB4	Data Output Bit 4
22	TEST	Test Mode Pin
23	$\overline{WR}$	Sample Window Control
24	DB3	Data Output Bit 3
25	DB2	Data Output Bit 2
26	DB1	Data Output Bit 1
27	DB0	Data Output Bit 0
28	A0	Analog Input Mux Address Bit 0

ELECTRICAL CHARACTERISTICS TABLE FOR DUAL SUPPLIES

Unless Otherwise Noted: V_{DD} = 5 V, GND = 0 V, $V_{REF(+)}$ = 1.5 V, $V_{REF(–)}$ = 0 V, V_{MID} = 2.5 V.

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Units	Test Conditions/Comments
DC CHARACTERISTICS						
Resolution	N	8			Bits	
Differential Non-Linearity	DNL	–1	±1/4	1	LSB	
Differential Non-Linearity[2]	DNL	–1	±1/2	1	LSB	@ $V_{REF(+)} – V_{REF(–)}$ = 0.5 V
Integral Non-Linearity[7]	INL	–1	±1/2	1	LSB	
Integral Non-Linearity[4, 7]	INL	–1	±1/2	1	LSB	@ $V_{REF(+)} – V_{REF(–)}$ = 0.5 V
Monotonicity			Guaranteed			
Bipolar Zero Error	B_{ZE}	–25	10	25	mV	Offset is measured as the bipolar zero code transition, 01111111 to 10000000, relative to V_{MID}
Zero Scale Drift[2, 5]	Z_{SD}			50	µV/°C	
Full Scale Error					%FS	This is a measure of the internal reference translation. Ideally $V_{RT} – V_{MID} = V_{MID} – V_{RB} = V_{REF(+)} – V_{REF(–)}$
V_{MID} to V_{RT}	$+F_{SE}$	–5.0	2.5	5.0		
V_{MID} to V_{RB}	$–F_{SE}$	–5.0	2.5	5.0		
Full Scale Drift[2, 6]	F_{SD}		0.025		%FS/°C	
DC Input Range[1]	V_{IN}p-p	1		3	Vpp	The analog input is specified as Vpp centered around V_{MID}
Aperture Delay	t_{AP}		50		ns	From rising edge of $\overline{WR}$
Input Capacitance	C_{IN}		25		pF	Measured with V_{IN} – DC = 2.5 V and $\overline{WR}$ = low
REFERENCE VOLTAGES						
Positive Reference Input Voltage	$V_{REF(+)}$	0.5		1.5	V	Reference voltage with respect to $V_{REF(–)}$
$V_{REF(+)}$ Input Resistance	RVR+		1		MΩ	
Internal Reference Settling Time	VR_{STL}		500		ns	Settling time required for ADC to make a proper conversion after ($V_{REF(+)} – V_{REF(–)}$) has changed
Negative Reference Input Voltage	$V_{REF(–)}$	0		$V_{REF(+)}$ –0.5	V	
$V_{REF(–)}$ Input Resistance	RVR–		1		KΩ	
V_{MID} Input Current	I_{VM}		0		mA	
V_{MID} Range	V_{MID}	2	2.5	3	V	$V_{MID} \le V_{DD}$ –0.5 – [$V_{REF(+)} – V_{REF(–)}$] $V_{MID} \le V_{SS}$ +0.5 + [$V_{REF(–)} – V_{REF(–)}$]
POWER SUPPLIES						All GNDs are Chip Substrate
Positive Supply	V_{DD}	4.75	5	5.25	V	
Negative Supply	GND	0	0	0	V	
Power Supply Rejection Ratio[2]	PSRR			–48	dB	f = 1 kHz. Not tested.
Supply Current	I_{DD}			45	mA	
DIGITAL CHARACTERISTICS[3, 4]						
Digital Input High Voltage	V_{IH}	4			V	
Digital Input Low Voltage	V_{IL}			1	V	

ELECTRICAL CHARACTERISTICS TABLE

Description	Symbol	25°C Min	25°C Typ	25°C Max	Units	Conditions
DIGITAL CHARACTERISTICS (CONT'D)						
V_{OL}	V_{OL}			0.5	V	@ I_{OL} = 1 mA
V_{OH}	V_{OH}	4.5				@ I_{OH} = 1 mA
I_{IN}-Dig	I_{DL}	–50		50	µA	
3-State Leakage	I_{LK}	–50		50	µA	
Digital Timing Specifications						For testing, rise time = fall time = 10 ns. Output loading = 50 pF.
Write time (analog input tracking)	t_{WR}	150			ns	
Conversion Time	t_{CONV}		500		ns	
Input mux set-up time	t_{MSU}	150			ns	
Input mux hold time	t_{MH}	50			ns	

NOTES

1 Maximum input voltage is 1 V less than V_{DD}.

2 Guaranteed but not production tested.

3 Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.

4 See timing diagram.

5 Measured as the change in the bipolar zero error over temperature. This error does not include the error introduced by the external reference drift.

6 This error does not include the error introduced by the external reference drift.

7 INL is measured as a 7-bit +sign ADC with 8-bit resolution.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND . . . . . 6 V
All Digital Inputs . . . . . V_{DD} +0.5 V to GND –0.5 V
Storage Temperature . . . . . –65 to 150°C
Lead Temperature (Soldering 10 seconds) . . . . . +300°C

ESD Rating . . . . . 2000 V
Package Power Dissipation Rating @ 75°C
SSOP, SOIC 1000mW
Derates above 75°C . . . . . 6mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

THEORY OF OPERATION

The defining feature of the MP8820 is that it digitizes a bipolar input signal centered around a given voltage, V_{MID}. The peak to peak swing of A_{IN} is defined by the two input reference voltages, $V_{REF(+)}$ and $V_{REF(–)}$.

The MP8820 takes in the center voltage and the two reference voltages and moves the resistor ladder endpoints V_{RT} and V_{RB} of the ADC around V_{MID} by $\pm(V_{REF(+)} - V_{REF(–)})$. In this way, a unipolar to bipolar translation can take place without having to use both a positive and negative supply. The center voltage acts as a bipolar zero and signals that moves below it are considered negative and signals that exceed it are taken to be positive. The block diagram is shown in *Figure 1.*

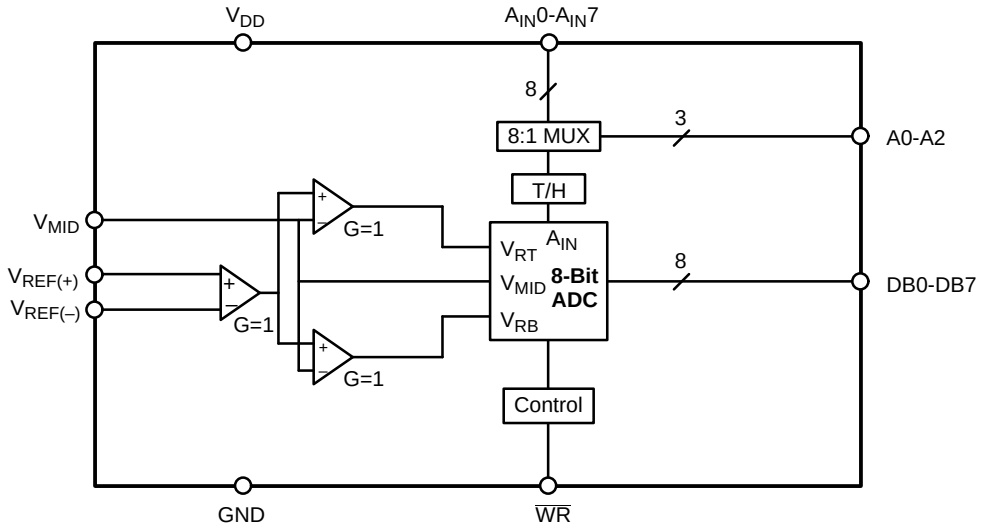


Figure 1. MP8820 Block Diagram

Unlike a unipolar system where one end of the ADC's resistor ladder is modulated above an offset voltage, both ends of the MP8820's reference chain expand or contract around a fixed V_{MID}. The maximum positive full scale voltage is $V_{RT} = V_{MID} + (V_{REF(+)} - V_{REF(–)})$. The maximum negative full scale voltage is $V_{RB} = V_{MID} - (V_{REF(+)} - V_{REF(–)})$. This type of translation is particularly useful in single supply applications where the input is centered about user specified V_{MID}.

The ideal transfer characteristic of the MP8820 is shown in *Figure 2.* An actual transfer characteristic with associated error terms is shown in *Figure 3.*

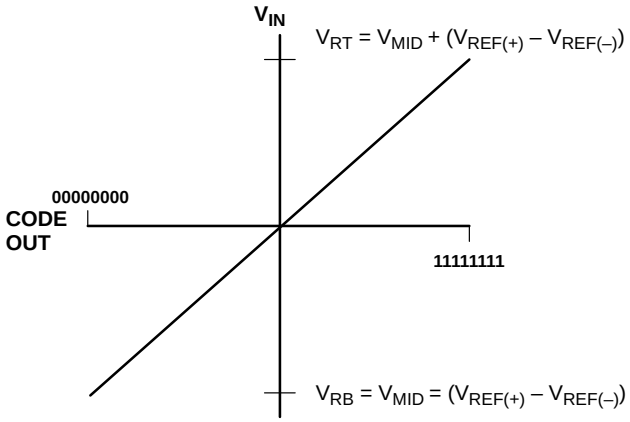


Figure 2. Ideal Transfer Characteristics

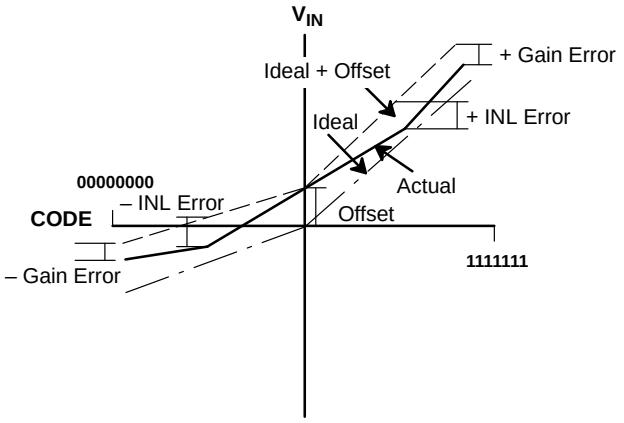


Figure 3. Transfer Characteristics with Error Terms

The sign of the digital output code is determined by whether the input voltage, A_{IN}, exceeds V_{MID}. If A_{IN} is greater than V_{MID}, then the seven bit conversion occurs in the positive half of the transfer function. If A_{IN} is less than V_{MID}, then the translation occurs in the negative half of the transfer function. *Table 1.* shows the digital codes that result from different input voltages.

CODE	A_{IN}
00000000	–FS
00000001	–FS + 1LSB
.	.
.	.
10000000	V_{MID} = BZ
.	.
.	.
11111110	FS – 2LSB
11111111	FS – 1LSB

Table 1. Digital Codes vs. Input Voltage

The MP8820 uses a stand alone µP interface. The user starts a conversion by taking $\overline{WR}$ low. While $\overline{WR}$ is low, the input track and hold follows the input voltage, A_{IN}. On the rising edge of $\overline{WR}$, the input is sampled. The rising edge of $\overline{WR}$ enables a state machine which steps the ADC through a conversion.

The output port is held in high impedance state during the conversion period. The operating timing diagrams are shown in *Figure 4.*

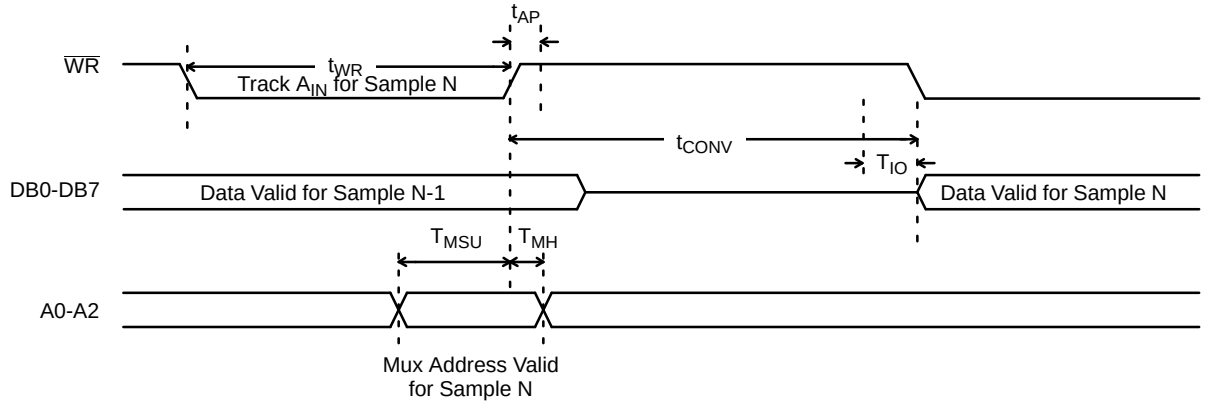


Figure 4. Operating Timing Diagrams

Analog To Digital Conversion

The MP8820 converts analog voltages into 256 digital codes by encoding the outputs of 15 coarse and 15 fine comparators. When $\overline{WR}$ goes low, the input sample and hold circuitry is enabled. The track and hold circuit will follow the output of the 8 channel mux. The channel that is to be converted does not need to be selected until a time equal to T_{MSU}, or 150 ns, before the rising edge of $\overline{WR}$. So, while $\overline{WR}$ is low, the track and hold circuit only has to follow the analog input to be converted for 150 ns.

The analog input is sampled at a time equal to the aperture delay, T_{AP}, after the rising edge of $\overline{WR}$. The aperture delay also accounts for internal propagation delays. The mux address lines may also select a new channel at a time equal to T_{AP} following the rising edge of $\overline{WR}$. For the analog timing diagram, see *Figure 5.*

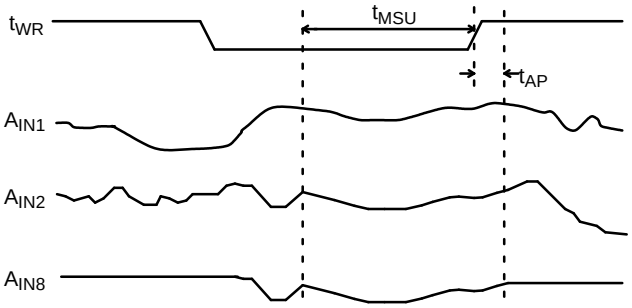


Figure 5. Analog Timing Diagram

clock phase ϕc. The voltage stored on the capacitor is then equal to $V_{BAL} + (V_{IN} - V_{TAP})$. This voltage will force the inverter high or low and the result is latched.

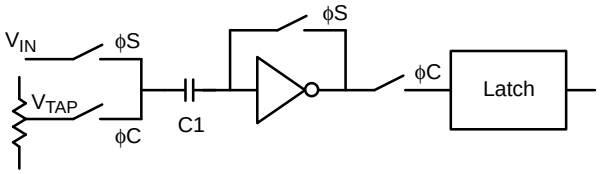


Figure 6. Comparator Block Diagram

Inside the ADC is a series of comparators that sample the analog input and compare it against a resistor tap voltage. A state machine generates the internal clocks necessary to control the comparators, ϕc (CLK high) and ϕs (CLK low = sample). See *Figure 6.* The rising edge of the CLK input marks the end of the sampling phase, ϕs. On ϕs, the analog input voltage is sampled and stored across capacitor C1. The switches controlled by ϕs are opened prior to the compare which is done on

The analog to digital conversion happens in four phases. During the first phase, the analog input is sampled. During the second phase, this input is compared against the reference ladder to determine the MSBs. After the MSBs are determined, a subrange is set for phase three, the conversion of the LSBs. Once all the bits have been derived, the MP8820 performs a correction. The valid data is then ready at the output. The timing diagram is shown in *Figure 7.*

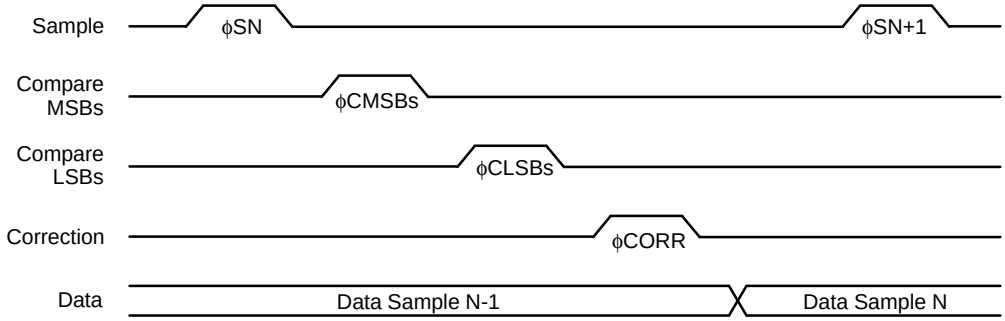
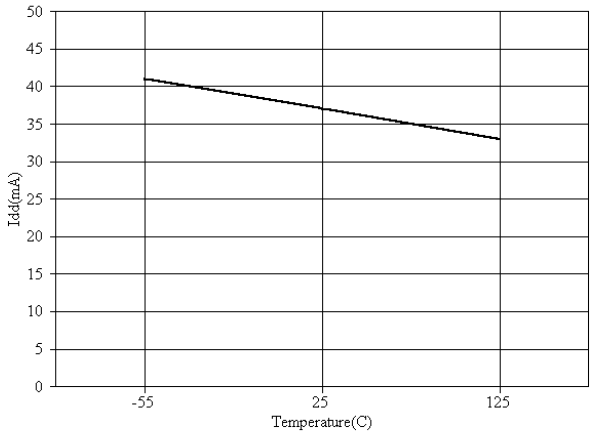


Figure 7. Internal ADC Timing Diagram

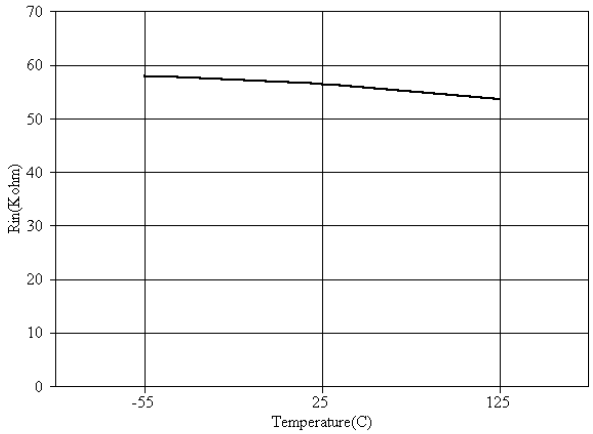
The input mux operates as a standard 8 to 1 decoder. One of eight analog inputs is selected depending on the condition of the address pins A0, A1, and A2. The mux can change address after a time equal to t_{AP} following the rising edge of $\overline{WR}$. The address should be held constant for at least 150 ns before the rising edge of $\overline{WR}$.

Function	$\overline{WR}$	XINT	A0	A1	A2
Start A_{IN} tracking	↓	1	X	X	X
Sample A_{IN}	↑	1	X	X	X
Start Convert	↑	1	X	X	X
Conversion Complete	1	↓	X	X	X
Enable Output Data	X	0	X	X	X
Select Input A_{IN1}	X	X	0	0	0
Select Input A_{IN2}	X	X	0	0	1
Select Input A_{IN3}	X	X	0	1	0
Select Input A_{IN4}	X	X	0	1	1
Select Input A_{IN5}	X	X	1	0	0
Select Input A_{IN6}	X	X	1	0	1
Select Input A_{IN7}	X	X	1	1	0
Select Input A_{IN8}	X	X	1	1	1

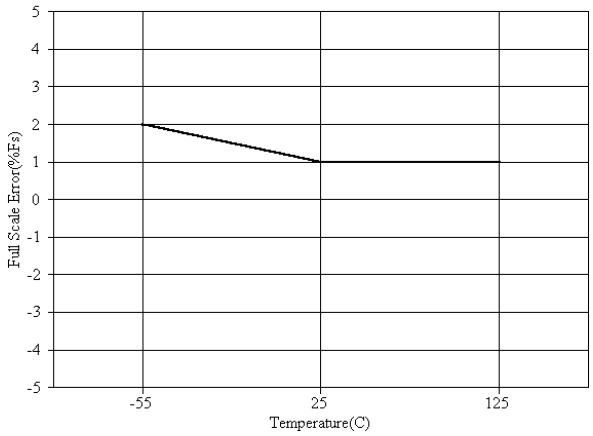
Table 2. Truth Table



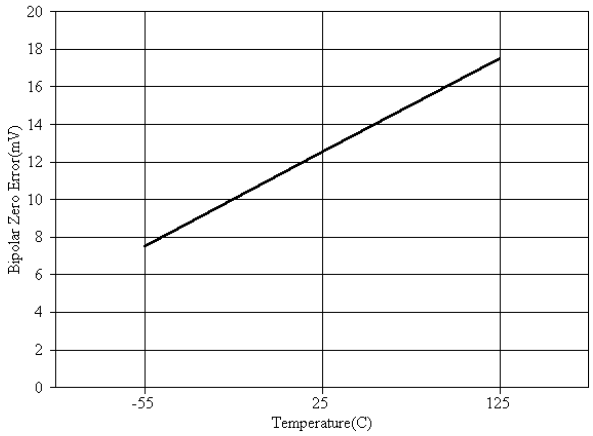
Graph 1. Supply Current vs. Temperature



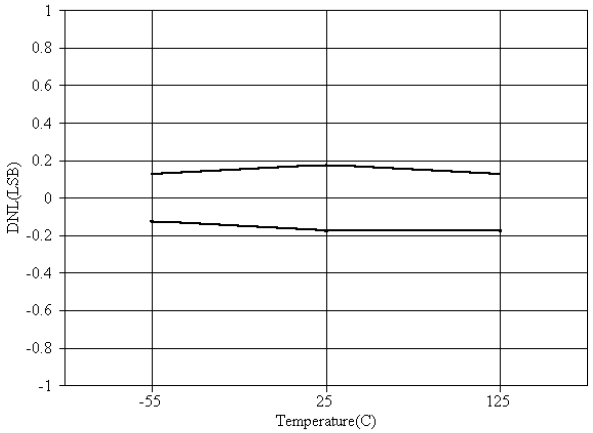
Graph 2. Input Resistance vs. Temperature



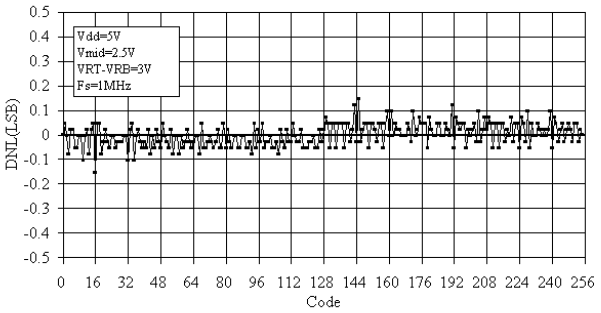
Graph 3. Full Scale Error vs. Temperature



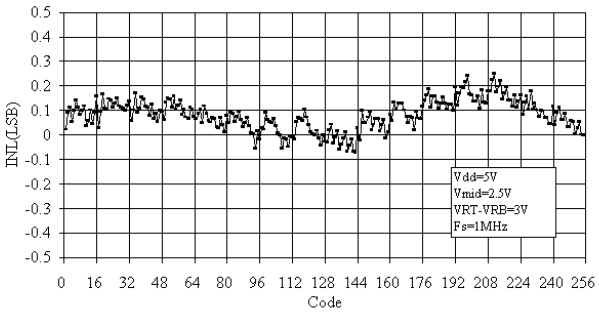
Graph 4. Bipolar Zero Error vs. Temperature



Graph 5. DNL vs. Temperature

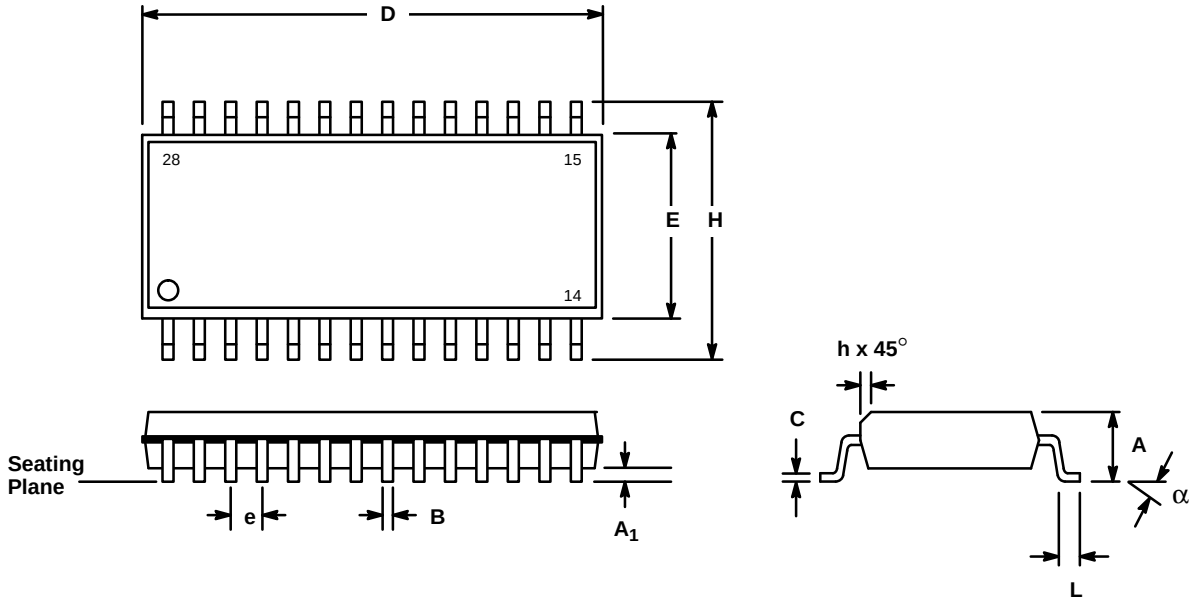


Graph 6. DNL Error Plot



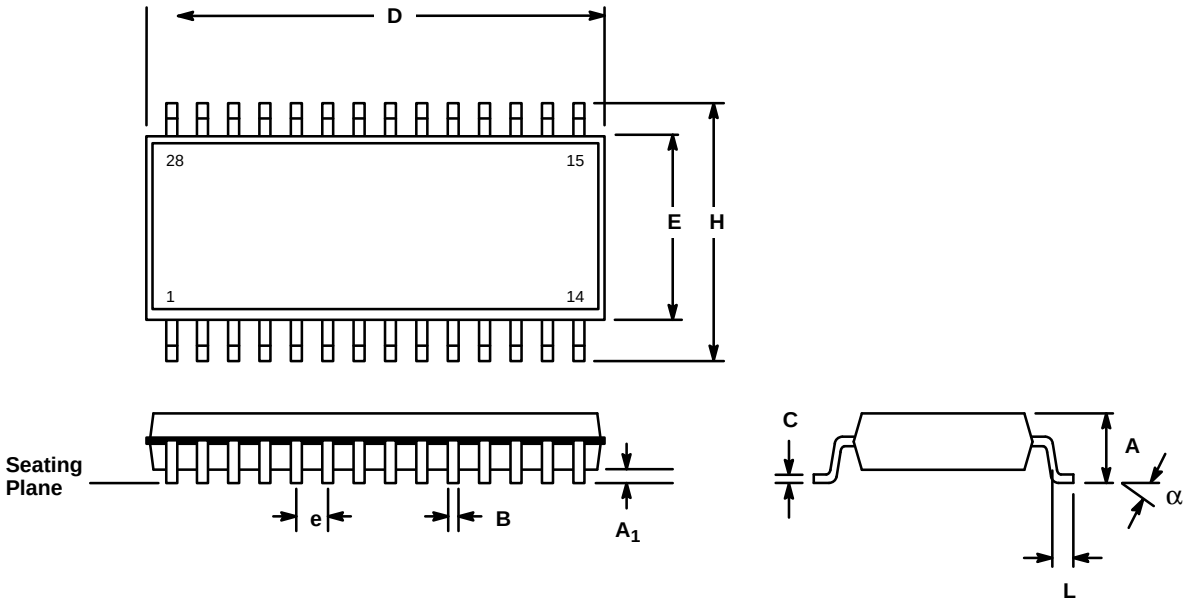
Graph 7. INL Error Plot for 7-Bit + Sign ADC

28 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S28



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.701	0.711	17.81	18.06
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

28 LEAD SHRINK SMALL OUTLINE PACKAGE (SSOP)
A28



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.73	2.05	0.068	0.081
A_1	0.05	0.21	0.002	0.008
B	0.20	0.40	0.008	0.016
C	0.13	0.25	0.005	0.010
D	10.07	10.40	0.397	0.409
E	5.20	5.38	0.205	0.212
e	0.65 BSC		0.0256 BSC	
H	7.65	8.1	0.301	0.319
L	0.45	0.95	0.018	0.037
α	0°	8°	0°	8°

NOTICE

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