

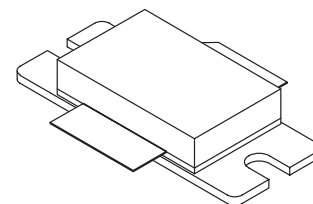
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF18090A
MRF18090AS

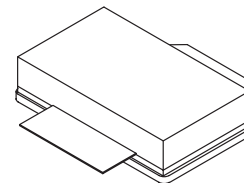
Designed for GSM and EDGE base station applications with frequencies from 1.8 to 2.0 GHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in class AB for GSM and EDGE cellular radio applications.

- GSM and EDGE Performances, Full Frequency Band
Power Gain — 13.5 dB (Typ) @ 90 Watts (CW)
Efficiency — 52% (Typ) @ 90 Watts (CW)
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 90 Watts (CW) Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters

1.80 – 1.88 GHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETS



CASE 465B-03, STYLE 1
(NI-880)
(MRF18090A)



CASE 465C-02, STYLE 1
(NI-880S)
(MRF18090AS)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	+15, -0.5	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 26\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Quiescent Voltage ($V_{DS} = 26\text{ Vdc}$, $I_D = 750\text{ mAdc}$)	$V_{GS(Q)}$	2.5	3.7	4.5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.1	—	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 3\text{ Adc}$)	g_{fs}	—	7.2	—	S

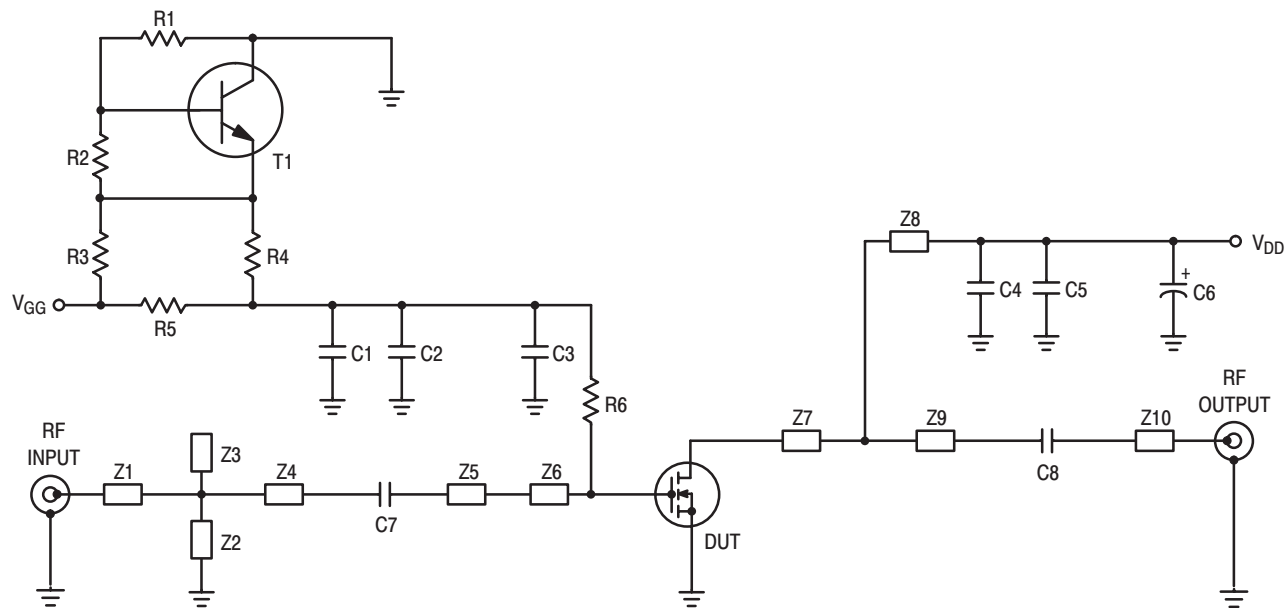
DYNAMIC CHARACTERISTICS

Reverse Transfer Capacitance ($V_{DS} = 26\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	4.2	—	pF
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FUNCTIONAL TESTS (In Motorola Test Fixture)

Common–Source Amplifier Power Gain @ 90 W (1) ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 750\text{ mA}$, $f = 1805 - 1880\text{ MHz}$)	G_{ps}	12.0	13.5	—	dB
Drain Efficiency @ 90 W (1) ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 750\text{ mA}$, $f = 1805 - 1880\text{ MHz}$)	η	47	52	—	%
Input Return Loss (1) ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 750\text{ mA}$, $f = 1805 - 1880\text{ MHz}$)	IRL	—	—	-10	dB
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 750\text{ mA}$ VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			

(1) To meet application requirements, Motorola test fixtures have been designed to cover the full GSM1800 band, ensuring batch-to-batch consistency.



C1, C3	1.0 μ F Chip Capacitors (0805)	Z2	0.197" x 0.087" Microstrip
C2	1.0 nF Chip Capacitor (0805)	Z3	0.819" x 0.087" Microstrip
C4, C5	6.8 pF, 100B Chip Capacitors, ATC	Z4	0.181" x 0.144" Microstrip
C6	220 μ F, 50 V Electrolytic Capacitor	Z5	0.383" x 1.148" Microstrip
C7, C8	12 pF, 100B Chip Capacitors, ATC	Z6	0.400" x 1.380" Microstrip
R1	2.2 k Ω Chip Resistor (0805)	Z7	0.351" x 0.351" Microstrip
R2, R3, R6	1.0 k Ω Chip Resistors (0805)	Z8	0.126" x 0.087" Microstrip
R4	10 k Ω Chip Resistor (0805)	Z9	1.280" x 0.087" Microstrip
R5	6.8 k Ω Chip Resistor (0805)	Z10	\approx 1.275" x 0.055" Microstrip
T1	BC847 SOT-23	PCB	Teflon [®] Glass
Z1	0.697" x 0.087" Microstrip		

Figure 1. 1.80 – 1.88 GHz Test Fixture Schematic

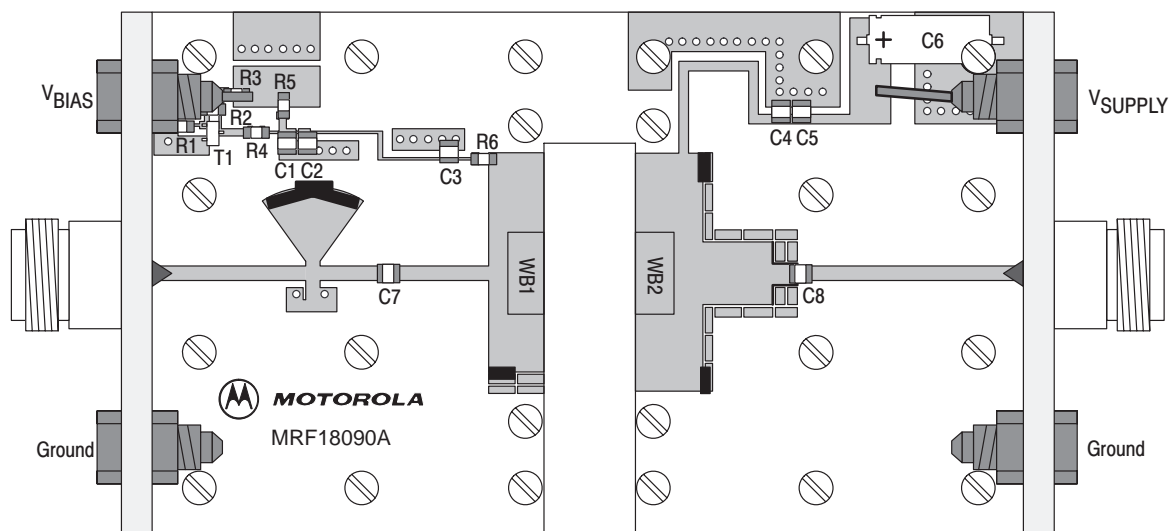
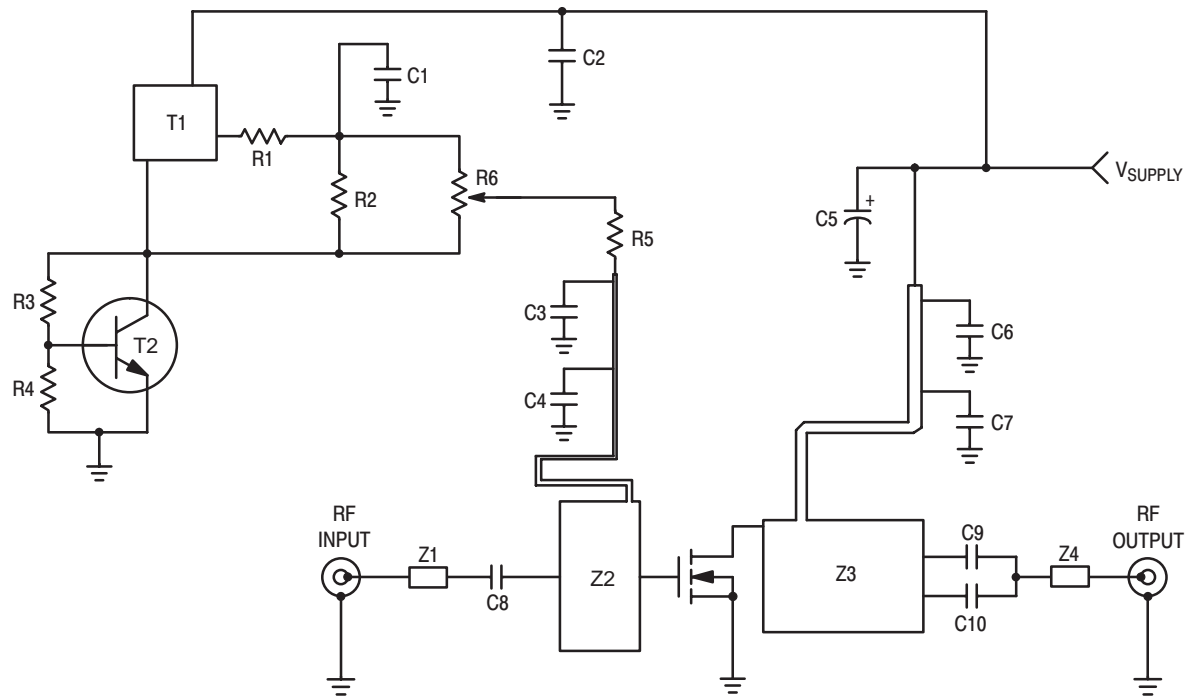


Figure 2. 1.80 – 1.88 GHz Test Fixture Component Layout



C1, C3	1 μ F Chip Capacitors (0805)	R5	10 k Ω Chip Resistor (0603)
C2	0.1 μ F Chip Capacitor (0805)	R6	5 k Ω , SMD Potentiometer
C4	1 nF Chip Capacitor (0805)	T1	LP2951 Micro-8 Voltage Regulator
C5	220 μ F, 50 V Electrolytic Capacitor	T2	BC847 SOT-23 NPN Transistor
C6, C7	8.2 pF, 100A Chip Capacitors	Z1	0.210" x 0.055" Microstrip
C8, C9, C10	22 pF, 100A Chip Capacitors	Z2	0.419" x 0.787" Microstrip
R1	10 Ω Chip Resistor (0805)	Z3	0.836" x 0.512" Microstrip
R2, R3	1 k Ω Chip Resistors (0805)	Z4	0.164" x 0.055" Microstrip
R4	2.2 k Ω Chip Resistor (0805)		Substrate = 0.5 mm Teflon [®] Glass

Figure 3. 1.80 – 1.88 GHz Demo Board Schematic

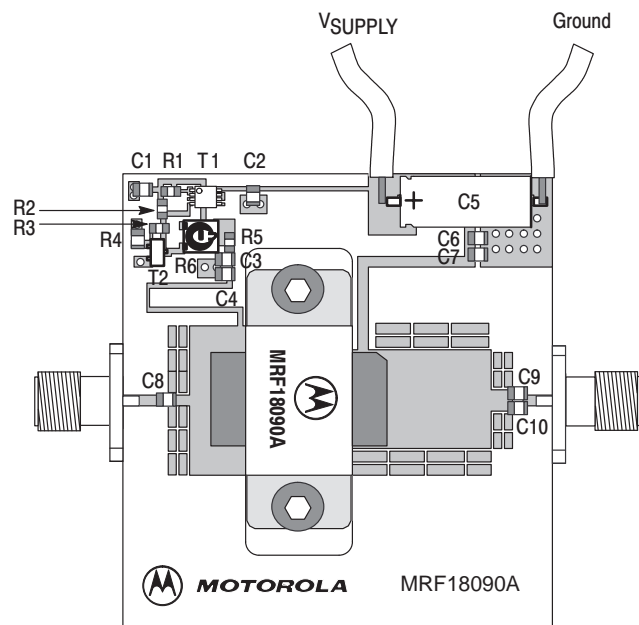


Figure 4. 1.80 – 1.88 GHz Demo Board Component Layout

TYPICAL CHARACTERISTICS

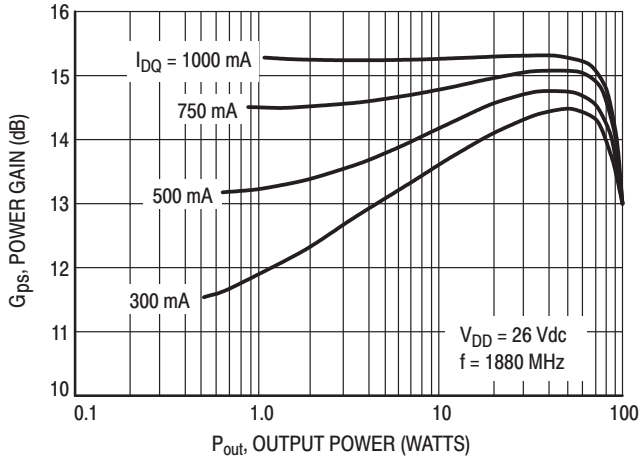


Figure 5. Power Gain versus Output Power

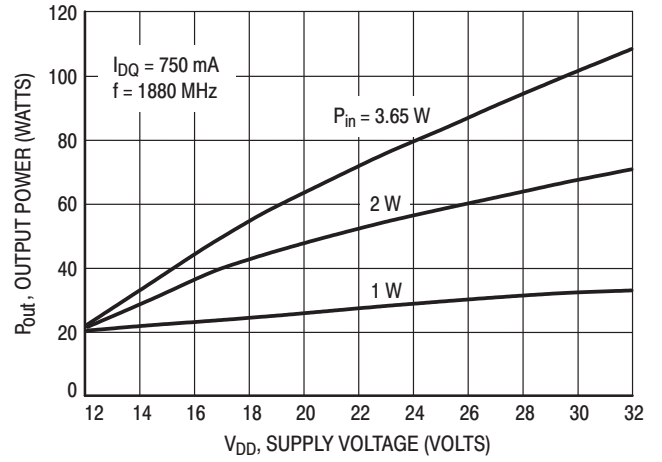


Figure 6. Output Power versus Supply Voltage

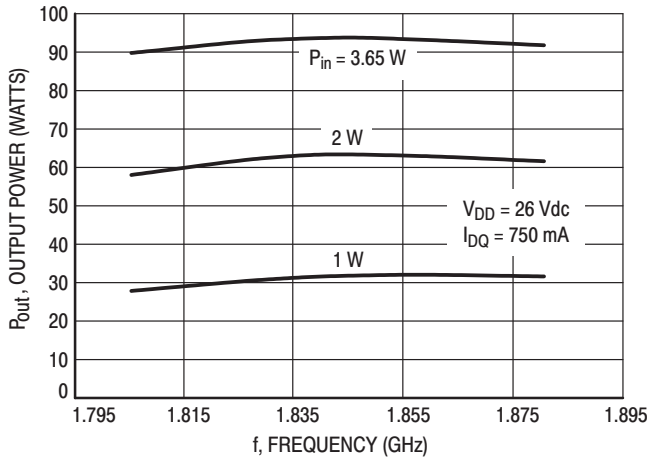


Figure 7. Output Power versus Frequency

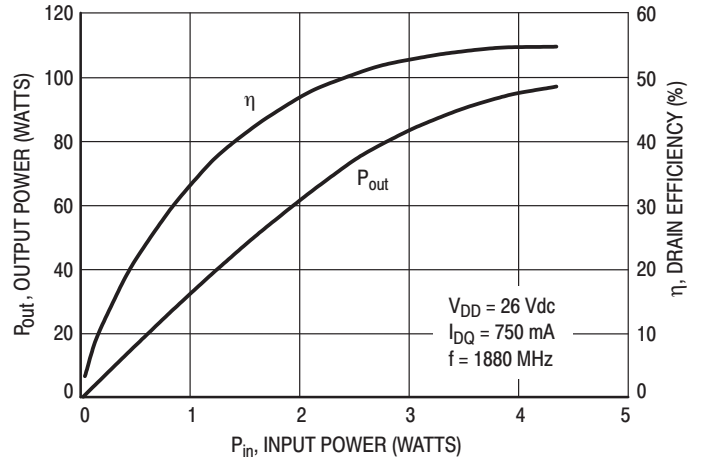


Figure 8. Output Power and Efficiency versus Input Power

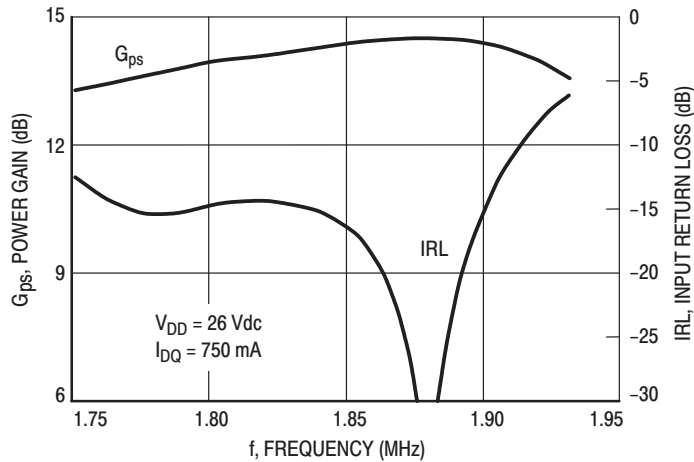
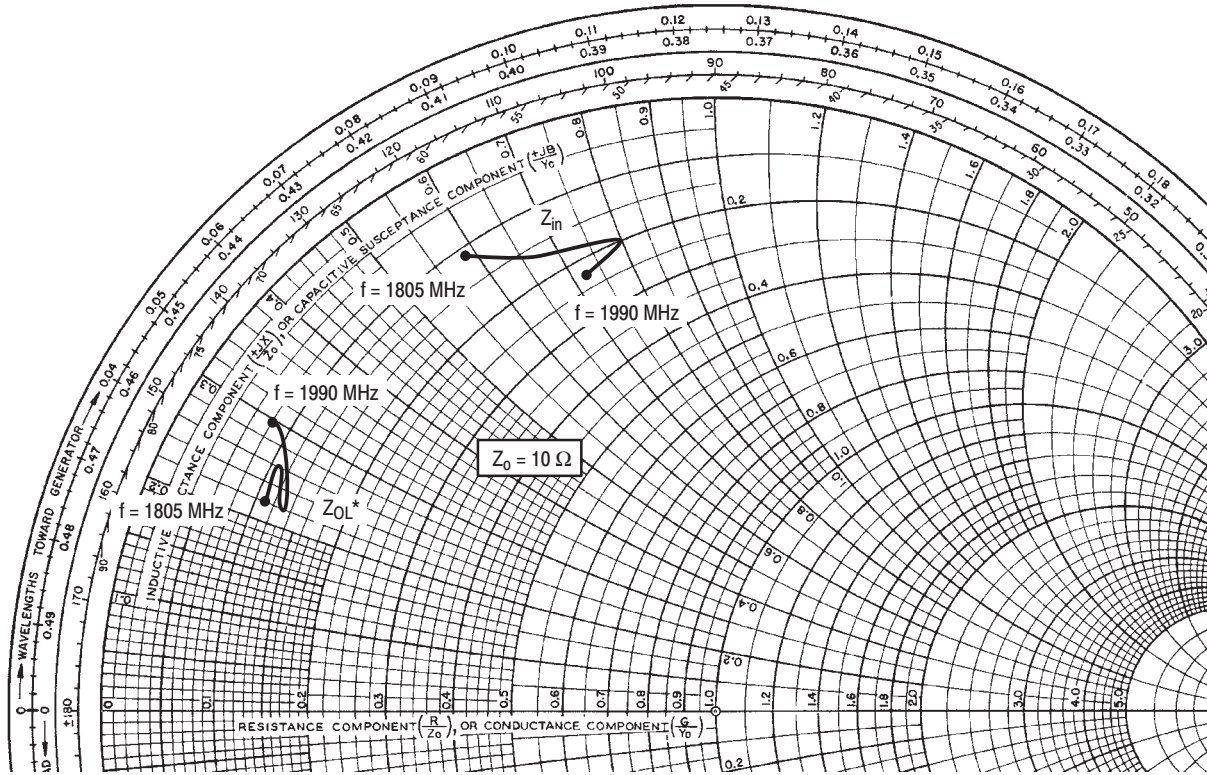


Figure 9. Wideband Gain and IRL (at Small Signal)



$V_{DD} = 26\text{ V}$, $I_{DQ} = 750\text{ mA}$, $P_{out} = 90\text{ Watts (CW)}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1805	$1.10 + j5.85$	$1.15 + j2.16$
1880	$1.56 + j6.75$	$1.13 + j2.60$
1930	$2.05 + j8.00$	$1.30 + j2.23$
1990	$2.30 + j7.30$	$0.82 + j2.90$

Z_{in} = Complex conjugate of the source impedance.

Z_{OL}^* = Complex conjugate of the optimum load at a given voltage, P1dB, gain, efficiency, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, and drain efficiency.

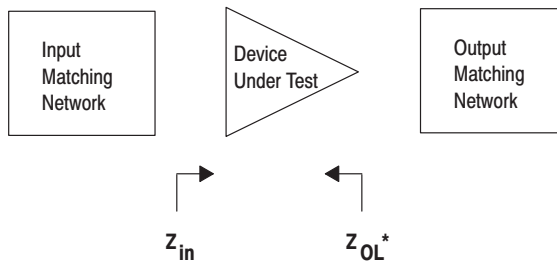
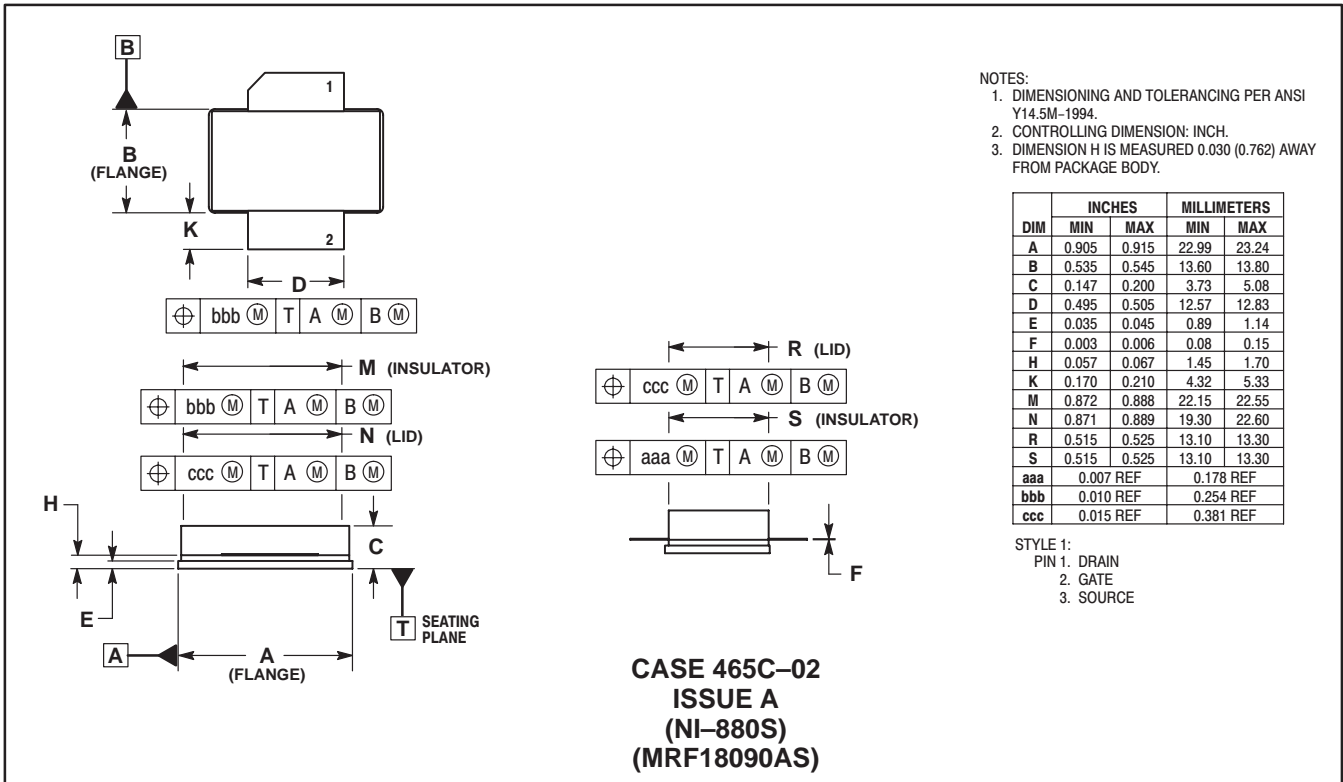
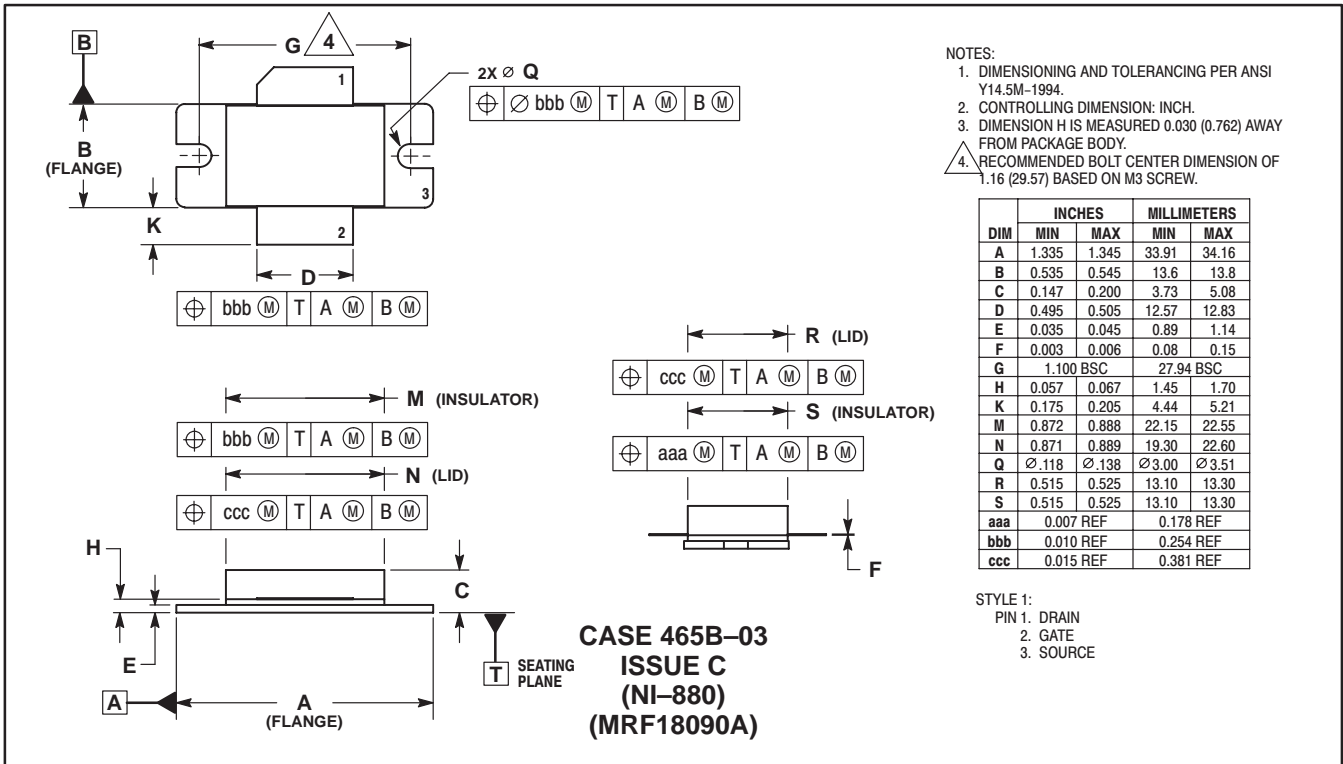



Figure 10. Large Signal Input and Output Impedance

PACKAGE DIMENSIONS



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