

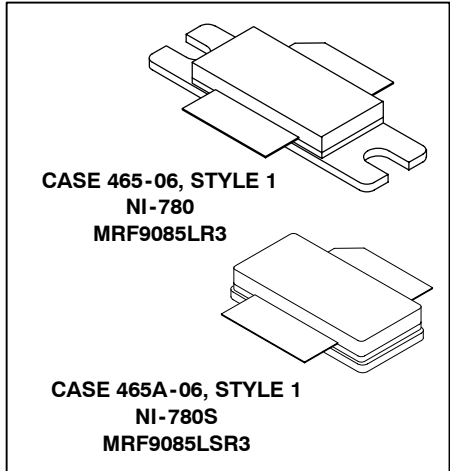
The RF Sub-Micron MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF9085LR3
MRF9085LSR3

Designed for broadband commercial and industrial applications with frequencies from 865 to 895 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 26 volt base station equipment.

880 MHz, 90 W, 26 V
LATERAL N-CHANNEL
RF POWER MOSFETs

- Typical CDMA Performance @ 880 MHz, 26 Volts, $I_{DQ} = 700$ mA
 IS-97 CDMA Pilot, Sync, Paging, Traffic Codes 8 Through 13
 Output Power — 20 Watts
 Power Gain — 17.9 dB
 Efficiency — 28%
 Adjacent Channel Power —
 750 kHz: -45.0 dBc @ 30 kHz BW
 1.98 MHz: -60.0 dBc @ 30 kHz BW
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 880 MHz, 90 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40 μ ” Nominal.
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25 $^\circ\text{C}$	P_D	250 1.43	Watts W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

(1) MTTF calculator available at <http://www.motorola.com/semiconductors/xf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

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ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model MRF9085LR3 MRF9085LSR3	M2 (Minimum) M1 (Minimum)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 26 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μAdc)	V _{GS(th)}	2.0	—	4.0	Vdc
Gate Quiescent Voltage (V _{DS} = 26 Vdc, I _D = 700 mAdc)	V _{GS(Q)}	—	3.7	—	Vdc
Drain-Source On-Voltage (V _{GS} = 10 Vdc, I _D = 2 Adc)	V _{DS(on)}	—	0.19	0.4	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 6 Adc)	g _{fs}	—	8.0	—	S

DYNAMIC CHARACTERISTICS (1)

Output Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{OSS}	—	73	—	pF
Reverse Transfer Capacitance (V _{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rSS}	—	2.9	—	pF

(1) Part is internally input matched.

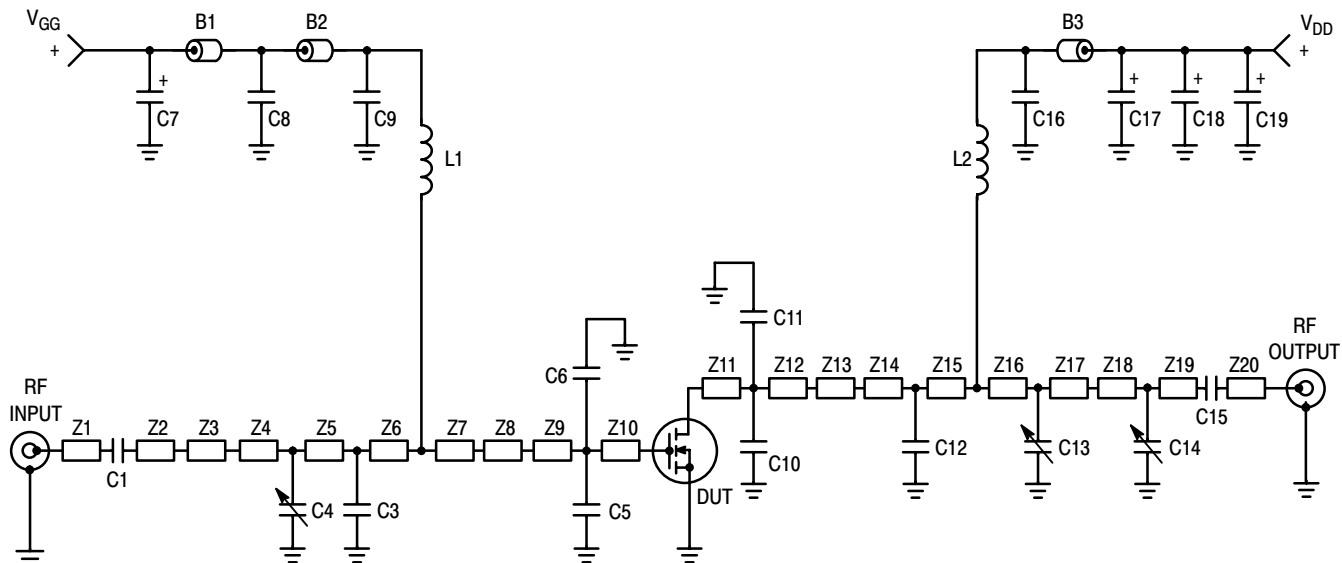
(continued)

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ELECTRICAL CHARACTERISTICS - continued ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	G_{ps}	17	17.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	η	36	40	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IMD	—	-31	-28	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$, $f_2 = 880.1\text{ MHz}$)	IRL	—	-21	-9	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	G_{ps}	—	17.9	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	η	—	40.0	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IMD	—	-31	—	dBc
Input Return Loss ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W PEP}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 865.0\text{ MHz}$, $f_2 = 865.1\text{ MHz}$)	IRL	—	-16	—	dB
Power Output, 1 dB Compression Point, CW ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	P_{1dB}	—	105	—	W
Common-Source Amplifier Power Gain ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	G_{ps}	—	17.5	—	dB
Drain Efficiency ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 880.0\text{ MHz}$)	η	—	51	—	%
Output Mismatch Stress ($V_{DD} = 26\text{ Vdc}$, $P_{out} = 90\text{ W CW}$, $I_{DQ} = 700\text{ mA}$, $f = 880.0\text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power			
Power Output, 1 dB Compression Point, CW (1) ($V_{DD} = 26\text{ Vdc}$, $I_{DQ} = 700\text{ mA}$, $f_1 = 960\text{ MHz}$)	P_{1dB}	—	105	—	W

(1) These values are derived from a 960 MHz optimized test fixture. Values are not applicable to Figures 1 and 2.



B1, B2, B3	Short Ferrite Beads, Surface Mount	Z6	0.076" x 0.220" Microstrip
C1, C9, C15, C16	47 pF Chip Capacitors, B Case, ATC	Z7	0.261" x 0.220" Microstrip
C3	5.6 pF Chip Capacitor, B Case, ATC	Z8	0.220" x 0.630" x 0.200" Taper
C4, C13	0.8 - 8.0 Variable Capacitors, Gigatrim	Z9	0.240" x 0.630" Microstrip
C5, C6, C12	8.2 pF Chip Capacitors, B Case, ATC	Z10	0.060" x 0.630" Microstrip
C7, C17, C18, C19	10 μ F, 35 V Tantalum Surface Mount Capacitors, Kemet	Z11	0.067" x 0.630" Microstrip
C8	20 K pF Chip Capacitor, B Case, ATC	Z12	0.233" x 0.630" Microstrip
C10, C11	16 pF Chip Capacitors, B Case, ATC	Z13	0.630" x 0.220" x 0.200" Taper
C14	0.6 - 4.5 Variable Capacitor, Gigatrim	Z14	0.200" x 0.220" Microstrip
L1	7.15 nH Inductor, Coilcraft	Z15	0.055" x 0.220" Microstrip
L2	17.5 nH Inductor, Coilcraft	Z16	0.088" x 0.220" Microstrip
N1, N2	N-Type Panel Mount, Stripline, M/A-Com	Z17	0.226" x 0.220" Microstrip
WB1, WB2	5 Mil BeCu Shim (0.225 x 0.525)	Z18	0.868" x 0.080" Microstrip
Z1	0.219" x 0.080" Microstrip	Z19	0.129" x 0.080" Microstrip
Z2	0.150" x 0.080" Microstrip	Z20	0.223" x 0.080" Microstrip
Z3	0.851" x 0.080" Microstrip	PCB	Arlon GX-0300-55-22, 30 mils
Z4	0.125" x 0.220" Microstrip		$\epsilon_r = 2.55$
Z5	0.123" x 0.220" Microstrip		

Figure 1. 865-895 MHz Broadband Test Circuit Schematic

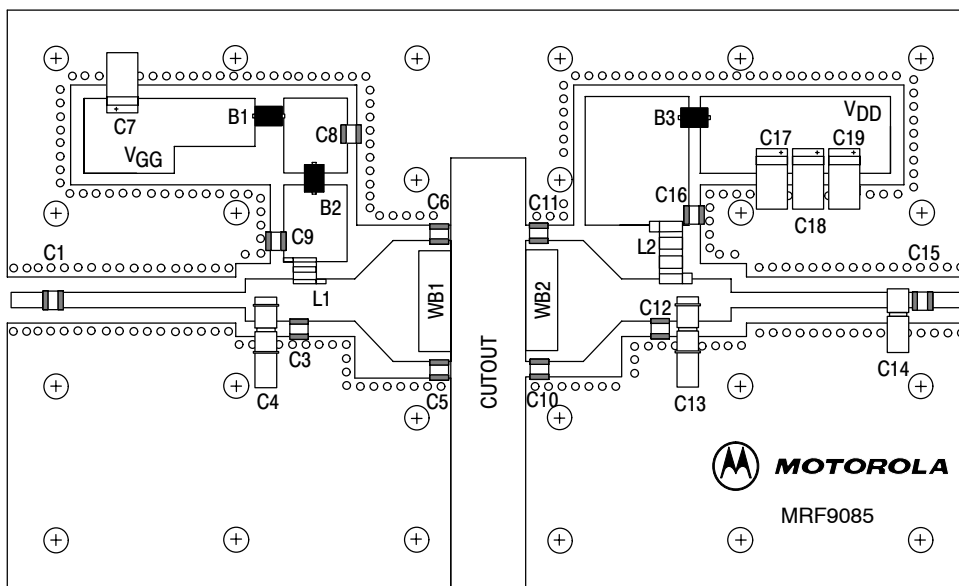


Figure 2. 865-895 MHz Broadband Test Circuit Component Layout

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TYPICAL CHARACTERISTICS

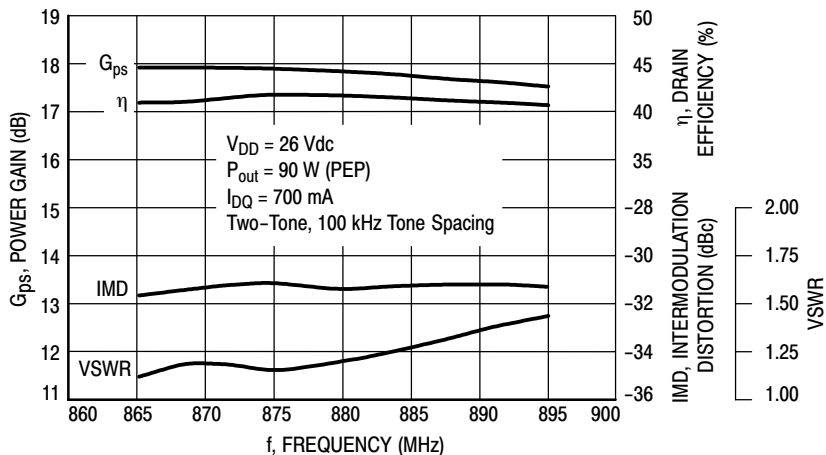


Figure 3. Class AB Broadband Circuit Performance

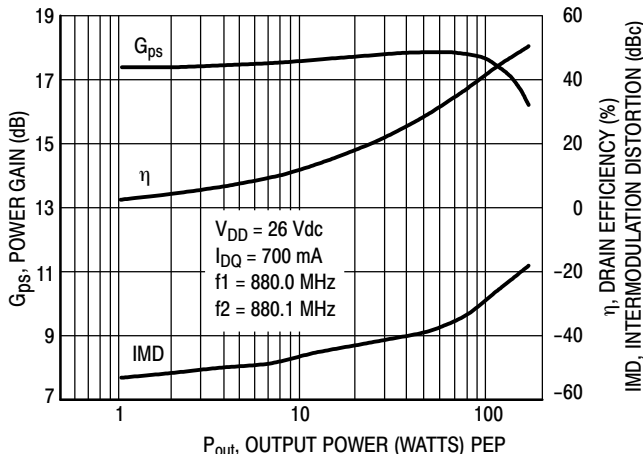


Figure 4. Power Gain, Efficiency, IMD versus Output Power

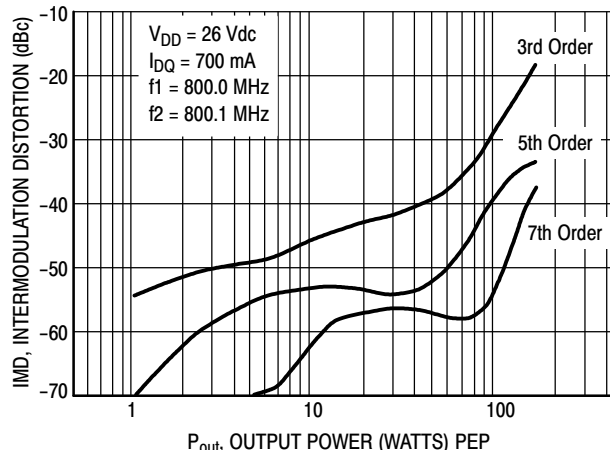


Figure 5. Intermodulation Distortion Products versus Output Power

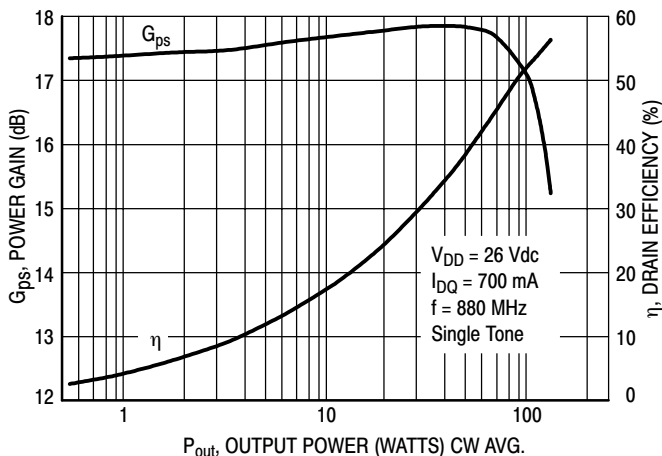


Figure 6. Power Gain, Efficiency versus Output Power

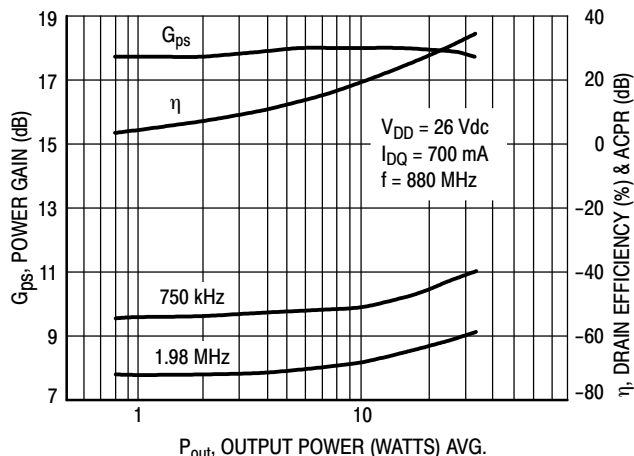
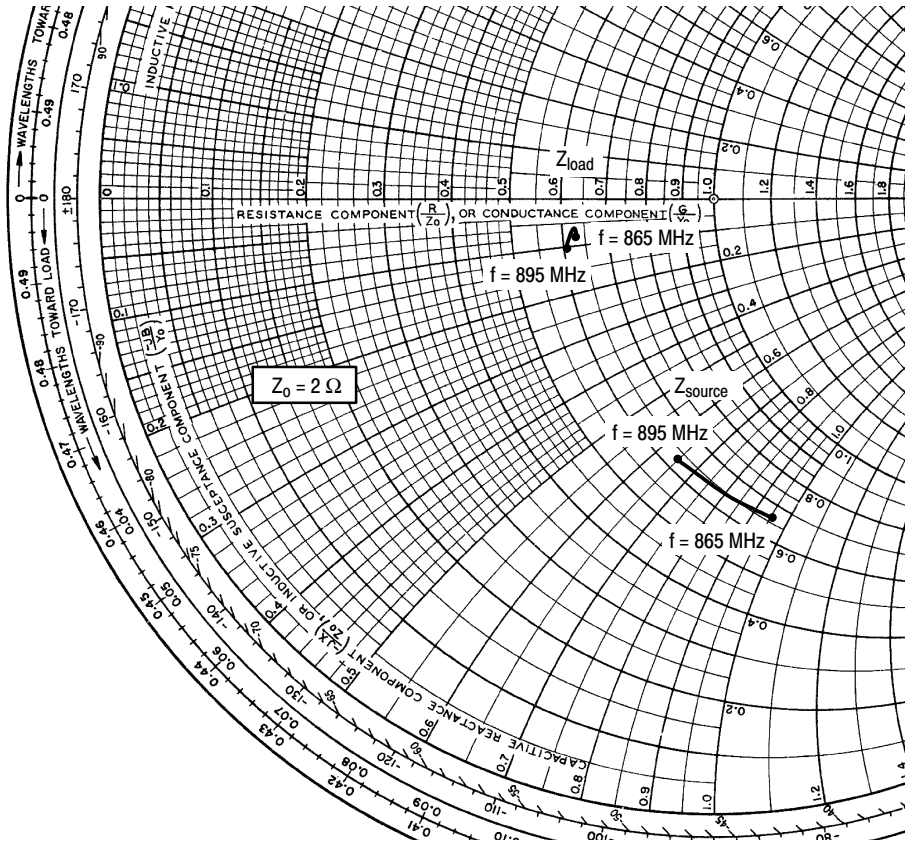


Figure 7. Power Gain, Efficiency, ACPR versus Output Power



$V_{DD} = 26 \text{ V}$, $I_{DQ} = 700 \text{ mA}$, $P_{out} = 90 \text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
865	$1.35 - j1.92$	$1.26 - j0.15$
880	$1.33 - j1.66$	$1.26 - j0.10$
895	$1.28 - j1.30$	$1.21 - j0.20$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

Note: Z_{load} was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

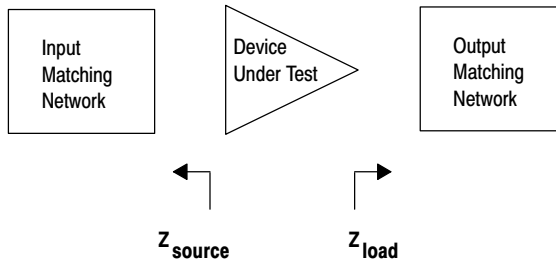
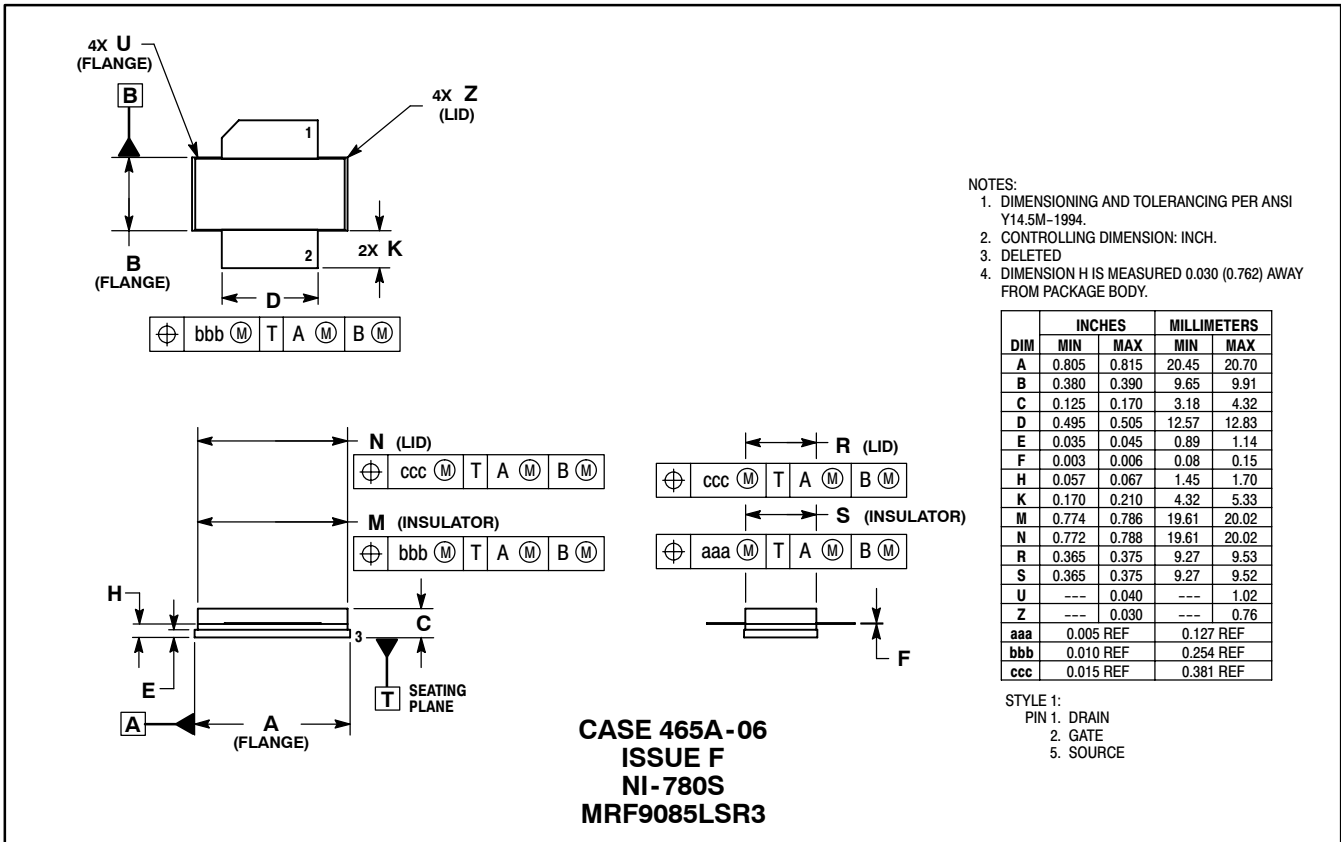
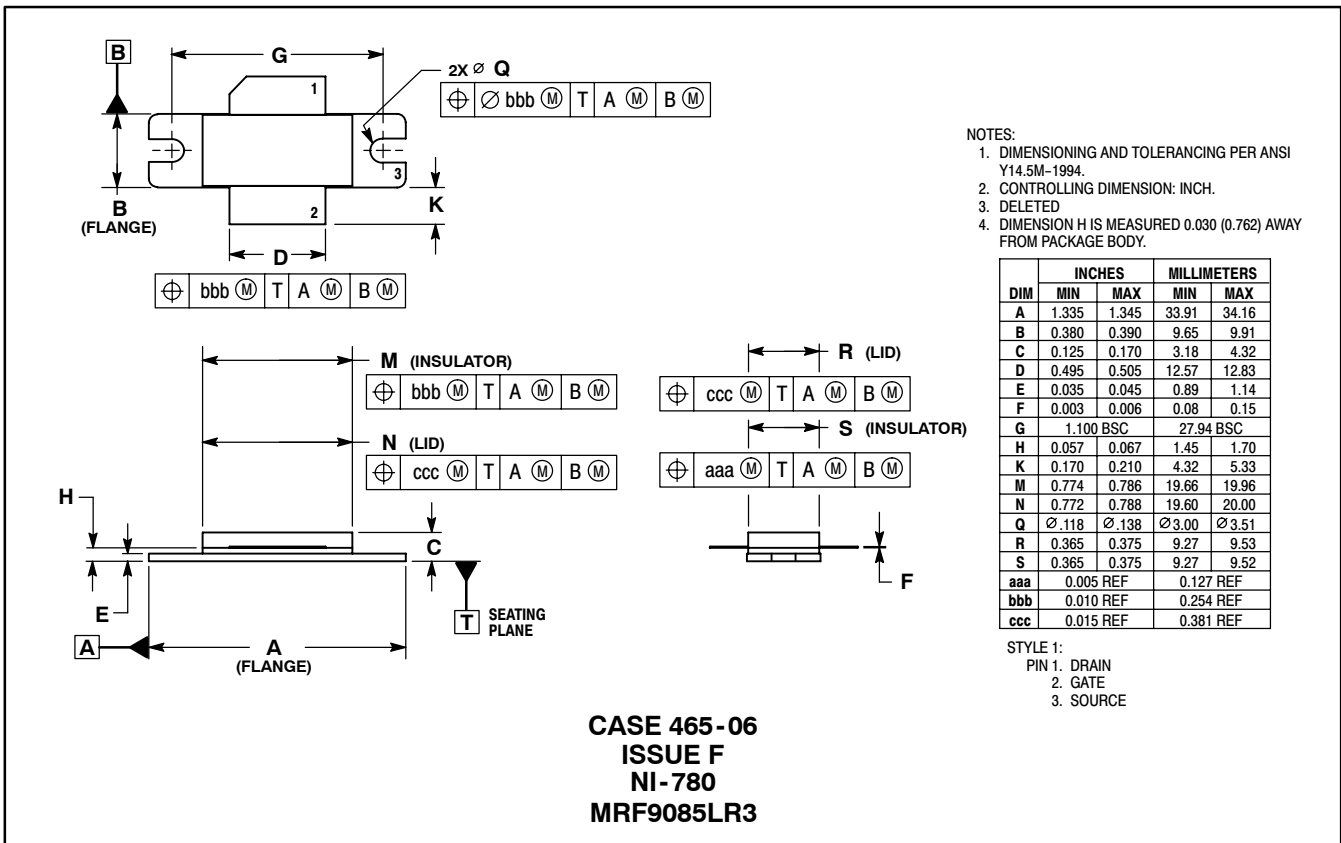


Figure 8. Series Equivalent Input and Output Impedance

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PACKAGE DIMENSIONS



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