

# OKI Semiconductor

## MSC23232C/CL-xxBS16/DS16

2,097,152-Word × 32-Bit DRAM MODULE : FAST PAGE MODE TYPE

### DESCRIPTION

The OKI MSC23232C/CL-xxBS16/DS16 is a fully decoded 2,097,152-word × 32-bit CMOS Dynamic Random Access Memory Module composed of sixteen 4-Mb DRAMs (1M × 4) in SOJ packages mounted with sixteen decoupling capacitors on a 72-pin glass epoxy single-inline package. This module is generally used for non-parity memory expansion applications such as fax machines, printers and personal computers. The low-power version (CL) offers reduced power consumption for mobile computing applications like laptops and palmtops.

### FEATURES

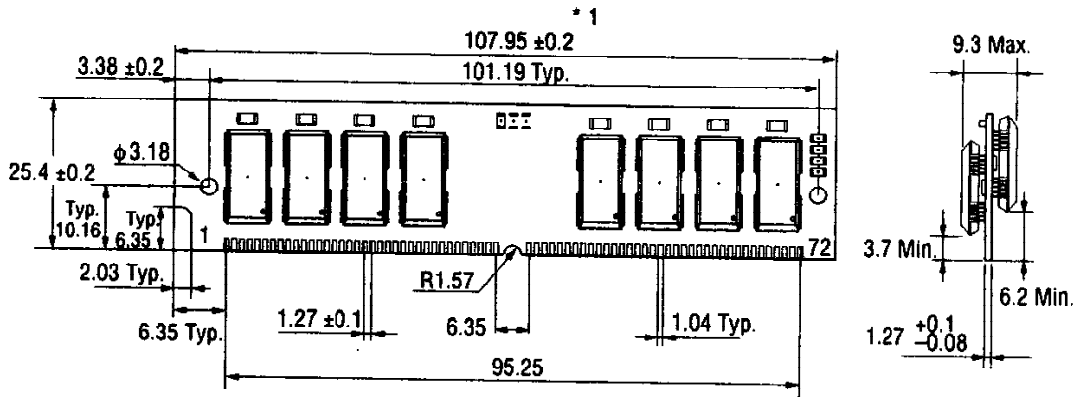
- 2-Meg × 32-bit organization
- 72-Pin Socket Insertable Module
  - MSC23232C/CL-xxBS16 : Gold tab
  - MSC23232C/CL-xxDS16: Solder tab
- Single 5 V supply ±10% tolerance
- Access times : 60, 70, 80 ns
- Input : TTL compatible
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms (128 ms : L-version)
- CAS before RAS refresh, CAS before RAS hidden refresh, RAS-only refresh capability
- Multi-bit test mode capability
- Fast Page Mode capability

### PRODUCT FAMILY

| Family                   | Access Time (Max.) |                 |                  | Cycle Time<br>(Min.) | Power Dissipation |                               |
|--------------------------|--------------------|-----------------|------------------|----------------------|-------------------|-------------------------------|
|                          | t <sub>RAC</sub>   | t <sub>AA</sub> | t <sub>CAC</sub> |                      | Operating (Max.)  | Standby (Max.)                |
| MSC23232C/CL-60BS16/DS16 | 60 ns              | 30 ns           | 15 ns            | 110 ns               | 4620 mW           | 88 mW/<br>17.6 mW (L-version) |
| MSC23232C/CL-70BS16/DS16 | 70 ns              | 35 ns           | 20 ns            | 130 ns               | 4180 mW           |                               |
| MSC23232C/CL-80BS16/DS16 | 80 ns              | 40 ns           | 20 ns            | 150 ns               | 3740 mW           |                               |

## PIN CONFIGURATION

MSC23232C/CL-xxBS16/DS16



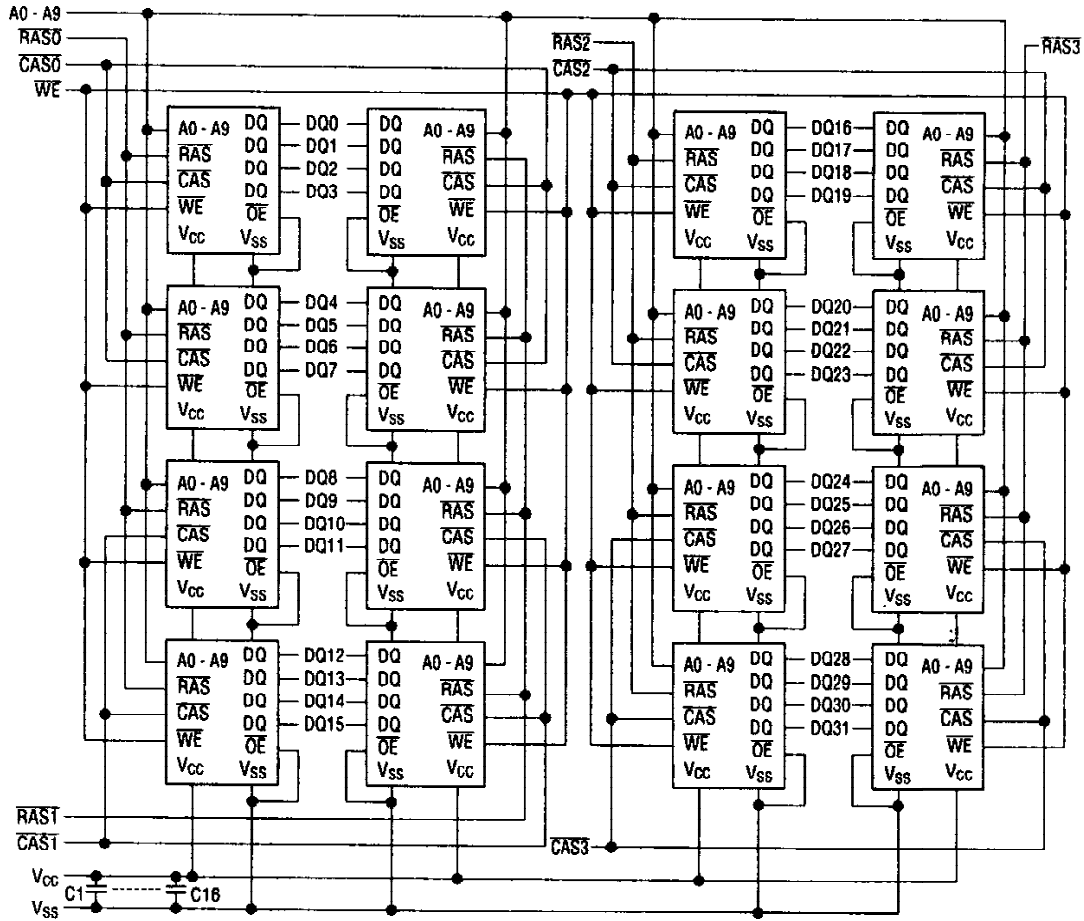
\*1 The common size difference of the board width 12.5 mm of its height is specified as  $\pm 0.2$ . The value above 12.5 mm is specified as  $\pm 0.5$ .

| Pin No. | Pin Name        | Pin No. | Pin Name        | Pin No. | Pin Name        | Pin No. | Pin Name        | Pin No. | Pin Name        |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1       | V <sub>SS</sub> | 16      | A4              | 31      | A8              | 46      | NC              | 61      | DQ13            |
| 2       | DQ0             | 17      | A5              | 32      | A9              | 47      | WE              | 62      | DQ30            |
| 3       | DQ16            | 18      | A6              | 33      | RAS3            | 48      | NC              | 63      | DQ14            |
| 4       | DQ1             | 19      | NC              | 34      | RAS2            | 49      | DQ8             | 64      | DQ31            |
| 5       | DQ17            | 20      | DQ4             | 35      | NC              | 50      | DQ24            | 65      | DQ15            |
| 6       | DQ2             | 21      | DQ20            | 36      | NC              | 51      | DQ9             | 66      | NC              |
| 7       | DQ18            | 22      | DQ5             | 37      | NC              | 52      | DQ25            | 67      | PD1             |
| 8       | DQ3             | 23      | DQ21            | 38      | NC              | 53      | DQ10            | 68      | PD2             |
| 9       | DQ19            | 24      | DQ6             | 39      | V <sub>SS</sub> | 54      | DQ26            | 69      | PD3             |
| 10      | V <sub>CC</sub> | 25      | DQ22            | 40      | CAS0            | 55      | DQ11            | 70      | PD4             |
| 11      | NC              | 26      | DQ7             | 41      | CAS2            | 56      | DQ27            | 71      | NC              |
| 12      | A0              | 27      | DQ23            | 42      | CAS3            | 57      | DQ12            | 72      | V <sub>SS</sub> |
| 13      | A1              | 28      | A7              | 43      | CAS1            | 58      | DQ28            |         |                 |
| 14      | A2              | 29      | NC              | 44      | RAS0            | 59      | V <sub>CC</sub> |         |                 |
| 15      | A3              | 30      | V <sub>CC</sub> | 45      | RAS1            | 60      | DQ29            |         |                 |

## Presence Detect Pins

| Pin No. | Pin Name | MSC23232C/CL-60BS16/DS16 | MSC23232C/CL-70BS16/DS16 | MSC23232C/CL-80BS16/DS16 |
|---------|----------|--------------------------|--------------------------|--------------------------|
| 67      | PD1      | NC                       | NC                       | NC                       |
| 68      | PD2      | NC                       | NC                       | NC                       |
| 69      | PD3      | NC                       | V <sub>SS</sub>          | NC                       |
| 70      | PD4      | NC                       | NC                       | V <sub>SS</sub>          |

# BLOCK DIAGRAM



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

| Parameter                                                  | Symbol                             | Rating      | Unit |
|------------------------------------------------------------|------------------------------------|-------------|------|
| Voltage on Any Pin Relative to V <sub>SS</sub>             | V <sub>IN</sub> , V <sub>OUT</sub> | -1.0 to 7.0 | V    |
| Voltage V <sub>CC</sub> Supply Relative to V <sub>SS</sub> | V <sub>CC</sub>                    | -1.0 to 7.0 | V    |
| Short Circuit Output Current                               | I <sub>OS</sub>                    | 50          | mA   |
| Power Dissipation                                          | P <sub>D</sub>                     | 16          | W    |
| Operating Temperature                                      | T <sub>opr</sub>                   | 0 to 70     | °C   |
| Storage Temperature                                        | T <sub>stg</sub>                   | -40 to 125  | °C   |

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

(Ta = 0°C to 70°C)

| Parameter            | Symbol          | Min. | Typ. | Max. | Unit |
|----------------------|-----------------|------|------|------|------|
| Power Supply Voltage | V <sub>CC</sub> | 4.5  | 5.0  | 5.5  | V    |
|                      | V <sub>SS</sub> | 0    | 0    | 0    | V    |
| Input High Voltage   | V <sub>IH</sub> | 2.4  | —    | 6.5  | V    |
| Input Low Voltage    | V <sub>IL</sub> | -1.0 | —    | 0.8  | V    |

**Capacitance**

(Ta = 25°C, f = 1 MHz)

| Parameter                             | Symbol           | Typ. | Max. | Unit |
|---------------------------------------|------------------|------|------|------|
| Input Capacitance (A0 - A9)           | C <sub>IN1</sub> | —    | 109  | pF   |
| Input Capacitance ( $\overline{WE}$ ) | C <sub>IN2</sub> | —    | 125  | pF   |
| Input Capacitance (RAS0 - RAS3)       | C <sub>IN3</sub> | —    | 35   | pF   |
| Input Capacitance (CAS0 - CAS3)       | C <sub>IN4</sub> | —    | 35   | pF   |
| I/O Capacitance (DQ0 - DQ31)          | C <sub>DQ</sub>  | —    | 20   | pF   |

Note : Capacitance measured with Boonton Meter.

## DC Characteristics

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C)

(V<sub>CC</sub> = 5 V ± 10%, I<sub>A</sub> = 0 V to 70 °C)

| Parameter                                                                                            | Symbol            | Condition                                                                                                              | MSC23232C/CL<br>-60BS16/DS16 |                 | MSC23232C/CL<br>-70BS16/DS16 |                 | MSC23232C/CL<br>-80BS16/DS16 |                 | Unit | Note         |
|------------------------------------------------------------------------------------------------------|-------------------|------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|------------------------------|-----------------|------------------------------|-----------------|------|--------------|
|                                                                                                      |                   |                                                                                                                        | Min.                         | Max.            | Min.                         | Max.            | Min.                         | Max.            |      |              |
|                                                                                                      |                   |                                                                                                                        |                              |                 |                              |                 |                              |                 |      |              |
| Input Leakage Current                                                                                | I <sub>LI</sub>   | 0 V ≤ V <sub>I</sub> ≤ 6.5 V;<br>All other pins not<br>under test = 0 V                                                | -160                         | 160             | -160                         | 160             | -160                         | 160             | μA   |              |
| Output Leakage Current                                                                               | I <sub>LO</sub>   | D <sub>OUT</sub> disable<br>0 V ≤ V <sub>O</sub> ≤ 5.5 V                                                               | -20                          | 20              | -20                          | 20              | -20                          | 20              | μA   |              |
| Output High Voltage                                                                                  | V <sub>OH</sub>   | I <sub>OH</sub> = -5.0 mA                                                                                              | 2.4                          | V <sub>CC</sub> | 2.4                          | V <sub>CC</sub> | 2.4                          | V <sub>CC</sub> | V    |              |
| Output Low Voltage                                                                                   | V <sub>OL</sub>   | I <sub>OL</sub> = 4.2 mA                                                                                               | 0                            | 0.4             | 0                            | 0.4             | 0                            | 0.4             | V    |              |
| Average Power<br>Supply Current<br>(Operating)                                                       | I <sub>CC1</sub>  | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling,<br>t <sub>RC</sub> = Min.                                   | —                            | 840             | —                            | 760             | —                            | 680             | mA   | 1, 2         |
| Power Supply<br>Current (Standby)                                                                    | I <sub>CC2</sub>  | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ = V <sub>IH</sub>                                                    | —                            | 32              | —                            | 32              | —                            | 32              | mA   | 1            |
|                                                                                                      |                   | $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$                                                                      | —                            | 16              | —                            | 16              | —                            | 16              | mA   | 1            |
|                                                                                                      |                   | ≥ V <sub>CC</sub> - 0.2 V                                                                                              | —                            | 3.2             | —                            | 3.2             | —                            | 3.2             | mA   | 1, 5         |
| Average Power<br>Supply Current<br>( $\overline{\text{RAS}}$ -only Refresh)                          | I <sub>CC3</sub>  | $\overline{\text{RAS}}$ cycling,<br>$\overline{\text{CAS}}$ = V <sub>IH</sub> ,<br>t <sub>RC</sub> = Min.              | —                            | 840             | —                            | 760             | —                            | 680             | mA   | 1, 2         |
| Average Power<br>Supply Current<br>( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh) | I <sub>CC6</sub>  | $\overline{\text{RAS}}$ cycling,<br>$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ ,<br>t <sub>RC</sub> = Min. | —                            | 840             | —                            | 760             | —                            | 680             | mA   | 1, 2         |
| Average Power<br>Supply Current<br>(Fast Page Mode)                                                  | I <sub>CC7</sub>  | $\overline{\text{RAS}}$ = V <sub>IL</sub> ,<br>$\overline{\text{CAS}}$ cycling,<br>t <sub>PC</sub> = Min.              | —                            | 680             | —                            | 600             | —                            | 520             | mA   | 1, 3         |
| Average Power<br>Supply Current<br>(Battery Backup)                                                  | I <sub>CC10</sub> | t <sub>RC</sub> = 125 μs,<br>$\overline{\text{CAS}}$ before<br>$\overline{\text{RAS}}$ cycling                         | —                            | 4.8             | —                            | 4.8             | —                            | 4.8             | mA   | 1, 2<br>4, 5 |

- Notes: 1. Specified values are obtained with the output open.  
2. Address can be changed once or less while  $\overline{\text{RAS}}$  = V<sub>IL</sub>.  
3. Address can be changed once or less while  $\overline{\text{CAS}}$  = V<sub>IH</sub>.  
4. V<sub>CC</sub> - 0.2 V ≤ V<sub>IH</sub> ≤ 6.5 V, -1.0 V ≤ V<sub>IL</sub> ≤ 0.2 V.  
5. L-version.

## AC Characteristics (1/2)

(V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1,2,3,9,10

| Parameter                                                         | Symbol            | MSC23232C/CL<br>-60BS16/DS16 |      | MSC23232C/CL<br>-70BS16/DS16 |      | MSC23232C/CL<br>-80BS16/DS16 |      | Unit | Note    |
|-------------------------------------------------------------------|-------------------|------------------------------|------|------------------------------|------|------------------------------|------|------|---------|
|                                                                   |                   | Min.                         | Max. | Min.                         | Max. | Min.                         | Max. |      |         |
|                                                                   |                   |                              |      |                              |      |                              |      |      |         |
| Random Read or Write Cycle Time                                   | t <sub>RC</sub>   | 110                          | —    | 130                          | —    | 150                          | —    | ns   |         |
| Fast Page Mode Cycle Time                                         | t <sub>PC</sub>   | 40                           | —    | 45                           | —    | 50                           | —    | ns   |         |
| Access Time from $\overline{\text{RAS}}$                          | t <sub>RAC</sub>  | —                            | 60   | —                            | 70   | —                            | 80   | ns   | 4, 5, 6 |
| Access Time from $\overline{\text{CAS}}$                          | t <sub>CAC</sub>  | —                            | 15   | —                            | 20   | —                            | 20   | ns   | 4, 5    |
| Access Time from Column Address                                   | t <sub>AA</sub>   | —                            | 30   | —                            | 35   | —                            | 40   | ns   | 4, 6    |
| Access Time from $\overline{\text{CAS}}$ Precharge                | t <sub>CPA</sub>  | —                            | 35   | —                            | 40   | —                            | 45   | ns   | 4       |
| Output Low Impedance Time from $\overline{\text{CAS}}$            | t <sub>CLZ</sub>  | 0                            | —    | 0                            | —    | 0                            | —    | ns   | 4       |
| Output Buffer Turn-off Delay Time                                 | t <sub>OFF</sub>  | 0                            | 15   | 0                            | 20   | 0                            | 20   | ns   | 7       |
| Transition Time                                                   | t <sub>T</sub>    | 3                            | 50   | 3                            | 50   | 3                            | 50   | ns   | 3       |
| Refresh Period                                                    | t <sub>REF</sub>  | —                            | 16   | —                            | 16   | —                            | 16   | ms   |         |
| Refresh Period (L-version)                                        | t <sub>REF</sub>  | —                            | 128  | —                            | 128  | —                            | 128  | ms   |         |
| $\overline{\text{RAS}}$ Precharge Time                            | t <sub>RP</sub>   | 40                           | —    | 50                           | —    | 60                           | —    | ns   |         |
| $\overline{\text{RAS}}$ Pulse Width                               | t <sub>RAS</sub>  | 60                           | 10K  | 70                           | 10K  | 80                           | 10K  | ns   |         |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)              | t <sub>RASP</sub> | 60                           | 100K | 70                           | 100K | 80                           | 100K | ns   |         |
| $\overline{\text{RAS}}$ Hold Time                                 | t <sub>RSH</sub>  | 15                           | —    | 20                           | —    | 20                           | —    | ns   |         |
| $\overline{\text{CAS}}$ Precharge Time                            | t <sub>CP</sub>   | 10                           | —    | 10                           | —    | 10                           | —    | ns   |         |
| $\overline{\text{CAS}}$ Pulse Width                               | t <sub>CAS</sub>  | 15                           | 10K  | 20                           | 10K  | 20                           | 10K  | ns   |         |
| $\overline{\text{CAS}}$ Hold Time                                 | t <sub>CSH</sub>  | 60                           | —    | 70                           | —    | 80                           | —    | ns   |         |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | t <sub>CRP</sub>  | 5                            | —    | 5                            | —    | 5                            | —    | ns   |         |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time     | t <sub>RCD</sub>  | 20                           | 45   | 20                           | 50   | 20                           | 60   | ns   | 5       |
| $\overline{\text{RAS}}$ to Column Address Delay Time              | t <sub>RAD</sub>  | 15                           | 30   | 15                           | 35   | 15                           | 40   | ns   | 6       |
| Row Address Set-up Time                                           | t <sub>ASR</sub>  | 0                            | —    | 0                            | —    | 0                            | —    | ns   |         |
| Row Address Hold Time                                             | t <sub>RAH</sub>  | 10                           | —    | 10                           | —    | 10                           | —    | ns   |         |
| Column Address Set-up Time                                        | t <sub>ASC</sub>  | 0                            | —    | 0                            | —    | 0                            | —    | ns   |         |
| Column Address Hold Time                                          | t <sub>CAH</sub>  | 15                           | —    | 15                           | —    | 15                           | —    | ns   |         |
| Column Address Hold Time from $\overline{\text{RAS}}$             | t <sub>AR</sub>   | 50                           | —    | 55                           | —    | 60                           | —    | ns   |         |
| Column Address to $\overline{\text{RAS}}$ Lead Time               | t <sub>RAL</sub>  | 30                           | —    | 35                           | —    | 40                           | —    | ns   |         |

**AC Characteristics (2/2)**

 (V<sub>CC</sub> = 5 V ±10%, T<sub>a</sub> = 0°C to 70°C) Note 1,2,3,9,10

VCC = 5 V ±10%, TA = 0 °C to 70 °C Note 1,2,3,5,10

| Parameter                                                                                              | Symbol           | MSC23232C/CL |      | MSC23232C/CL |      | MSC23232C/CL |      | Unit | Note |
|--------------------------------------------------------------------------------------------------------|------------------|--------------|------|--------------|------|--------------|------|------|------|
|                                                                                                        |                  | -60BS16/DS16 |      | -70BS16/DS16 |      | -80BS16/DS16 |      |      |      |
|                                                                                                        |                  | Min.         | Max. | Min.         | Max. | Min.         | Max. |      |      |
| Read Command Set-up Time                                                                               | t <sub>RCS</sub> | 0            | —    | 0            | —    | 0            | —    | ns   |      |
| Read Command Hold Time                                                                                 | t <sub>RCH</sub> | 0            | —    | 0            | —    | 0            | —    | ns   | 8    |
| Read Command Hold Time referenced to $\overline{\text{RAS}}$                                           | t <sub>RRH</sub> | 0            | —    | 0            | —    | 0            | —    | ns   | 8    |
| Write Command Set-up Time                                                                              | t <sub>WCS</sub> | 0            | —    | 0            | —    | 0            | —    | ns   |      |
| Write Command Hold Time                                                                                | t <sub>WCH</sub> | 10           | —    | 10           | —    | 10           | —    | ns   |      |
| Write Command Hold Time from $\overline{\text{RAS}}$                                                   | t <sub>WCR</sub> | 45           | —    | 50           | —    | 60           | —    | ns   |      |
| Write Command Pulse Width                                                                              | t <sub>WP</sub>  | 10           | —    | 10           | —    | 10           | —    | ns   |      |
| Write Command to $\overline{\text{RAS}}$ Lead Time                                                     | t <sub>RWL</sub> | 15           | —    | 20           | —    | 20           | —    | ns   |      |
| Write Command to $\overline{\text{CAS}}$ Lead Time                                                     | t <sub>CWL</sub> | 15           | —    | 20           | —    | 20           | —    | ns   |      |
| Data-in Set-up Time                                                                                    | t <sub>DS</sub>  | 0            | —    | 0            | —    | 0            | —    | ns   |      |
| Data-in Hold Time                                                                                      | t <sub>DH</sub>  | 15           | —    | 15           | —    | 15           | —    | ns   |      |
| Data-in Hold Time from $\overline{\text{RAS}}$                                                         | t <sub>DHR</sub> | 50           | —    | 55           | —    | 60           | —    | ns   |      |
| CAS Active Delay Time from $\overline{\text{RAS}}$ Precharge                                           | t <sub>RPC</sub> | 5            | —    | 5            | —    | 5            | —    | ns   |      |
| $\overline{\text{RAS}}$ to CAS Set-up Time (CAS before $\overline{\text{RAS}}$ )                       | t <sub>CSR</sub> | 5            | —    | 5            | —    | 5            | —    | ns   |      |
| $\overline{\text{RAS}}$ to CAS Hold Time (CAS before $\overline{\text{RAS}}$ )                         | t <sub>CHR</sub> | 10           | —    | 10           | —    | 10           | —    | ns   |      |
| CAS Precharge Time (Refresh Counter Test)                                                              | t <sub>CPT</sub> | 30           | —    | 35           | —    | 40           | —    | ns   |      |
| $\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time (CAS before $\overline{\text{RAS}}$ ) | t <sub>WRP</sub> | 10           | —    | 10           | —    | 10           | —    | ns   |      |
| $\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ (CAS before $\overline{\text{RAS}}$ )    | t <sub>WRH</sub> | 10           | —    | 10           | —    | 10           | —    | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)                              | t <sub>WTS</sub> | 10           | —    | 10           | —    | 10           | —    | ns   |      |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)                                | t <sub>WTH</sub> | 10           | —    | 10           | —    | 10           | —    | ns   |      |

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.  
When using the internal refresh counter, a minimum of eight  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  initialization cycles is required.
  2. AC measurement assume  $t_r = 5$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, access time is controlled by  $t_{AA}$ .
  7.  $t_{OFF}$  (Max.) defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
  8.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  9. The test mode is initiated by performing a  $\overline{\text{WE}}$  and  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operating state by performing a RAS-only refresh cycle or a  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh cycle.
  10. In a test mode read cycle, the access time parameters are delayed by 5 ns. The test mode parameters are obtained by adding 5 ns to the normal read cycle values.

**See ADDENDUM E for AC Timing Waveforms**