

PRELIMINARY

OKI Semiconductor

REVISION-2 1996.11.2

MSM54V16258A/SL

262,144-Word x 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO

DESCRIPTION

The MSM54V16258A/SL is a 262,144-word x 16-bit dynamic RAM fabricated in OKI's CMOS silicon gate technology. The MSM54V16258A/SL achieves high integration, high-speed operation, and low-power consumption due to quadruple polysilicon double metal CMOS. The MSM54V16258A/SL is available in a 40-pin plastic SOJ or 44/40-pin plastic TSOP.

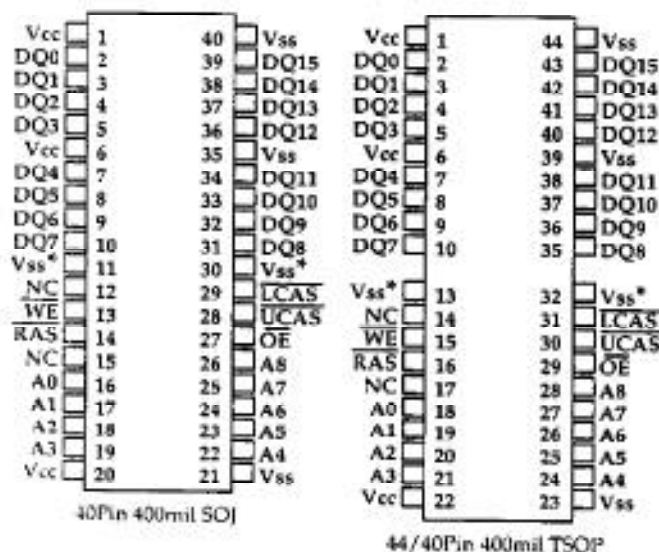
FEATURES

- 262,144-word x 16-bit configuration
 - Single 3.3V power supply, $\pm 0.3V$ tolerance
 - Input : LVTTTL compatible, low input capacitance
 - Output : LVTTTL compatible, 3-state
 - Refresh : 512 cycles/8ms
 - Fast page mode with EDO, read modify write capability
 - Byte wide control: 2 CAS control
 - CAS before RAS refresh, Hidden refresh, RAS only refresh capability
 - CAS before RAS self-refresh capability (SL version)
 - Package options:
 - 40-Pin 400 mil plastic SOJ (SOJ40-P-400) (Product : MSM54V16258A/SL-xx[S])
 - 44/40-Pin 400 mil plastic TSOP (TSOP44/40-P-400/0.8-K) (Product : MSM54V16258A/SL-xx[TS-K])
- xx indicates speed rank.

PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)		Power Dissipation
	t _{TRAC}	t _{AA}	t _{CAC}	t _{OEA}	t _{RC}	t _{HPC}	
MSM54V16258A/SL-40	40ns	22ns	10ns	10ns	80ns	15ns	50mW
MSM54V16258A/SL-45	45ns	24ns	12ns	12ns	90ns	17ns	450mW

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
A0-A8	Address Input
RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
DQ0-15	Data-Input/ Data-Output
WE	Write Enable
OE	Output Enable
Vcc	Power Supply (3.3V)
Vss	Ground (0V)
NC	No Connection
Vss*	Ground (0V) : see Note2

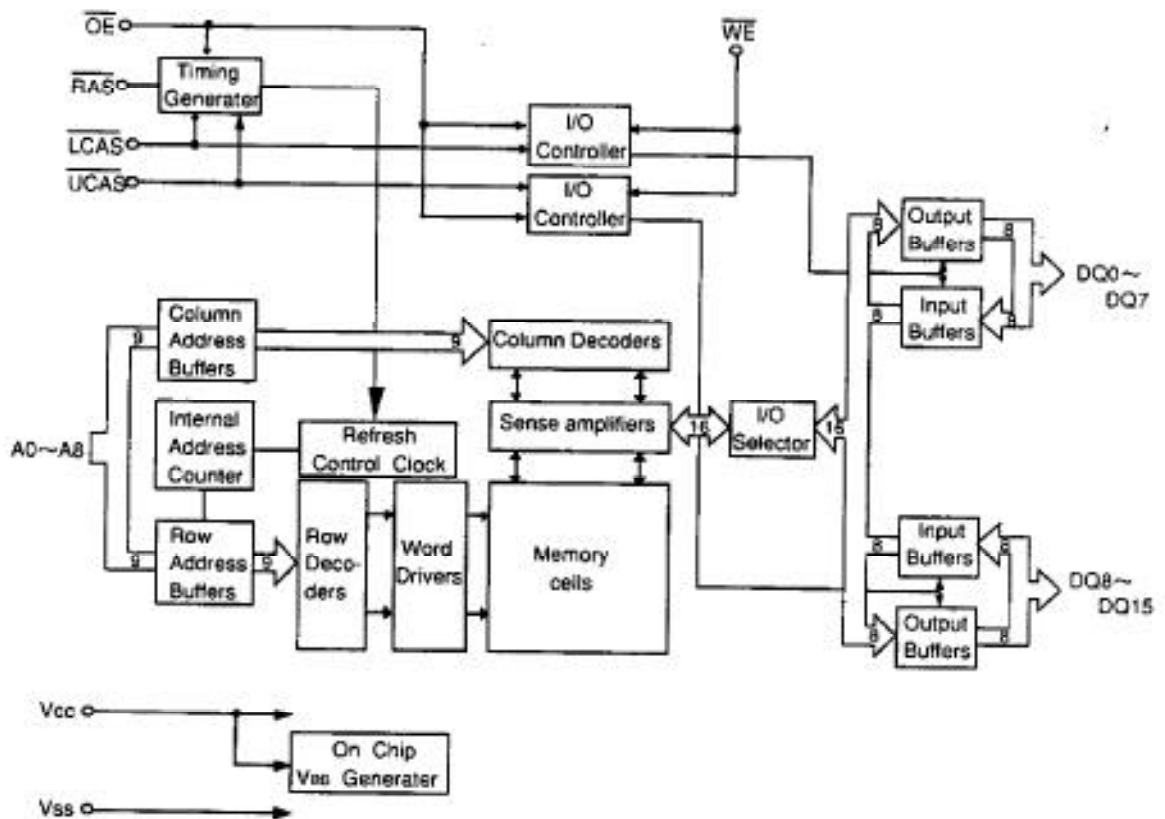
Note1 :

The same power supply voltage must be provided to every Vcc pin, and the same GND voltage level must be provided to every Vss pin.

Note2 :

For improved signal integrity, it is recommended to connect the Vss* pins, pin 11 and 31(SOJ) or pin 13 and 32(TSOP) to GND : the pins are electrically connected to internal GND.

BLOCK DIAGRAM



FUNCTION TABLE

Input Pin					DQPin		Functional Mode
\overline{RAS}	\overline{LCAS}	\overline{UCAS}	\overline{WE}	\overline{OE}	$DQ0 \sim DQ7$	$DQ8 \sim DQ15$	
H	•	•	•	•	High-Z	High-Z	Standby
L	H	H	•	•	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	Dout	Upper Byte Read
L	L	L	H	L	Dout	Dout	Word Read
L	L	H	L	H	Dw	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	Dw	Upper Byte Write
L	L	L	L	H	Dw	Dw	Word Write
L	L	L	H	H	High-Z	High-Z	—

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to Vss	Vt	Ta=25°C	-0.5~+4.6	V
Short circuit output current	Ios	Ta=25°C	50	mA
Power dissipation	Po	Ta=25°C	1	W
Operating temperature	Topt	—	0~+70	°C
Storage temperature	Tstg	—	-55~+150	°C

Recommended Operating Conditions

(Ta=0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	—	3.0	3.3	3.6	V
	Vss	—	0	0	0	V
Input high voltage	Vih	—	2.0	—	Vcc+0.3	V
Input low voltage	Vil	—	-0.3	—	0.8	V

Capacitance

(Vcc=3.3V±0.3V, Ta=25°C, f=1MHz)

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Input capacitance (A0~A8)	Cin1	—	—	8	pf
Input capacitance (RAS, LCAS, UCAS, WE, OE)	Cin2	—	—	8	pf
Input / output capacitance (DQ0~DQ15)	Cio	—	—	9	pf

DC CHARACTERISTICS

($V_{CC}=3.3V \pm 0.3V$, $T_a=0$ to $70^\circ C$)

Parameter	Symbol	Condition	MSM54V16258A /SL-40		MSM54V16258A /SL-45		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	$I_{OH} = 1.0mA$	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	$I_{OL} = 2.0mA$	0	0.4	0	0.4	V	
Input Leakage Current	I_{I1}	$0V \leq V_{IN} \leq V_{CC}$	-10	10	-10	10	μA	
Output Leakage Current	I_{IO}	DO Disable $0V \leq V_{O} \leq 3.6V$	-10	10	-10	10	μA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{RAS}, \overline{CAS}$ Cycling $t_{RC} = \text{Min.}$	—	140	—	125	mA	1,2
Power Supply Current (Standby)	I_{CC2}	$\overline{RAS}, \overline{CAS} = V_{IH}$	—	3	—	3	mA	1
Average Power Supply Current (\overline{RAS} only Refresh)	I_{CC3}	$\overline{RAS} = \text{Cycling}$ $\overline{CAS} = V_{IH}$ $t_{RC} = \text{Min.}$	—	140	—	125	mA	1,2
Average Power Supply Current (Fast Page Mode)	I_{CC4}	$\overline{RAS} = V_{IL}$ \overline{CAS} Cycling $t_{RC} = \text{Min.}$	—	140	—	125	mA	1,3
Average Power Supply Current (\overline{CAS} Before \overline{RAS} Refresh)	I_{CC5}	$\overline{RAS} = \text{Cycling}$ \overline{CAS} Before \overline{RAS}	—	140	—	125	mA	1,2
Average Power Supply Current (Battery Backup)	I_{CC6}	$t_{RC} = 125 \mu s$ \overline{CAS} Before \overline{RAS} $t_{RAS} \leq 1 \mu s$	—	300	—	300	μA	1,2,4,5
Average Power Supply Current (\overline{CAS} Before \overline{RAS} Self-refresh)	I_{CC7}	$\overline{RAS} \leq 0.2V$ $\overline{CAS} \leq 0.2V$	—	200	—	200	μA	1,2,4,5

- Notes : 1. I_{CC} Max. is specified as I_{CC} for the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.
 4. $V_{CC} - 0.2V \leq V_{IH} \leq 6.5V$, $-1.0V \leq V_{IL} \leq 0.2V$.
 5. SL version.

AC CHARACTERISTICS (1/2)

(V_{CC} = 3.3V ± 0.3V, T_a = 0~70°C)

Parameter	Symbol	MSM54V16258A (SL-40)		MSM54V16258A (SL-45)		Unit	Note
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t _{RC}	80	—	90	—	ns	
Read/Write cycle time	t _{RMW}	115	—	130	—	ns	
Hyper page mode cycle time	t _{HPC}	15	—	17	—	ns	
Fast page mode read/write cycle time	t _{FRMW}	55	—	60	—	ns	
Access time from $\overline{\text{RAS}}$	t _{TRAC}	—	40	—	45	ns	7,12,13
Access time from $\overline{\text{CAS}}$	t _{TCAC}	—	10	—	12	ns	7,12
Access time from column address	t _{TAA}	—	22	—	24	ns	7,13
Access time from $\overline{\text{OE}}$	t _{TEA}	—	10	—	12	ns	
Access time from $\overline{\text{CAS}}$ precharge	t _{CPA}	—	24	—	27	ns	7,12
Data hold after $\overline{\text{CAS}}$ low	t _{COH}	3	—	3	—	ns	17
Output buffer turn-off delay time	t _{OFF}	3	8	3	8	ns	8
$\overline{\text{OE}}$ to data output buffer turn-off delay time	t _{OEZ}	3	8	3	8	ns	8
$\overline{\text{RAS}}$ to data output buffer turn-off delay time	t _{REZ}	3	8	3	8	ns	8
$\overline{\text{WE}}$ to data output buffer turn-off delay time	t _{WEZ}	3	8	3	8	ns	8
Transition time	t _T	2	35	2	35	ns	
Refresh preiod	t _{REF}	—	8	—	8	ms	
$\overline{\text{RAS}}$ precharge time	t _{RP}	30	—	35	—	ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	40	10,000	45	10,000	ns	
$\overline{\text{RAS}}$ pulse width (Fast page mode)	t _{RASP}	40	100,000	45	100,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	8	—	10	—	ns	
$\overline{\text{RAS}}$ hold time reference to $\overline{\text{OE}}$	t _{ROH}	8	—	8	—	ns	
$\overline{\text{CAS}}$ precharge time	t _{CP}	5	—	6	—	ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	6	10,000	7	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	40	—	45	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCO}	18	30	18	33	ns	12
$\overline{\text{RAS}}$ to column address delay time	t _{RAO}	13	18	13	21	ns	
Row address set-up time	t _{ASR}	0	—	0	—	ns	13
Row address hold time	t _{AH}	8	—	8	—	ns	
Column address set-up time	t _{ASC}	0	—	0	—	ns	
Column address hold time	t _{CAH}	5	—	6	—	ns	
Column address hold time from $\overline{\text{RAS}}$	t _{AR}	30	—	30	—	ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	22	—	24	—	ns	
Read command set-up time	t _{RCS}	0	—	0	—	ns	9
Read command hold time	t _{RCH}	0	—	0	—	ns	
Read command hold time reference to $\overline{\text{RAS}}$	t _{RWH}	0	—	0	—	ns	9
$\overline{\text{WE}}$ pulse width	t _{WEP}	10	—	10	—	ns	

AC CHARACTERISTICS (2/2)

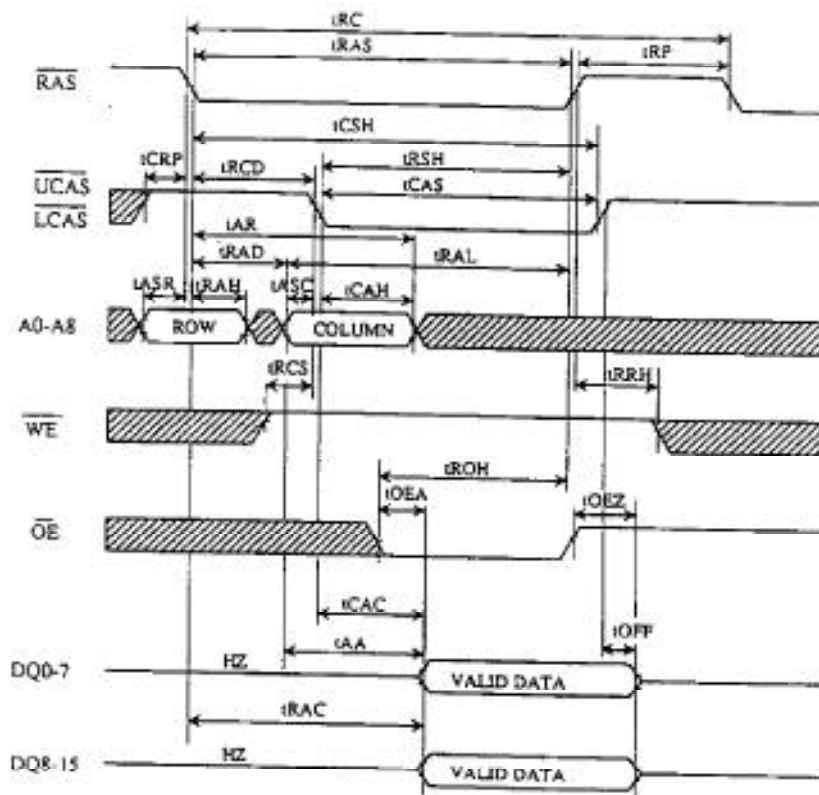
(V_{CC} = 3.3V ± 0.3V, T_a = 0–70°C)

Parameter	Symbol	MSM54V16258A /SL-40		MSM54V16258A /SL-45		Unit	Note
		MIN	MAX	MIN	MAX		
Write command set-up time	t _{WCS}	0	—	0	—	ns	
Write command hold time	t _{WCH}	7	—	8	—	ns	
Write command pulse width	t _{WP}	7	—	8	—	ns	
Write command hold time from $\overline{\text{RAS}}$	t _{WCR}	30	—	30	—	ns	
$\overline{\text{OE}}$ command hold time	t _{CEH}	7	—	8	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{OWL}	7	—	8	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	10	—	12	—	ns	
Data to $\overline{\text{CAS}}$ delay time	t _{ODC}	0	—	0	—	ns	
Data to $\overline{\text{OE}}$ delay time	t _{ODO}	0	—	0	—	ns	
Data-in set-up time	t _{OS}	0	—	0	—	ns	10
Data-in hold time	t _{OH}	6	—	7	—	ns	10
Data-in hold time referenced to $\overline{\text{RAS}}$	t _{OHRR}	20	—	20	—	ns	
$\overline{\text{OE}}$ to Data-in delay time	t _{CEB}	8	—	8	—	ns	
$\overline{\text{OE}}$ "L" to $\overline{\text{CAS}}$ "H" lead time	t _{CECH}	10	—	10	—	ns	
$\overline{\text{CAS}}$ "H" to $\overline{\text{OE}}$ "L" lead time	t _{CHCO}	10	—	10	—	ns	
Hi-Z command pulse width	t _{CEP}	10	—	10	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t _{OWD}	26	—	30	—	ns	11
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	38	—	40	—	ns	11
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t _{RWD}	60	—	65	—	ns	11
$\overline{\text{CAS}}$ active delay time from $\overline{\text{RAS}}$ precharge	t _{RPC}	0	—	0	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ set-up time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CSR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ hold time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t _{CHR}	10	—	10	—	ns	
$\overline{\text{RAS}}$ Pulse Width ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RASS}	100	—	100	—	ns	
$\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{RPS}	100	—	100	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self-Refresh)	t _{CHS}	-40	—	-40	—	ns	

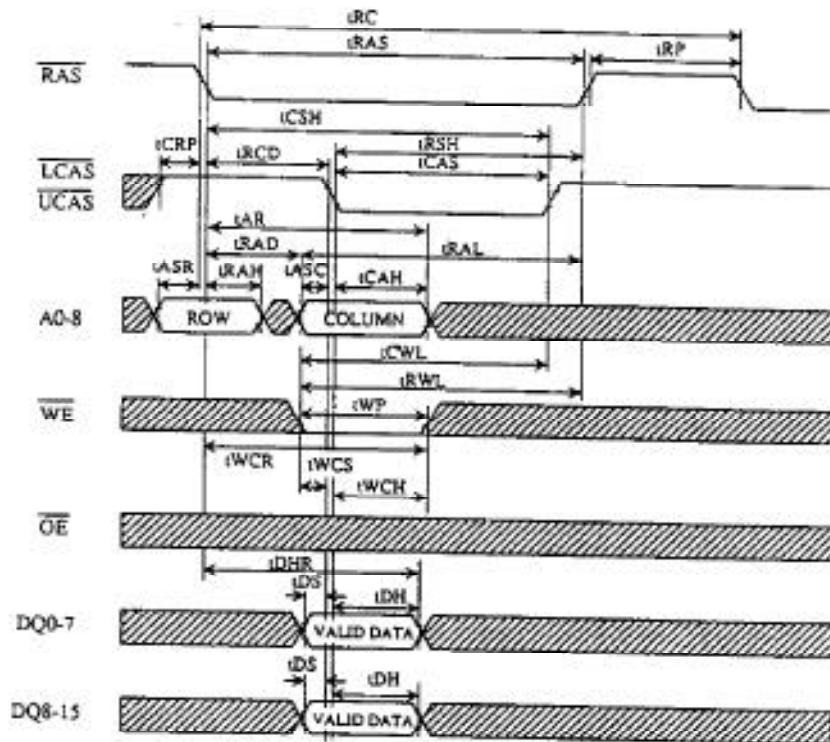
Notes:

1. All voltages are referenced to V_{SS} .
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of $200 \mu s$ is required after power-up, followed by any $8 \overline{RAS}$ cycles. (Example: \overline{RAS} -only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of $8 \overline{CAS}$ before \overline{RAS} cycles instead of $8 \overline{RAS}$ cycles are required.
5. The AC characteristics assume $t_r=5ns$.
6. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Data outputs are measured with a load of $50 pF$. DOUT reference levels: $V_{OH}/V_{OL}=2.0V/1.4V$. Note that V_{OL} is defined as $1.4V$ when V_{SS}^* pins, pin 11 and pin 30, were open. The data output measurements under $V_{OH}/V_{OL}=2.0V/0.8V$ are guaranteed when V_{SS}^* pins, pin 11 and 30(SOJ) or pin 13 and 32(TSOP) were connected to GND.
8. t_{OEZ} (Max.), t_{OF} (Max.), t_{WZ} (Max.) and t_{WZ} (Max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100 % tested.
9. Either t_{OCH} or t_{OHL} must be satisfied for a read cycle.
10. These parameters are referenced to \overline{CAS} leading edge of early write cycles and to \overline{WE} leading edge in OE-controlled write cycles and read-modify-write cycles.
11. t_{WCS} , t_{WDS} , t_{WOS} and t_{WWS} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{Min.})$, the cycle is an early write cycle and the data out pins will remain open circuit throughout the entire cycle. If $t_{WDS} \geq t_{WDS}(\text{Min.})$, $t_{WOS} \geq t_{WOS}(\text{Min.})$ and $t_{WWS} \geq t_{WWS}(\text{Min.})$, the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither or the above sets of conditions is satisfied, the condition of the data out is indeterminate.
12. Operation within the $t_{RCD}(\text{Max.})$ limit insures that $t_{RAC}(\text{Max.})$ can be met. $t_{RCD}(\text{Max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{Max.})$ limit, then access time is controlled by t_{RDC} .
13. Operation within the $t_{RAD}(\text{Max.})$ limit ensures that $t_{RAC}(\text{Max.})$ can be met. $t_{RAD}(\text{Max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{Max.})$ limit, then access time is controlled by t_{RAA} .
14. Input levels at the AC testing are $3.0V/0V$.
15. Addresses (A0 - A8) may be changed two times or less while $\overline{RAS} = V_{IL}$.
16. Addresses (A0 - A8) may be changed once or less while $\overline{CAS} = V_{IH}$ and $\overline{RAS} = V_{IL}$.
17. This is guaranteed by design. ($t_{COH}=t_{CAC}$ - output transition time). This parameter is not 100 % tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.

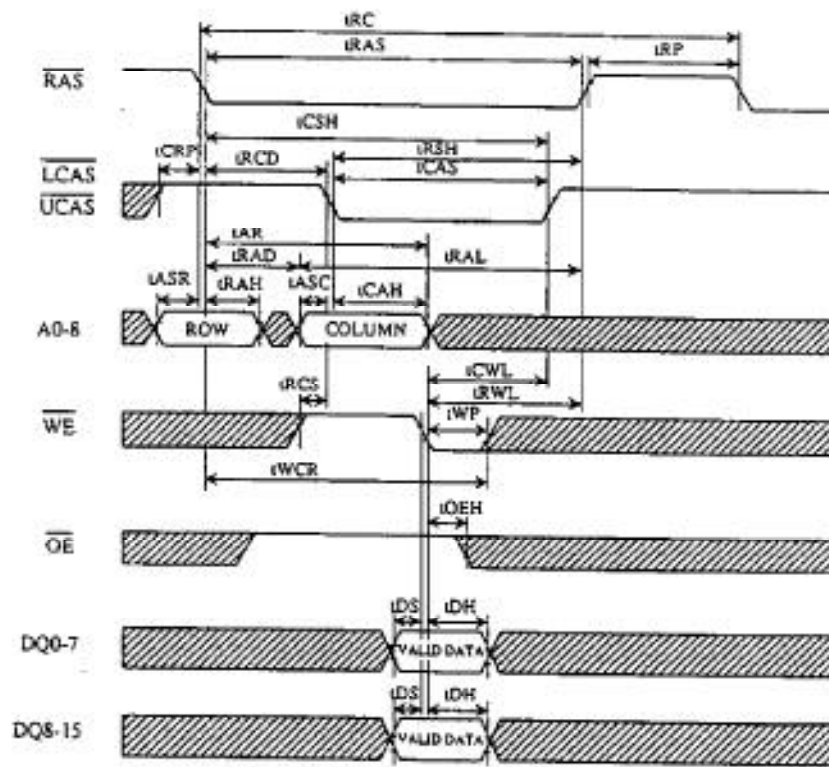
READ CYCLE ($\overline{\text{CAS}}$ output control)



EARLY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)

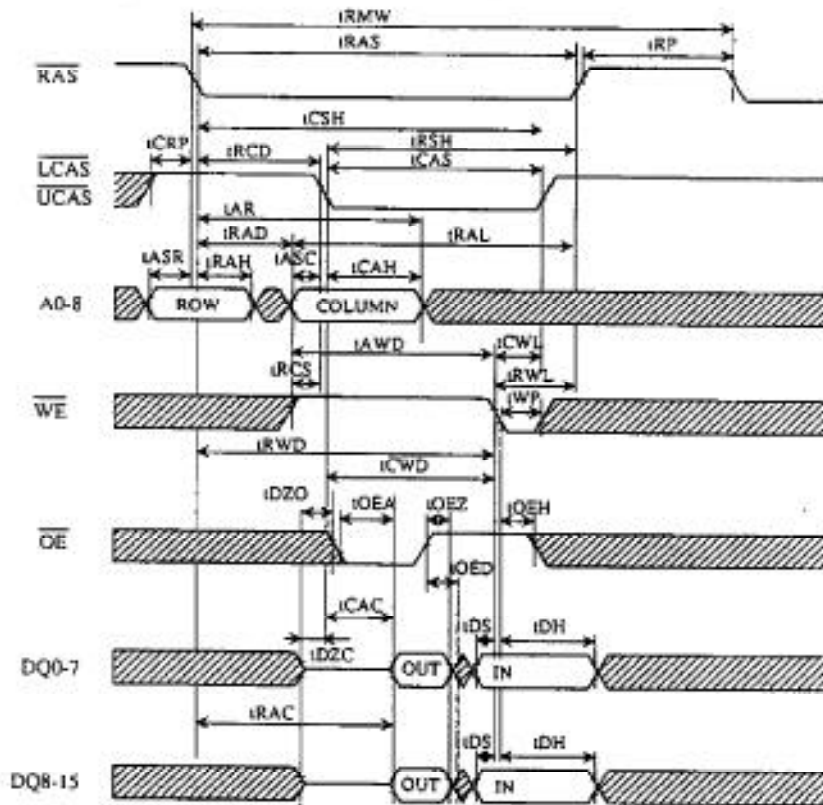


LATE WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)



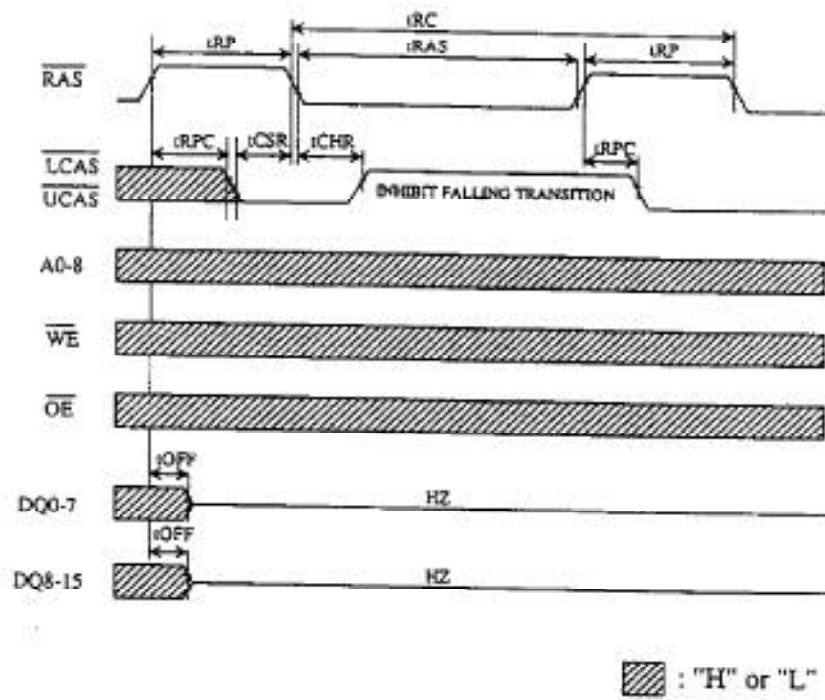
▨ : "H" or "L"

READ MODIFY WRITE CYCLE ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ active)

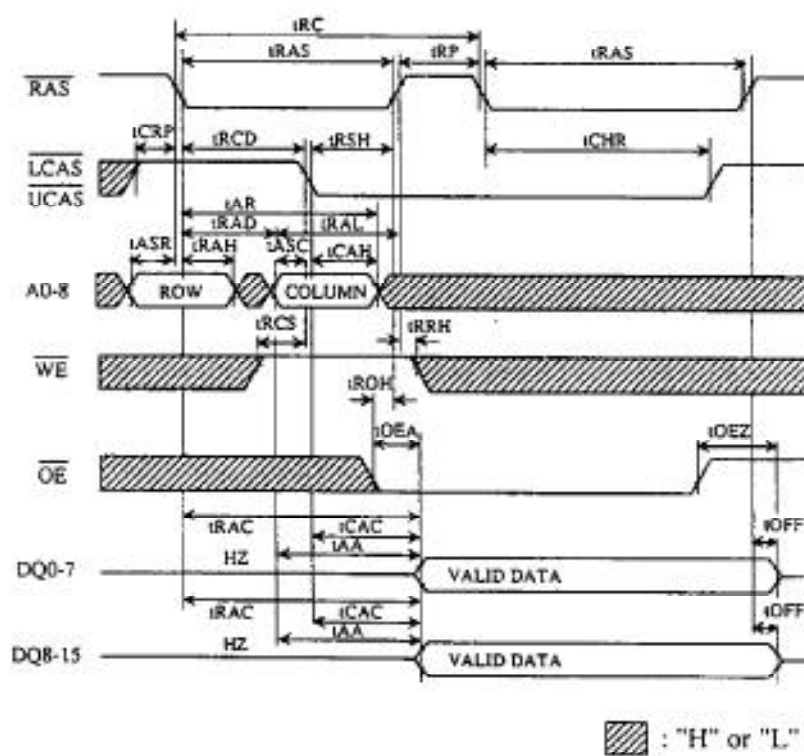


▨ : "H" or "L"

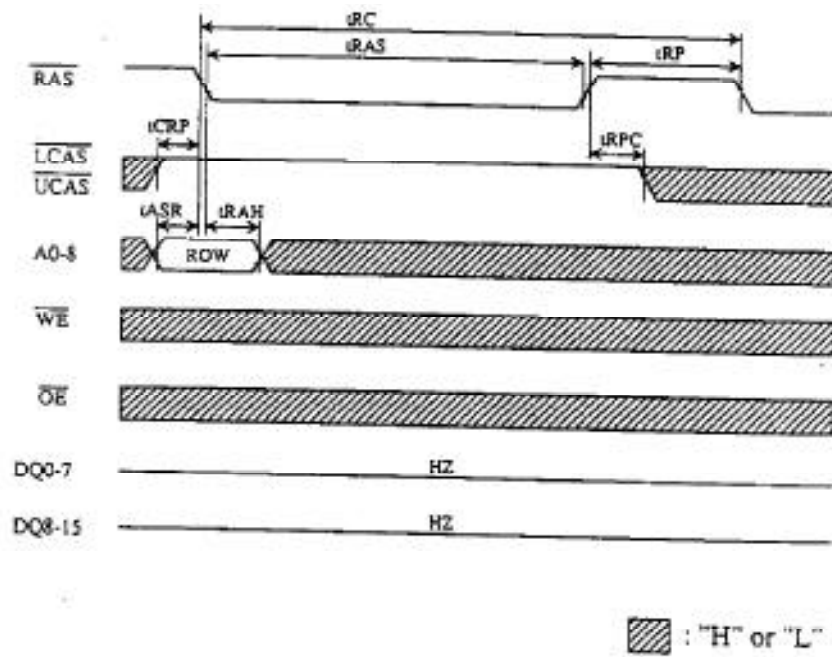
CAS BEFORE RAS REFRESH CYCLE



HIDDEN REFRESH CYCLE



RAS ONLY REFRESH CYCLE



CAS BEFORE RAS SELFREFRESH CYCLE

