

MSM64162D**4-Bit Microcontroller with Built-in RC Oscillation Type A/D Converter and LCD Driver****GENERAL DESCRIPTION**

The MSM64162D is a low power 4-bit microcontroller that employs Oki's original CPU core nX-4/20.

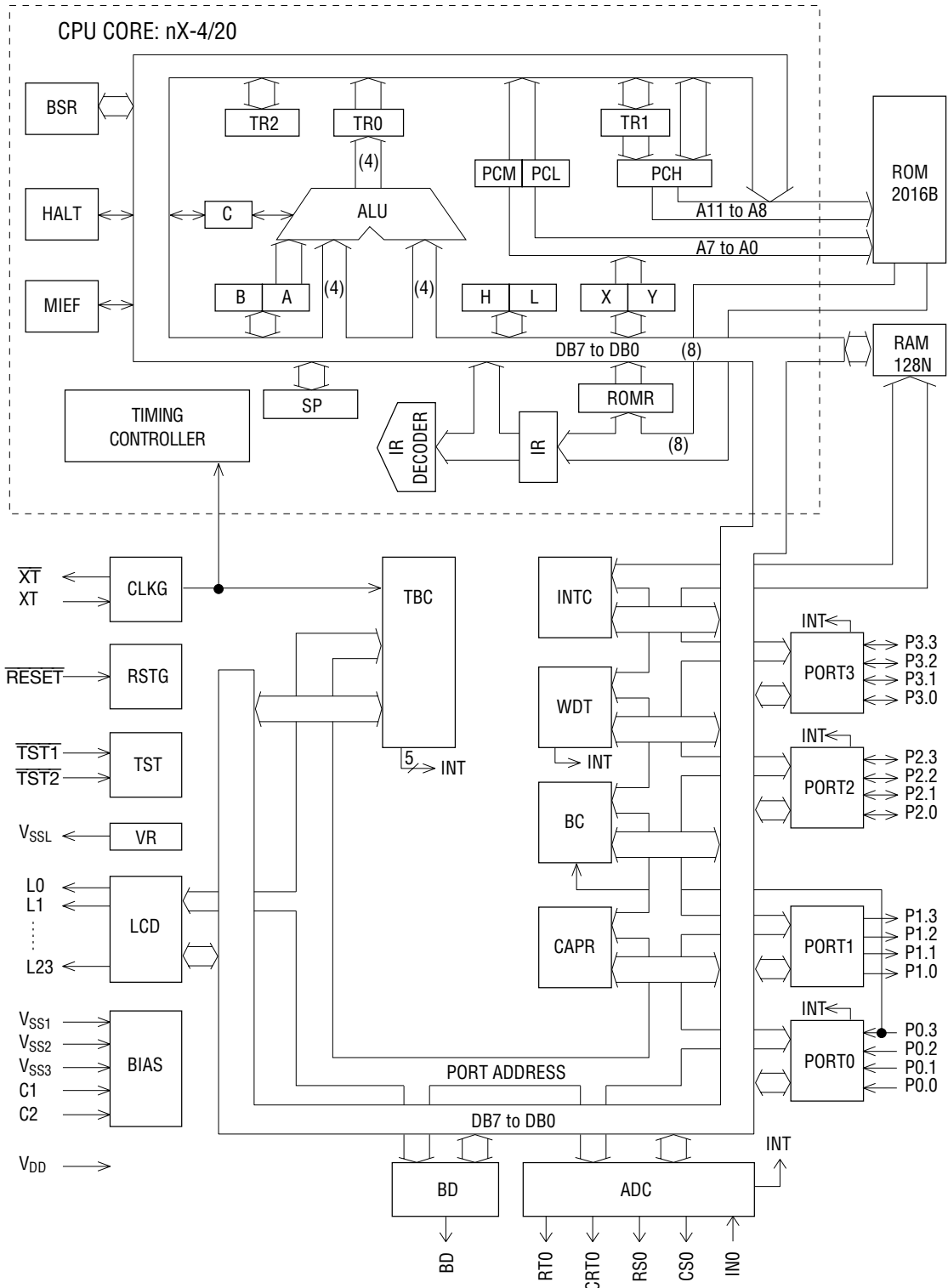
The MSM64162D has 1-channel RC oscillation type A/D converter, LCD driver for up to 80 segments, and buzzer output port. It is best suited for applications such as low power thermometers and clinical thermometers.

FEATURES

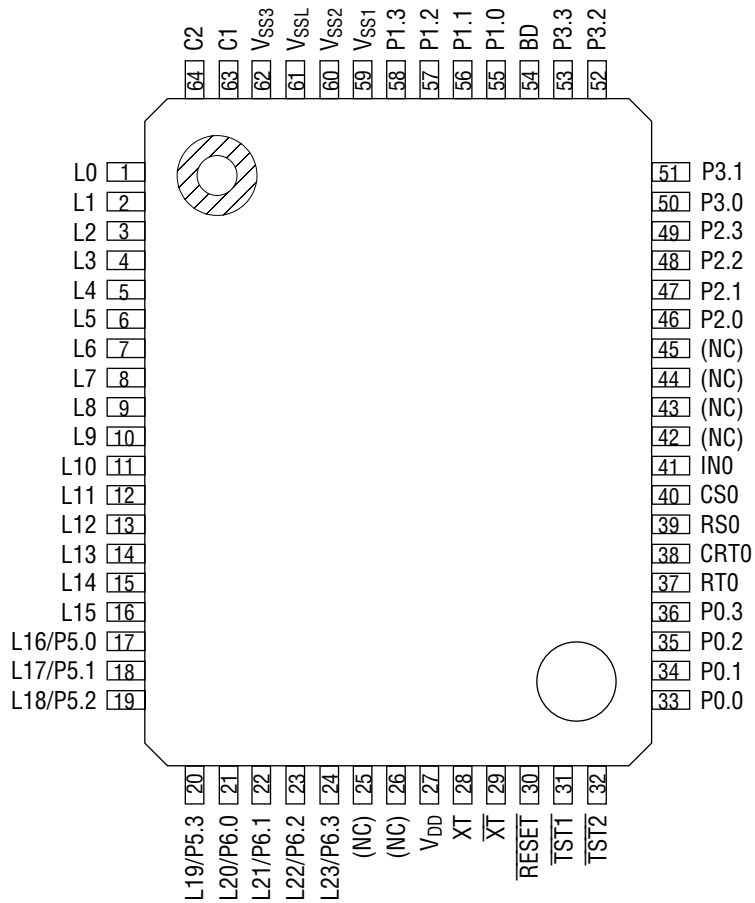
- Operating range
 - Operating frequencies : 32.768 kHz
 - Operating voltage : 1.25 to 1.7 V (1.5 V spec.)
2.0 to 3.5 V (3 V spec.)
2.2 to 3.5 V (3 V spec., 1/2 duty)
 - Operating temperature : -40 to +85°C
- Memory space
 - Internal program memory : 2016 bytes
 - Internal data memory : 128 nibbles
- Minimum instruction execution time : 91.6 μ s @ 32.768 kHz
- RC oscillation type A/D converter : 1 channel (2 sensors can be connected)
- LCD driver : 24 outputs; duty ratio switchable by software
 - (1) At 1/4 duty and 1/3 bias : 80 segments (max)
 - (2) At 1/3 duty and 1/3 bias : 63 segments (max)
 - (3) At 1/2 duty and 1/2 bias : 44 segments (max)
- Buzzer driver : 1 output (4 output modes selectable)
- Capture circuit : 2 channels
- Watchdog timer
- Clock : 32.768 kHz crystal oscillator
 - CPU clock : 32.768 kHz
 - Time base clock : 32.768 kHz
- Power supply voltage : 1.5 V/3 V (selectable by mask option)
- I/O port
 - Input-output port : 2 ports \times 4 bits
 - Input port : 1 port \times 4 bits
 - Output port : 1 port \times 4 bits
(8 out of the 24 LCD driver outputs can be used as output-only ports by mask option.)
- Interrupt sources
 - External interrupt : 2 sources
 - Internal interrupt : 7 sources
- Battery check circuit : 1 (incorporated into the input-only port)

- Package options:
 - 64-pin plastic QFP (QFP64-P-1420-1.00-BK) : (Product name : MSM64162D-××GS-BK)
 - 80-pin plastic QFP (QFP80-P-1420-0.80-BK) : (Product name : MSM64162D-××GS-BK-F)
 - Chip : (Product name : MSM64162D-××)
- ×× indicates a code number.

BLOCK DIAGRAM



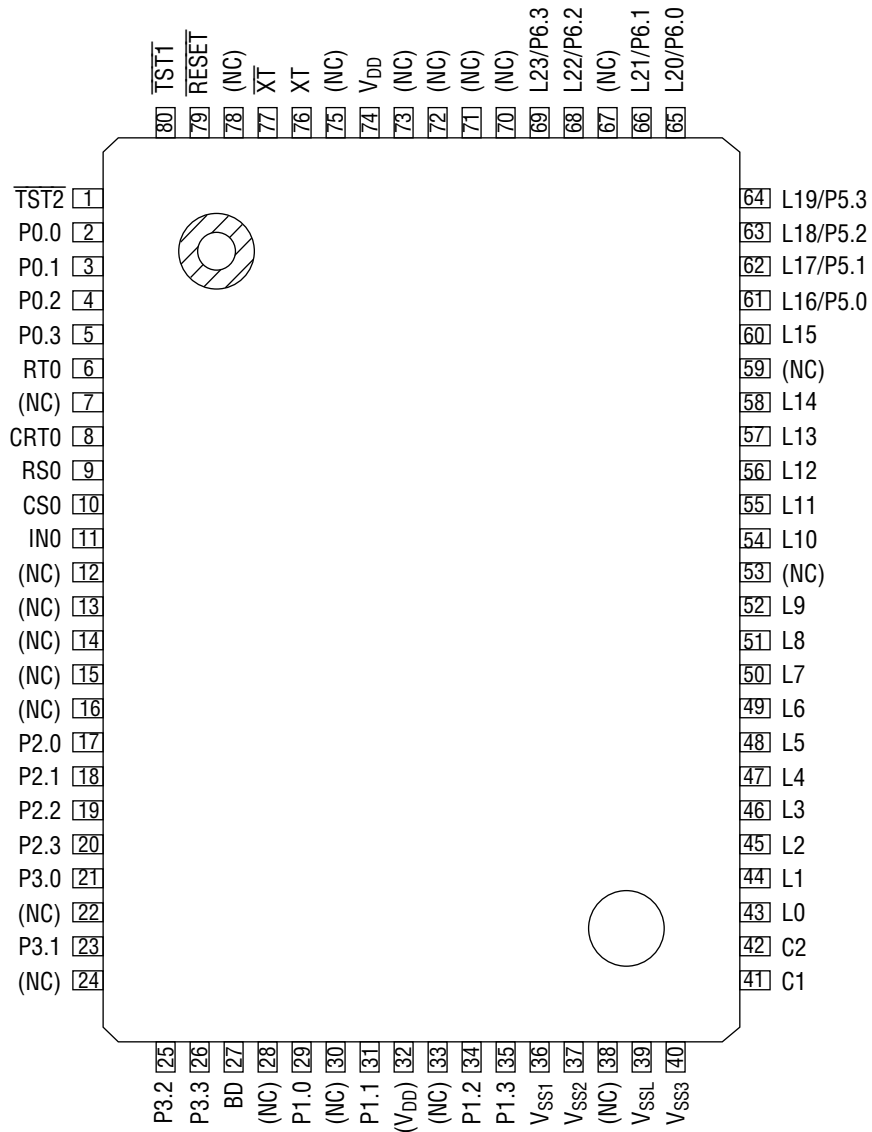
PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

Note: Pins marked as (NC) are no-connection pins which are left open.

PIN CONFIGURATION (TOP VIEW) (continued)

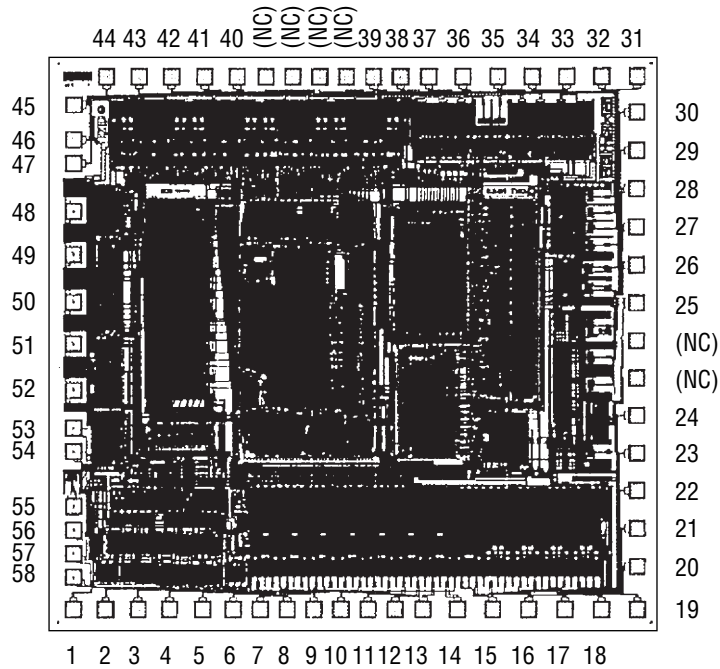


80-Pin Plastic QFP

- Notes: 1. Pins marked as (NC) are no-connection pins which are left open.
 2. V_{DD} should be supplied from pin 74. Pin 32 is internally connected to V_{DD}.

PAD CONFIGURATION

Pad Layout



Chip Size	: 4.69 mm × 4.41 mm
Chip Thickness	: 350 μm (typ.)
Coordinate Origin	: Chip center
Pad Hole Size	: 110 μm × 110 μm
Pad Size	: 130 μm × 130 μm
Minimum Pad Pitch	: 180 μm

Note: The chip substrate voltage is V_{DD} .

Pad Coordinates

Pad No.	Pad Name	X (μm)	Y (μm)	Pad No.	Pad Name	X (μm)	Y (μm)
1	L0	-2168	-2042	30	$\overline{\text{TST2}}$	2168	1766
2	L1	-1918	-2042	31	P0.0	2168	2042
3	L2	-1669	-2042	32	P0.1	1899	2042
4	L3	-1426	-2042	33	P0.2	1628	2042
5	L4	-1170	-2042	34	P0.3	1364	2042
6	L5	-934	-2042	35	RT0	1100	2042
7	L6	-727	-2042	36	CRT0	829	2042
8	L7	-519	-2042	37	RS0	565	2042
9	L8	-312	-2042	38	CS0	349	2042
10	L9	-104	-2042	39	IN0	141	2042
11	L10	104	-2042	40	P2.0	-911	2042
12	L11	311	-2042	41	P2.1	-1160	2042
13	L12	527	-2042	42	P2.2	-1416	2042
14	L13	791	-2042	43	P2.3	-1666	2042
15	L14	1062	-2042	44	P3.0	-1916	2042
16	L15	1340	-2042	45	P3.1	-2168	1829
17	L16/P5.0	1618	-2042	46	P3.2	-2168	1563
18	L17/P5.1	1897	-2042	47	P3.3	-2168	1382
19	L18/P5.2	2168	-2042	48	BD	-2168	1017
20	L19/P5.3	2168	-1714	49	P1.0	-2168	688
21	L20/P6.0	2168	-1424	50	P1.1	-2168	328
22	L21/P6.1	2168	-1134	51	P1.2	-2168	6
23	L22/P6.2	2168	-844	52	P1.3	-2168	-353
24	L23/P6.3	2168	-554	53	V _{SS1}	-2168	-645
25	V _{DD}	2168	316	54	V _{SS2}	-2168	-826
26	XT	2168	606	55	V _{SSL}	-2168	-1254
27	$\overline{\text{XT}}$	2168	896	56	V _{SS3}	-2168	-1435
28	$\overline{\text{RESET}}$	2168	1186	57	C1	-2168	-1616
29	$\overline{\text{TST1}}$	2168	1476	58	C2	-2168	-1796

PIN DESCRIPTIONS

Basic Functions

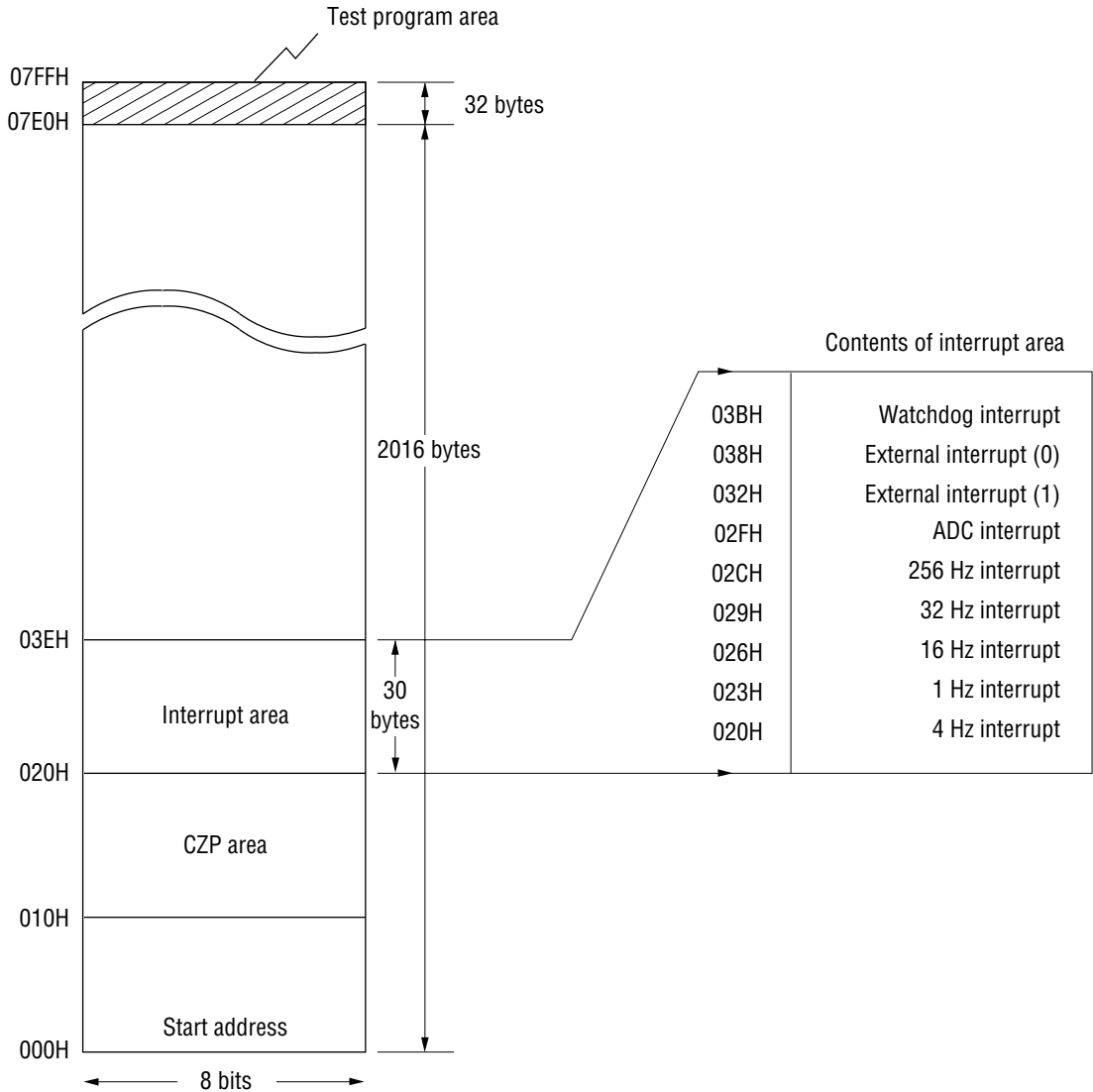
Function	Symbol	Type	Description
Power Supply	V _{DD}	—	0 V power supply
	V _{SS1}	—	Bias output for driving LCD (–1.5 V), or negative power supply at 1.5 V spec.
	V _{SS2}	—	Bias output for driving LCD (–3.0 V), or negative power supply at 3.0 V spec.
	V _{SS3}	—	Bias output for driving LCD (–4.5 V).
	V _{SSL}	—	Negative power supply pin for internal logic (internally generated constant voltage)
	C1, C2	—	Pins for connecting a capacitor for generating V _{SS1} , V _{SS2} , and V _{SS3} .
Oscillation	XT	I	32.768 kHz crystal connection pins
	\overline{XT}	O	
Ports	P1.0 to P1.3	O	Output port (P1.0 : high current output)
	P0.0 to P0.3	I	Input port
	P2.0 to P3.3	I/O	Input-output ports
	BD	O	Output pin for the buzzer driver
	L0 to L15	O	LCD driver pins
	L16/P5.0 to L23/P6.3	O	LCD driver pins, or output ports by mask option
A/D Converter	RT0	O	Resistance temperature sensor connection pin
	CRT0	O	Resistance/capacitance temperature sensor connection pin
	RS0	O	Reference resistor connection pin
	CS0	O	Reference capacitor connection pin
	INO	I	Input pin for RC oscillator circuit
Reset	\overline{RESET}	I	Reset pin
Test	$\overline{TST1}$	I	Input pins for testing
	$\overline{TST2}$	I	

Secondary Functions

Function	Symbol	Type	Description
RC Oscillation Monitor	P3.3	O	Monitor output pin (MON) for an RC oscillation clock.
Battery Check	P0.3	I	Analog comparator input pin for battery check.
External Interrupt	P3.0	I	Level-triggered external 0 interrupt input pins. The change of input signal level causes an interrupt to occur.
	P3.1	I	
	P3.2	I	
	P3.3	I	
	P2.0	I	
	P2.1	I	
	P2.2	I	
	P2.3	I	
	P0.0	I	
	P0.1	I	
	P0.2	I	
	P0.3	I	
	Capture	P0.0	I
P0.1		I	

MEMORY MAPS

Program Memory



Program Memory Map

Address 000H is the instruction execution start address by the system reset.

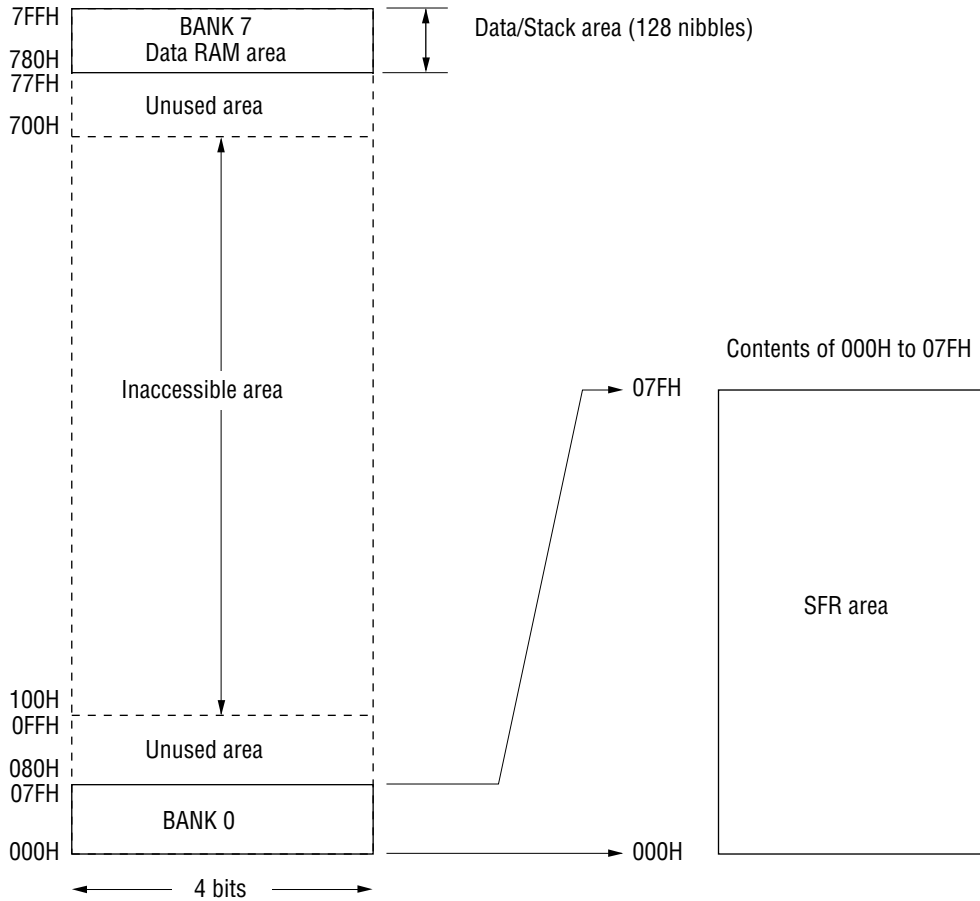
The CZP area from address 010H to address 01FH is the start address for the CZP subroutine of 1-byte call instruction.

The start address of interrupt subroutine is assigned to the interrupt address from address 020H to 03DH.

The user area has 2016 bytes of address 000H to address 07DFH. No program can be stored in the test program area.

Data Memory

The data memory area consists of 8 banks and each bank has 256 nibbles (256 × 4 bits). The data RAM is assigned to BANK 7 and peripheral ports are assigned to BANK 0.



Data Memory Map

The data RAM area (128 nibbles) is shared by the stack area. The stack is a memory starting from address 7FFH toward the low-order addresses where 4 nibbles are used by Subroutine Call Instruction and 8 nibbles are used by an interrupt.

The addresses 080H to 0FFH of BANK 0 and the addresses 700H to 77FH of BANK 7 are not assigned as the data memory, so access to these addresses has no effect. Moreover, it is impossible to access BANK 1 to BANK 6.

ABSOLUTE MAXIMUM RATINGS (1.5 V Spec.)(V_{DD} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{SS1}	Ta = 25°C	-2.0 to +0.3	V
Power Supply Voltage 2	V _{SS2}	Ta = 25°C	-4.0 to +0.3	V
Power Supply Voltage 3	V _{SS3}	Ta = 25°C	-5.5 to +0.3	V
Power Supply Voltage 4	V _{SSL}	Ta = 25°C	-2.0 to +0.3	V
Input Voltage 1	V _{IN1}	V _{SS1} Input, Ta = 25°C	V _{SS1} - 0.3 to +0.3	V
Input Voltage 2	V _{IN2}	V _{SSL} Input, Ta = 25°C	V _{SSL} - 0.3 to +0.3	V
Output Voltage 1	V _{OUT1}	V _{SS1} Output, Ta = 25°C	V _{SS1} - 0.3 to +0.3	V
Output Voltage 2	V _{OUT2}	V _{SS2} Output, Ta = 25°C	V _{SS2} - 0.3 to +0.3	V
Output Voltage 3	V _{OUT3}	V _{SS3} Output, Ta = 25°C	V _{SS3} - 0.3 to +0.3	V
Output Voltage 4	V _{OUT4}	V _{SSL} Output, Ta = 25°C	V _{SSL} - 0.3 to +0.3	V
Storage Temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (1.5 V Spec.)(V_{DD} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	-40 to +85	°C
Operating Voltage	V _{SS1}	—	-1.7 to -1.25	V
Crystal Oscillation Frequency	f _{XT}	—	30 to 35	kHz

ELECTRICAL CHARACTERISTICS (1.5 V Spec.)

DC Characteristics

($V_{DD} = 0\text{ V}$, $V_{SS1} = -1.5\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V_{SS2} Voltage	V_{SS2}	$C_a, C_b, C_{12} = 0.1\ \mu\text{F}$ +100% -50%	-3.2	-3.0	-2.8	V	1
V_{SS3} Voltage	V_{SS3}	$C_a, C_b, C_{12} = 0.1\ \mu\text{F}$ +100% -50%	-4.7	-4.5	-4.3	V	
V_{SSL} Voltage	V_{SSL}	—	-1.5	-1.3	-0.6	V	
Crystal Oscillation Start Voltage	V_{STA}	Oscillation start time: within 5 seconds	—	—	-1.45	V	
Crystal Oscillation Hold Voltage	V_{HOLD}	—	—	—	-1.25	V	
Crystal Oscillation Stop Detection Time	T_{STOP}	—	0.1	—	1000	ms	
Internal Crystal Oscillator Capacitance	C_G	—	10	15	20	pF	
External Crystal Oscillator Capacitance	C_{GEX}	When external C_G used	10	—	30	pF	
Internal Crystal Oscillator Capacitance	C_D	—	10	15	20	pF	
POR Generation Voltage	V_{POR1}	When V_{SS1} is between V_{POR1} and -1.5 V	-0.4	—	0	V	
POR Non-generation Voltage	V_{POR2}	No POR when V_{SS1} is between V_{POR2} and -1.5 V	-1.5	—	-1.2	V	
Battery Check Reference Voltage	V_{RB}	$T_a = 25^\circ\text{C}$	-0.73	-0.63	-0.53	V	
V_{RB} Temperature Variation	ΔV_{RB}	—	—	-2.0	—	mV/°C	

Notes: 1. "POR" denotes Power On Reset.

2. " T_{STOP} " indicates that if the crystal oscillator stops over the value of T_{STOP} , the system reset occurs.

DC Characteristics (continued)

(V_{DD} = 0 V, V_{SS1} = -1.5 V, T_a = -40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Supply Current 1	I _{DD1}	CPU in halt state	T _a = -40 to +40°C	—	2.0	5.0	μA	1
			T _a = +40 to +85°C	—	2.0	30	μA	
Supply Current 2	I _{DD2}	CPU in operating state	T _a = -40 to +40°C	—	5.0	15	μA	
			T _a = +40 to +85°C	—	5.0	40	μA	
Supply Current 3	I _{DD3}	CPU in halt state, RC oscillator for A/D converter is in operating state	RT0 = 10 kΩ	—	150	230	μA	
			RT0 = 2 kΩ	—	600	900	μA	
Supply Current 4	I _{DD4}	Battery check circuit in operating state, CPU in operating state	—	25	125	μA		

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P1.0)	I_{OH1}	$V_{OH1} = -0.5\text{ V}$	-2.1	-0.7	-0.2	mA	2
	I_{OL1}	$V_{OL1} = V_{SS1} + 0.5\text{ V}$	1.0	3.0	9.0	mA	
Output Current 2 (P1.1 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3)	I_{OH2}	$V_{OH2} = -0.5\text{ V}$	-2.1	-0.7	-0.2	mA	
	I_{OL2}	$V_{OL2} = V_{SS1} + 0.5\text{ V}$	0.2	0.7	2.1	mA	
Output Current 3 (BD)	I_{OH3}	$V_{OH3} = -0.7\text{ V}$	-1.8	-0.6	-0.2	mA	
	I_{OL3}	$V_{OL3} = V_{SS1} + 0.7\text{ V}$	0.2	0.6	1.8	mA	
Output Current 4 (RT0, RS0, CRT0, CS0)	I_{OH4}	$V_{OH4} = -0.1\text{ V}$	-1.1	-0.6	-0.3	mA	
	I_{OL4}	$V_{OL4} = V_{SS1} + 0.1\text{ V}$	0.3	0.6	1.1	mA	
Output Current 5 (When L16 to L23 are configured as output ports)	I_{OH5}	$V_{OH5} = -0.5\text{ V}$	-1.5	-0.5	-0.1	mA	
	I_{OL5}	$V_{OL5} = V_{SS1} + 0.5\text{ V}$	0.1	0.5	1.5	mA	
Output Current 6 (L0 to L23)	I_{OH6}	$V_{OH6} = -0.2\text{ V}$ (V_{DD} level)	—	—	-4.0	μA	
	I_{OMH6}	$V_{OMH6} = V_{SS1} + 0.2\text{ V}$ (V_{SS1} level)	4.0	—	—	μA	
	I_{OMH6S}	$V_{OMH6S} = V_{SS1} - 0.2\text{ V}$ (V_{SS1} level)	—	—	-4.0	μA	
	I_{OML6}	$V_{OML6} = V_{SS2} + 0.2\text{ V}$ (V_{SS2} level)	4.0	—	—	μA	
	I_{OML6S}	$V_{OML6S} = V_{SS2} - 0.2\text{ V}$ (V_{SS2} level)	—	—	-4.0	μA	
	I_{OL6}	$V_{OL6} = V_{SS3} + 0.2\text{ V}$ (V_{SS3} level)	4.0	—	—	μA	
Output Leakage Current (P1.0 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3) (RT0, RS0, CRT0, CS0)	I_{OOH}	$V_{OH} = V_{DD}$	—	—	0.3	μA	
	I_{OOL}	$V_{OL} = V_{SS1}$	-0.3	—	—	μA	

2

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

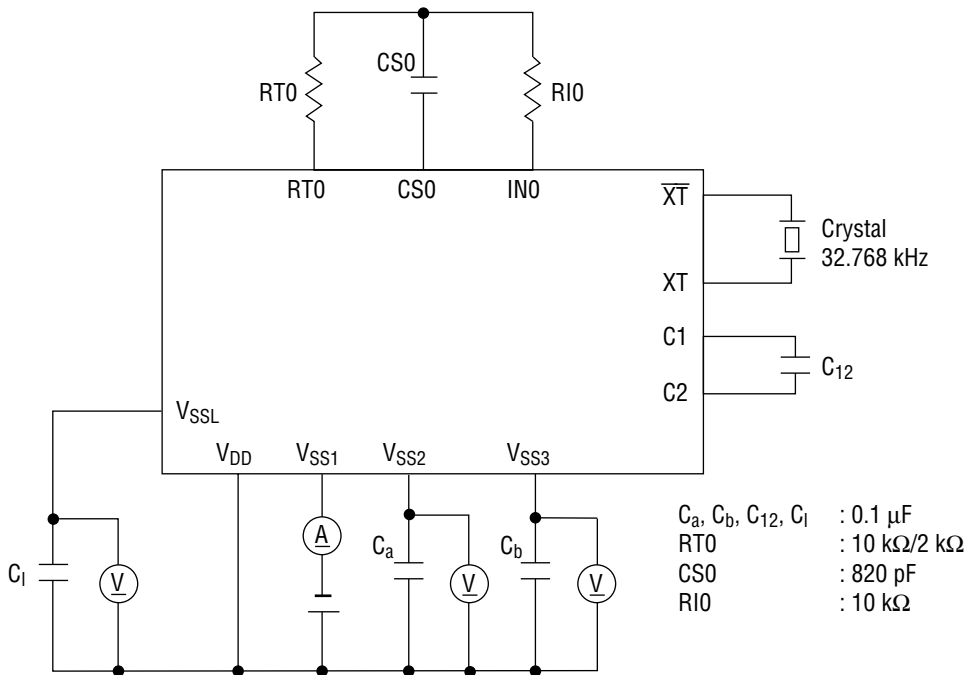
Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3) (P4.0 to P4.3)	I_{IH1}	$V_{IH1} = V_{DD}$ (when pulled down)	5	18	60	μA	3
	I_{IL1}	$V_{IL1} = V_{SS1}$ (when pulled up)	-60	-18	-5.0	μA	
	I_{IH1Z}	$V_{IH1} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL1Z}	$V_{IL1} = V_{SS1}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 2 (IN0)	I_{IH2}	$V_{IH2} = V_{DD}$ (when pulled down)	5	18	60	μA	3
	I_{IH2Z}	$V_{IH2} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL2Z}	$V_{IL2} = V_{SS1}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 3 (RESET, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	I_{IH3}	$V_{IH3} = V_{DD}$	0	—	1.0	μA	3
	I_{IL3}	$V_{IL3} = V_{SS1}$	-1.5	-0.75	-0.3	mA	
Input Voltage 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	V_{IH1}	—	-0.3	—	0	V	4
	V_{IL1}	—	-1.5	—	-1.2	V	
Input Voltage 2 (IN0)	V_{IH2}	—	-0.3	—	0	V	
	V_{IL2}	—	-1.5	—	-1.2	V	
Input Voltage 3 (RESET, $\overline{\text{TST1}}$, $\overline{\text{TST2}}$)	V_{IH3}	—	-0.3	—	0	V	
	V_{IL3}	—	-1.5	—	-1.2	V	

DC Characteristics (continued)

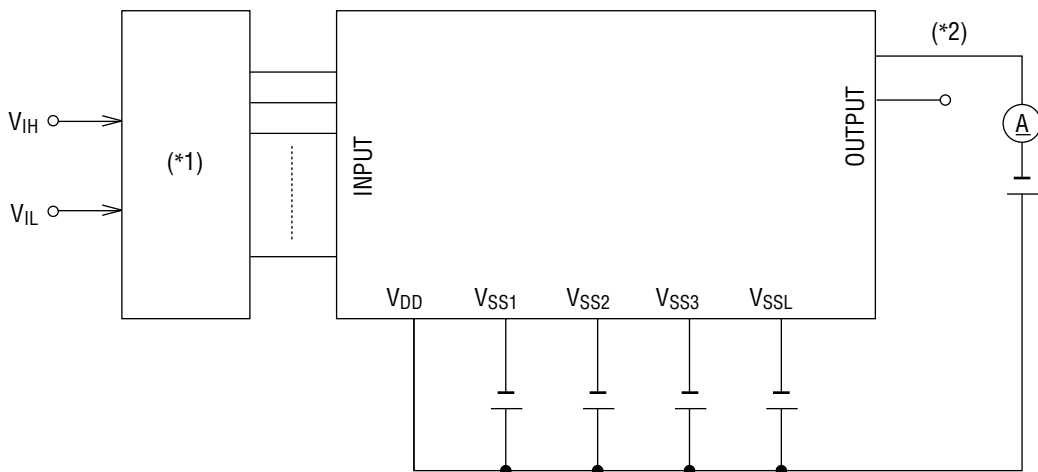
($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Hysteresis Width (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	ΔV_{T1}	—	0.05	0.1	0.3	V	4
Hysteresis Width (RESET, TST1, TST2)	ΔV_{T2}	—	0.05	0.1	0.3	V	
Input Pin Capacitance (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	C_{IN}	—	—	—	5.0	pF	1

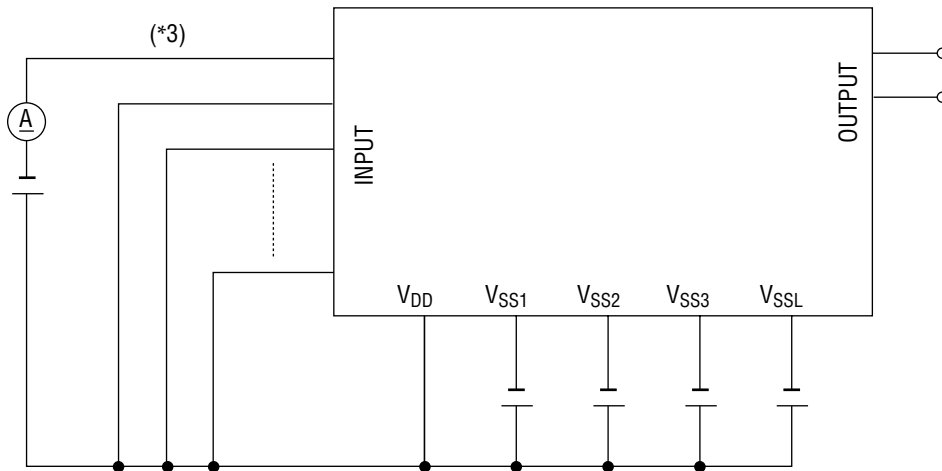
Measuring circuit 1



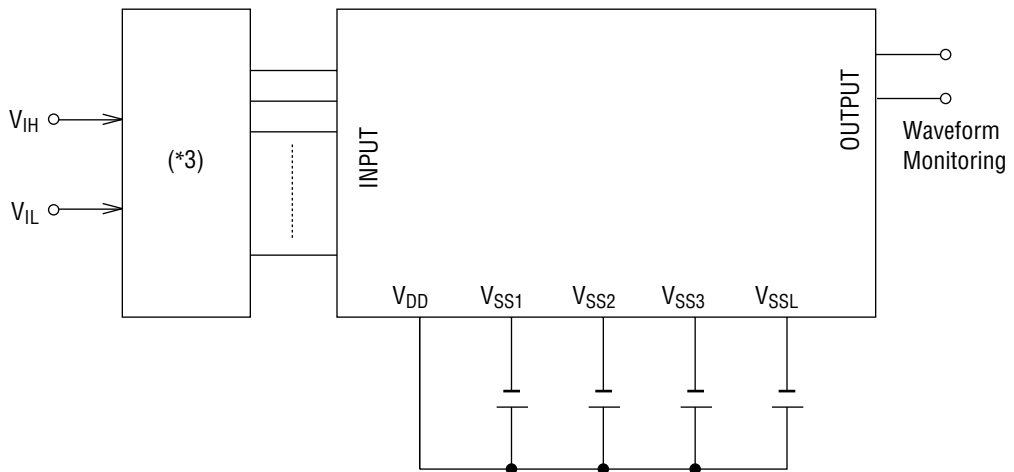
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



- *1 Input logic circuit to determine the specified measuring conditions.
- *2 Measured at the specified output pins.
- *3 Measured at the specified input pins.

A/D Converter Characteristics

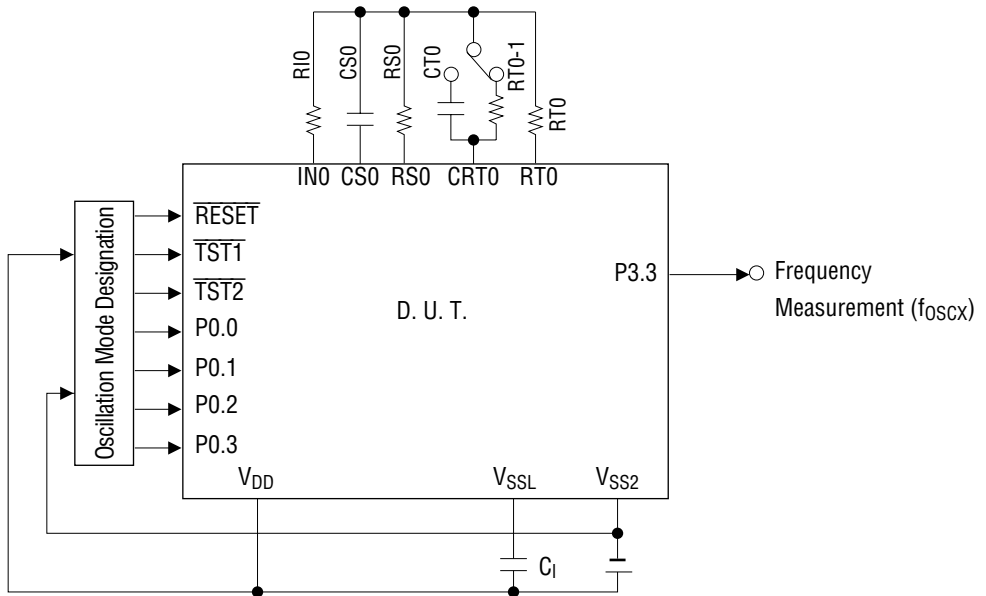
(V_{DD} = 0 V, V_{SS1} = -1.5 V, Ta = -40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Resistor for Oscillation	RS0, RT0, RT0-1	CS0, CT0 ≥ 740 pF	2.0	—	—	kΩ	5
Input Current Limiting Resistor	RI0	—	1.0	10	—	kΩ	
Oscillation Frequency	f _{osc1}	Resistor for oscillation = 2 kΩ	165	221	256	kHz	
	f _{osc2}	Resistor for oscillation = 10 kΩ	41.8	52.2	60.6	kHz	
	f _{osc3}	Resistor for oscillation = 200 kΩ	2.55	3.04	3.53	kHz	
RS•RT Oscillation Frequency Ratio (*)	Kf1	RT0, RT0-1 = 2 kΩ	3.89	4.18	4.35	—	
	Kf2	RT0, RT0-1 = 10 kΩ	0.990	1.0	1.010	—	
	Kf3	RT0, RT0-1 = 200 kΩ	0.0561	0.0584	0.0637	—	

* Kfx is the ratio of the oscillation frequency by a sensor resistor to the oscillation frequency by a reference resistor in the same condition.

$$Kfx = \frac{f_{oscx} \text{ (RT0-CS0 Oscillation)}}{f_{oscx} \text{ (RS0-CS0 Oscillation)}} , \frac{f_{oscx} \text{ (RT0-1-CS0 Oscillation)}}{f_{oscx} \text{ (RS0-CS0 Oscillation)}} \\ (x = 1, 2, 3)$$

Measuring circuit 5



- RT0, RT0-1 = 2 kΩ/10 kΩ/200 kΩ
- RS0 = 10 kΩ
- R10 = 10 kΩ
- CS0, CT0 = 820 pF
- C1 = 0.1 μF

ABSOLUTE MAXIMUM RATINGS (3.0 V Spec.)

(V_{DD} = 0 V)

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage 1	V _{SS1}	Ta = 25°C	-2.0 to +0.3	V
Power Supply Voltage 2	V _{SS2}	Ta = 25°C	-4.0 to +0.3	V
Power Supply Voltage 3	V _{SS3}	Ta = 25°C	-5.5 to +0.3	V
Power Supply Voltage 4	V _{SSL}	Ta = 25°C	-4.0 to +0.3	V
Input Voltage 1	V _{IN1}	V _{SS2} Input, Ta = 25°C	V _{SS2} - 0.3 to +0.3	V
Input Voltage 2	V _{IN2}	V _{SSL} Input, Ta = 25°C	V _{SSL} - 0.3 to +0.3	V
Output Voltage 1	V _{OUT1}	V _{SS2} Output, Ta = 25°C	V _{SS2} - 0.3 to +0.3	V
Output Voltage 2	V _{OUT2}	V _{SS3} Output, Ta = 25°C	V _{SS3} - 0.3 to +0.3	V
Output Voltage 3	V _{OUT3}	V _{SSL} Output, Ta = 25°C	V _{SSL} - 0.3 to +0.3	V
Storage Temperature	T _{STG}	—	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (3.0 V Spec.)

(V_{DD} = 0 V)

Parameter	Symbol	Condition	Range	Unit
Operating Temperature	T _{op}	—	-40 to +85	°C
Operating Voltage	V _{SS2}	Using LCD driver with "duty 1/2"	-3.5 to -2.2	V
		Except using LCD driver with "duty 1/2"	-3.5 to -2.0	
Crystal Oscillation Frequency	f _{XT}	—	30 to 66	kHz

ELECTRICAL CHARACTERISTICS (3.0 V Spec.)

DC Characteristics

(V_{DD} = 0 V, V_{SS2} = -3.0 V, T_a = -40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
V _{SS1} Voltage	V _{SS1}	C _a , C _b , C ₁₂ = 0.1 μF +100% -50%	-1.7	-1.5	-1.3	V	1
V _{SS3} Voltage	V _{SS3}	C _a , C _b , C ₁₂ = 0.1 μF +100% -50%	-4.7	-4.5	-4.3	V	
V _{SSL} Voltage	V _{SSL}	—	-1.9	-1.3	-0.6	V	
Crystal Oscillation Start Voltage	V _{STA}	Oscillation start time: within 5 seconds	—	—	-2.0	V	
Crystal Oscillation Hold Voltage	V _{HOLD}	—	—	—	-2.0	V	
Crystal Oscillation Stop Detection Time	T _{STOP}	—	0.1	—	1000	ms	
Internal Crystal Oscillator Capacitance	C _G	—	10	15	20	pF	
External Crystal Oscillator Capacitance	C _{GEX}	When external C _G used	10	—	30	pF	
Internal Crystal Oscillator Capacitance	C _D	—	10	15	20	pF	
POR Generation Voltage	V _{POR1}	When V _{SS2} is between V _{POR1} and -3.0 V	-0.7	—	0	V	
POR Non-generation Voltage	V _{POR2}	No POR when V _{SS2} is between V _{POR2} and -3.0 V	-3.0	—	-2.0	V	
Battery Check Reference Voltage	V _{RB}	T _a = 25°C	-0.73	-0.63	-0.53	V	2
V _{RB} Temperature Variation	ΔV _{RB}	—	—	-2.0	—	mV/°C	

Notes: 1. "POR" denotes Power On Reset.

2. "T_{STOP}" indicates that if the crystal oscillator stops over the value of T_{STOP}, the system reset occurs.

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit	
Supply Current 1	I_{DD1}	CPU in halt state	$T_a = -40\text{ to }+40^\circ\text{C}$	—	1.5	4.5	μA	1
			$T_a = +40\text{ to }+85^\circ\text{C}$	—	1.5	30	μA	
Supply Current 2	I_{DD2}	CPU in operating state	$T_a = -40\text{ to }+40^\circ\text{C}$	—	5.0	15	μA	
			$T_a = +40\text{ to }+85^\circ\text{C}$	—	5.0	40	μA	
Supply Current 3	I_{DD3}	CPU in halt state, RC oscillator for A/D converter is in operating state	$RT0 = 10\text{ k}\Omega$	—	300	450	μA	
			$RT0 = 2\text{ k}\Omega$	—	1300	2000	μA	
Supply Current 4	I_{DD4}	Battery check circuit in operating state, CPU in operating state	—	55	150	μA		

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Output Current 1 (P1.0)	I_{OH1}	$V_{OH1} = -0.5\text{ V}$	-6.0	-2.0	-0.7	mA	2
	I_{OL1}	$V_{OL1} = V_{SS2} + 0.5\text{ V}$	3.0	8.0	25	mA	
Output Current 2 (P1.1 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3)	I_{OH2}	$V_{OH2} = -0.5\text{ V}$	-6.0	-2.0	-0.7	mA	
	I_{OL2}	$V_{OL2} = V_{SS2} + 0.5\text{ V}$	0.7	2.0	6.0	mA	
Output Current 3 (BD)	I_{OH3}	$V_{OH3} = -0.7\text{ V}$	-6.0	-2.0	-0.7	mA	
	I_{OL3}	$V_{OL3} = V_{SS2} + 0.7\text{ V}$	0.7	2.0	6.0	mA	
Output Current 4 (RTO, RSO, CRT0, CS0)	I_{OH4}	$V_{OH4} = -0.1\text{ V}$	-2.5	-1.3	-0.7	mA	
	I_{OL4}	$V_{OL4} = V_{SS2} + 0.1\text{ V}$	0.7	1.3	2.5	mA	
Output Current 5 (When L16 to L23 are configured as output ports)	I_{OH5}	$V_{OH5} = -0.5\text{ V}$	-1.5	-0.6	-0.15	mA	
	I_{OL5}	$V_{OL5} = V_{SS2} + 0.5\text{ V}$	0.15	0.6	1.5	mA	
Output Current 6 (LO to L23)	I_{OH6}	$V_{OH6} = -0.2\text{ V}$ (V_{DD} level)	—	—	-4.0	μA	
	I_{OMH6}	$V_{OMH6} = V_{SS1} + 0.2\text{ V}$ (V_{SS1} level)	4.0	—	—	μA	
	I_{OMH6S}	$V_{OMH6S} = V_{SS1} - 0.2\text{ V}$ (V_{SS1} level)	—	—	-4.0	μA	
	I_{OML6}	$V_{OML6} = V_{SS2} + 0.2\text{ V}$ (V_{SS2} level)	4.0	—	—	μA	
	I_{OML6S}	$V_{OML6S} = V_{SS2} - 0.2\text{ V}$ (V_{SS2} level)	—	—	-4.0	μA	
	I_{OL6}	$V_{OL6} = V_{SS3} + 0.2\text{ V}$ (V_{SS3} level)	4.0	—	—	μA	
Output Leakage Current (P1.0 to P1.3) (P2.0 to P2.3) (P3.0 to P3.3) (RTO, RSO, CRT0, CS0)	I_{OOH}	$V_{OH} = V_{DD}$	—	—	0.3	μA	
	I_{OOL}	$V_{OL} = V_{SS2}$	-0.3	—	—	μA	

DC Characteristics (continued)

($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

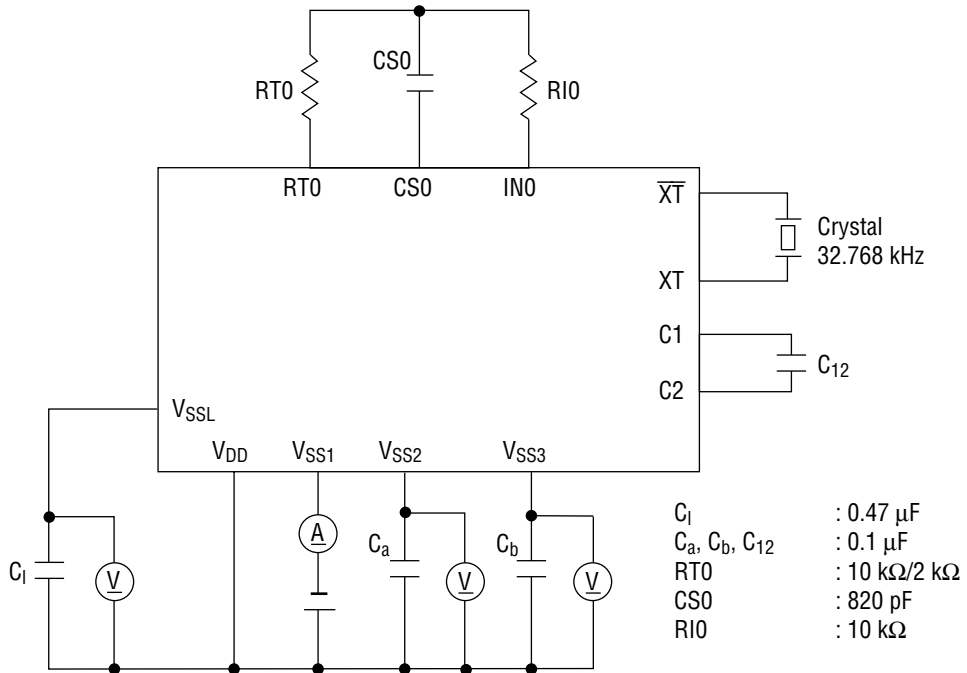
Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Input Current 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	I_{IH1}	$V_{IH1} = V_{DD}$ (when pulled down)	30	90	300	μA	3
	I_{IL1}	$V_{IL1} = V_{SS2}$ (when pulled up)	-300	-90	-30	μA	
	I_{IH1Z}	$V_{IH1} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL1Z}	$V_{IL1} = V_{SS2}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 2 (IN0)	I_{IH2}	$V_{IH2} = V_{DD}$ (when pulled down)	30	90	300	μA	3
	I_{IH2Z}	$V_{IH2} = V_{DD}$ (in a high impedance state)	0	—	1.0	μA	
	I_{IL2Z}	$V_{IL2} = V_{SS2}$ (in a high impedance state)	-1.0	—	0	μA	
Input Current 3 (RESET, TST1, TST2)	I_{IH3}	$V_{IH3} = V_{DD}$	0	—	1.0	μA	3
	I_{IL3}	$V_{IL3} = V_{SS2}$	-3.0	-1.5	-0.75	mA	
Input Voltage 1 (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	V_{IH1}	—	-0.6	—	0	V	4
	V_{IL1}	—	-3.0	—	-2.4	V	
Input Voltage 2 (IN0)	V_{IH2}	—	-0.6	—	0	V	
	V_{IL2}	—	-3.0	—	-2.4	V	
Input Voltage 3 (RESET, TST1, TST2)	V_{IH3}	—	-0.6	—	0	V	
	V_{IL3}	—	-3.0	—	-2.4	V	

DC Characteristics (continued)

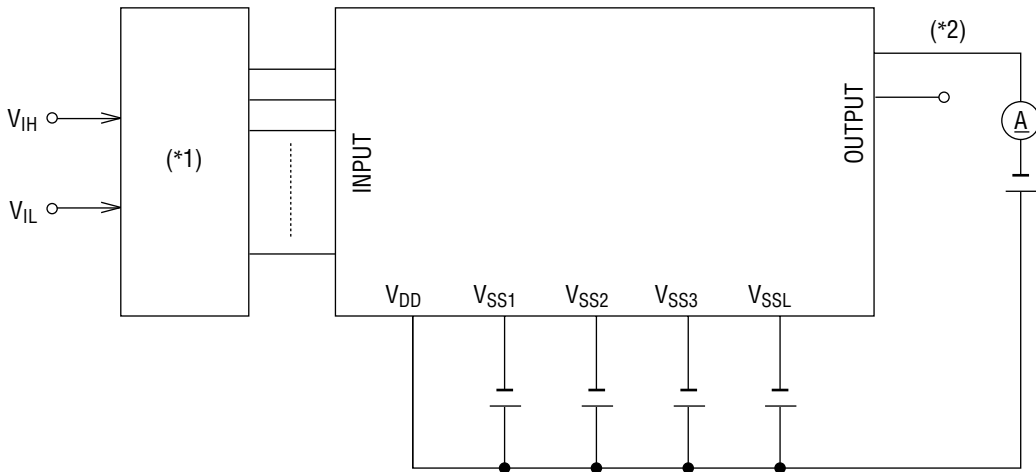
($V_{DD} = 0\text{ V}$, $V_{SS1} = V_{SSL} = -1.5\text{ V}$, $V_{SS2} = -3.0\text{ V}$, $V_{SS3} = -4.5\text{ V}$,
 $T_a = -40\text{ to }+85^\circ\text{C}$ unless otherwise specified)

Parameter (Pin Name)	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Hysteresis Width (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	ΔV_{T1}	—	0.2	0.5	1.0	V	4
Hysteresis Width (RESET, TST1, TST2)	ΔV_{T2}	—	0.2	0.5	1.0	V	
Input Pin Capacitance (P0.0 to P0.3) (P2.0 to P2.3) (P3.0 to P3.3)	C_{IN}	—	—	—	5.0	pF	1

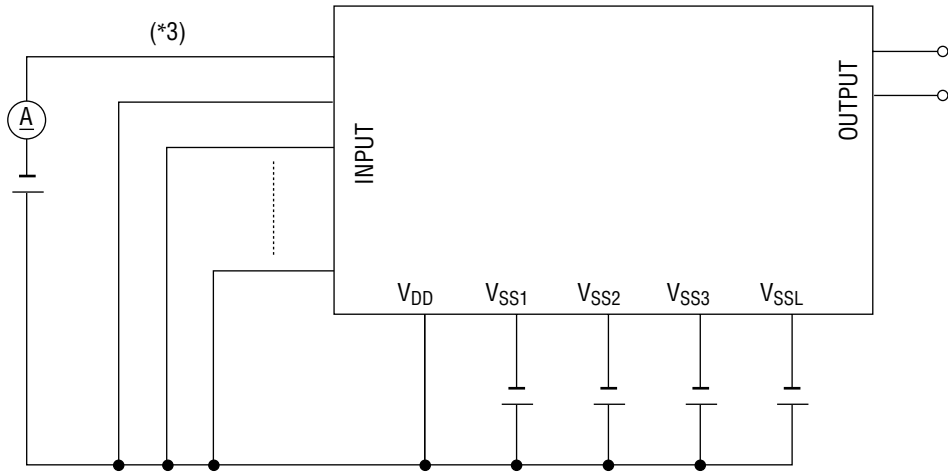
Measuring circuit 1



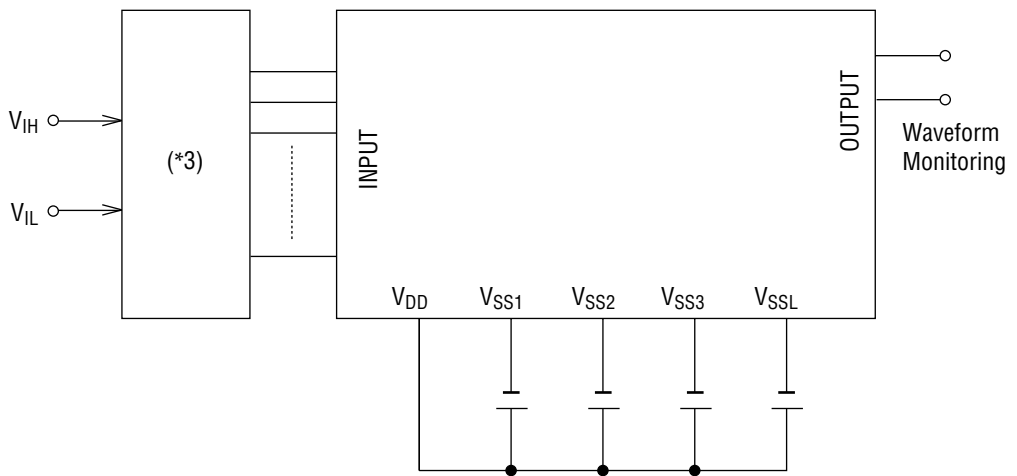
Measuring circuit 2



Measuring circuit 3



Measuring circuit 4



- *1 Input logic circuit to determine the specified measuring conditions.
- *2 Measured at the specified output pins.
- *3 Measured at the specified input pins.

A/D Converter Characteristics

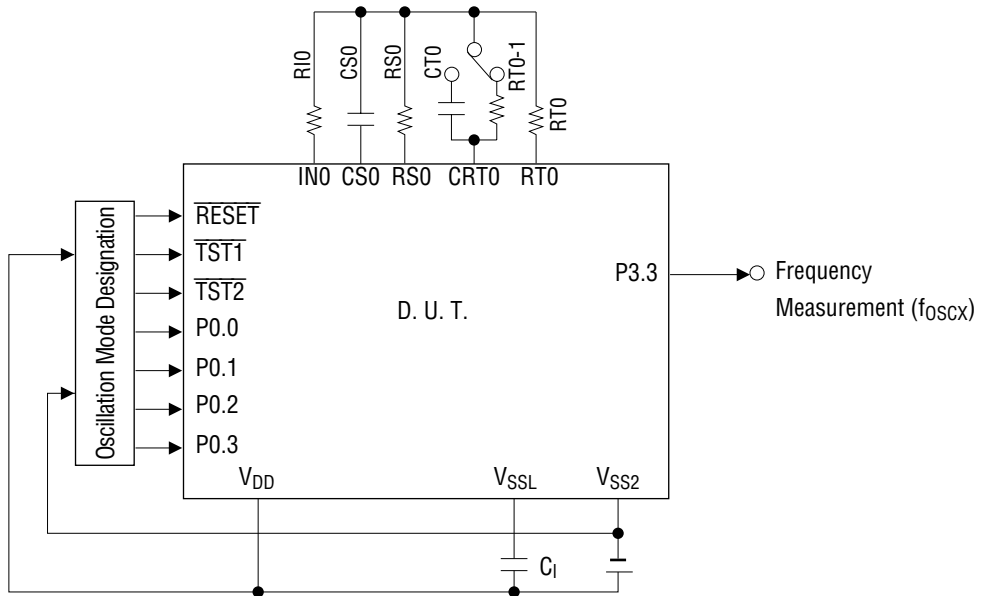
(V_{DD} = 0 V, V_{SS2} = -3.0 V, T_a = -40 to +85°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring Circuit
Resistor for Oscillation	RS0, RT0, RT0-1	CS0, CT0 ≥ 740 pF	1.0	—	—	kΩ	5
Input Current Limiting Resistor	RI0	—	1.0	10	—	kΩ	
Oscillation Frequency	f _{OSC1}	Resistor for oscillation = 2 kΩ	200	239	277	kHz	
	f _{OSC2}	Resistor for oscillation = 10 kΩ	46.5	55.4	64.3	kHz	
	f _{OSC3}	Resistor for oscillation = 200 kΩ	2.79	3.32	3.85	kHz	
RS•RT Oscillation Frequency Ratio(*)	Kf1	RT0, RT0-1 = 2 kΩ	4.115	4.22	4.326	—	
	Kf2	RT0, RT0-1 = 10 kΩ	0.990	1.0	1.010	—	
	Kf3	RT0, RT0-1 = 200 kΩ	0.0573	0.0616	0.0659	—	

* Kfx is the ratio of the oscillation frequency by a sensor resistor to the oscillation frequency by a reference resistor in the same condition.

$$Kfx = \frac{f_{oscx} \text{ (RT0-CS0 Oscillation)}}{f_{oscx} \text{ (RS0-CS0 Oscillation)}} , \frac{f_{oscx} \text{ (RT0-1-CS0 Oscillation)}}{f_{oscx} \text{ (RS0-CS0 Oscillation)}} \\ (x = 1, 2, 3)$$

Measuring circuit 5



RT0, RT0-1 = 2 kΩ/10 kΩ/200 kΩ
 RSO = 10 kΩ
 R10 = 10 kΩ
 CS0, CTO = 820 pF
 C1 = 0.47 μF

FUNCTIONAL DESCRIPTION

• A/D converter (ADC)

The MSM64162D has a built-in 1-channel RC oscillation type A/D converter. The A/D converter is composed of a 1-channel oscillation circuit, Counter A (CNTA0-4, a 4.8-digit decade counter), Counter B (CNTB0-3, a 14-bit binary counter), and A/D Converter Control Registers 0 and 1 (ADCON0, ADCON1).

By counting oscillation frequencies that vary depending on a resistor or capacitor connected to the RC oscillation circuit, the A/D converter converts resistance values or capacitance values to corresponding digital values. By using a thermistor or humidity sensor as a resistance, a thermometer or a hygrometer can be constructed.

• LCD driver (LCD)

The MSM64162D has a built-in LCD driver for 24 outputs.

The LCD driver consists of 21×4 -bit display registers (DSPR0-20), the Display Control Register (DSPCON), a 24-output LCD driver circuit, and a bias generation circuit (BIAS).

There are three types of driving methods: 1/4 duty, 1/3 duty and 1/2 duty. Software selects the duty mode.

A mask option can select either a common driver or a segment driver for each LCD driver pin. A mask option can also specify assignment of each bit of the display register to each segment. All the display registers must be selected by a mask option.

L16 to L23 of the LCD driver can be configured to be output ports by a mask option.

The relationship between the duty, the bias method, and the maximum segment number follows:

1/4 duty 1/3 bias method	-----	80 segments
1/3 duty 1/3 bias method	-----	63 segments
1/2 duty 1/2 bias method	-----	44 segments

• Buzzer driver (BD)

The MSM64162D has a built-in buzzer driver with 2 buzzer output frequencies and 4 buzzer output modes. Each buzzer output is selected by the Buzzer Control Register (BDCON) and the Buzzer Frequency Control Register (BFCON).

• Capture circuit (CAPR)

The MSM64162D captures 32 Hz to 256 Hz output of the time base counter at the falling of Port 0.0 or 0.1 (P0.0 or P0.1) to "L" level when the pull-up resistor input is chosen, or at the rising to "H" level when the pull-down resistor input is chosen. The capture circuit is composed of the Capture Control Register (CAPCON) and the Capture Registers (CAPR0, CAPR1) that fetch output from the time base counter.

• Watchdog timer (WDT)

The MSM64162D has a built-in watchdog timer to detect CPU malfunction. The watchdog timer is composed of a 6-bit watchdog timer counter (WDTC) to count a 16 Hz output and a watchdog timer control register (WDTCON) to reset WDTC.

• Clock generation circuit (CLKG)

The clock generation circuit (CLKG) in the MSM64162D contains a 32.768 kHz crystal oscillation circuit. This circuit generates the system clock (CLK) and the time base clock (32.768 kHz).

The system clock drives the CPU while the time base clock drives the time base counter and the buzzer driver.

The system clock frequency is 32.768 kHz, which is the output of the crystal oscillation circuit.

• Time base counter (TBC)

The MSM64162D has a built-in time base counter (TBC) that generates clocks to be supplied to internal peripheral circuits. The time base counter is composed of 15 binary counters. The count clock of the time base is driven by the oscillation clock (32.768 kHz) of the crystal oscillation circuit. The output of the time base counter is used for the buzzer driver, the system reset circuit, the watchdog timer, the time base interrupt, the sampling clocks of each port, and the capture circuit.

• I/O port

Input-output ports (P2, P3) (8 bits)	: Pull-up (pull-down) resistor input or high-impedance input, CMOS output or NMOS open drain output: these can be specified for each bit; external 0 interrupt
Input port (P0) (4 bits)	: Pull-up (pull-down) resistor input or high-impedance input; external 1 interrupt
Output port (P1) (4 bits)	: CMOS output or NMOS open drain output

• Interrupt (INTC)

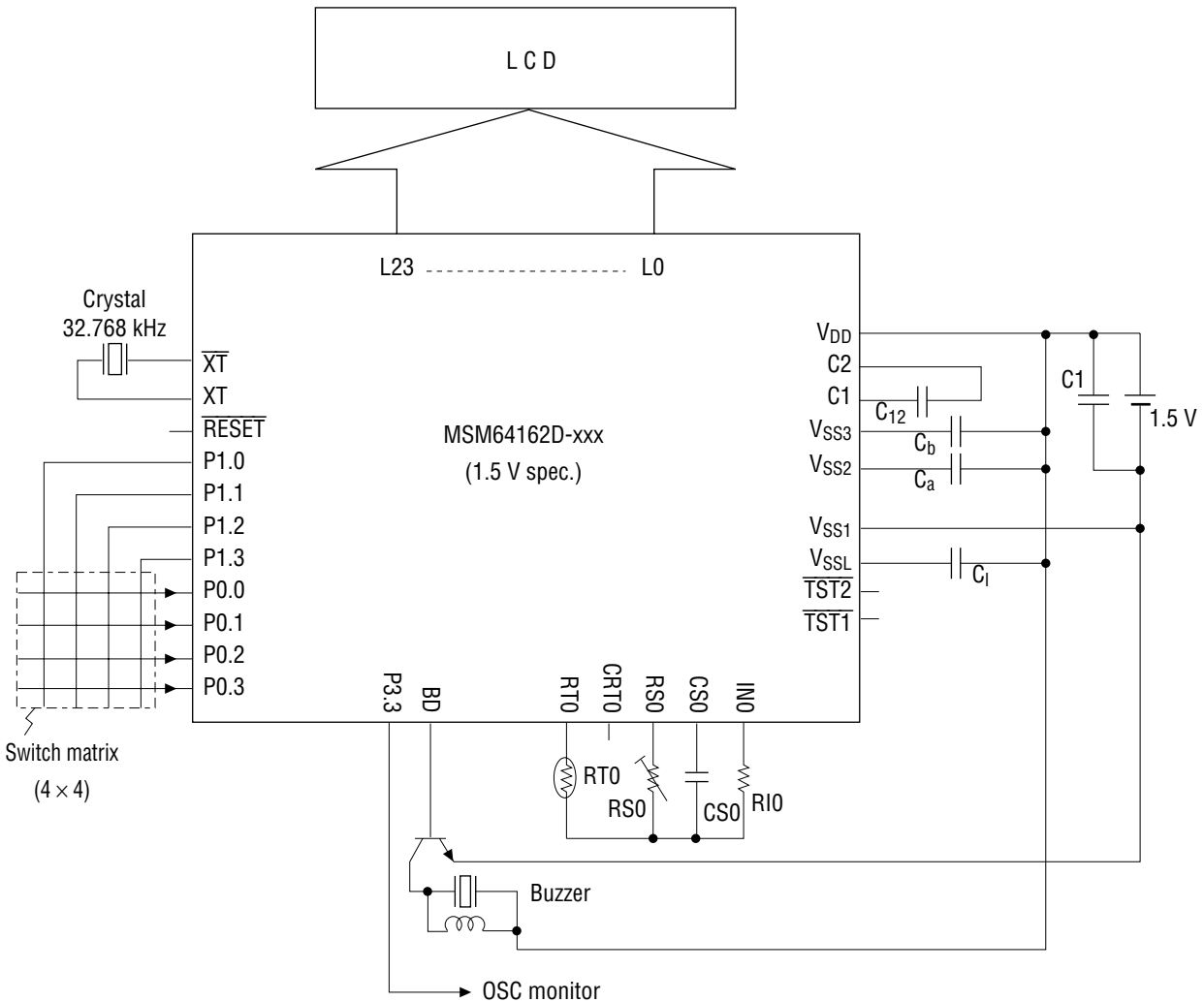
The MSM64162D has 9 interrupt sources (9 vector addresses), of which two are external interrupts from ports and seven are internal interrupts.

Of the nine interrupt sources, only the watchdog interrupt cannot be disabled (non-maskable interrupt). The other eight interrupts are controlled by the master interrupt enable flag (MI) and the interrupt enable registers (IE0, IE1 and IE2). When an interrupt condition is met, the CPU branches to a vector address corresponding to the interrupt source.

• Battery check circuit (BC)

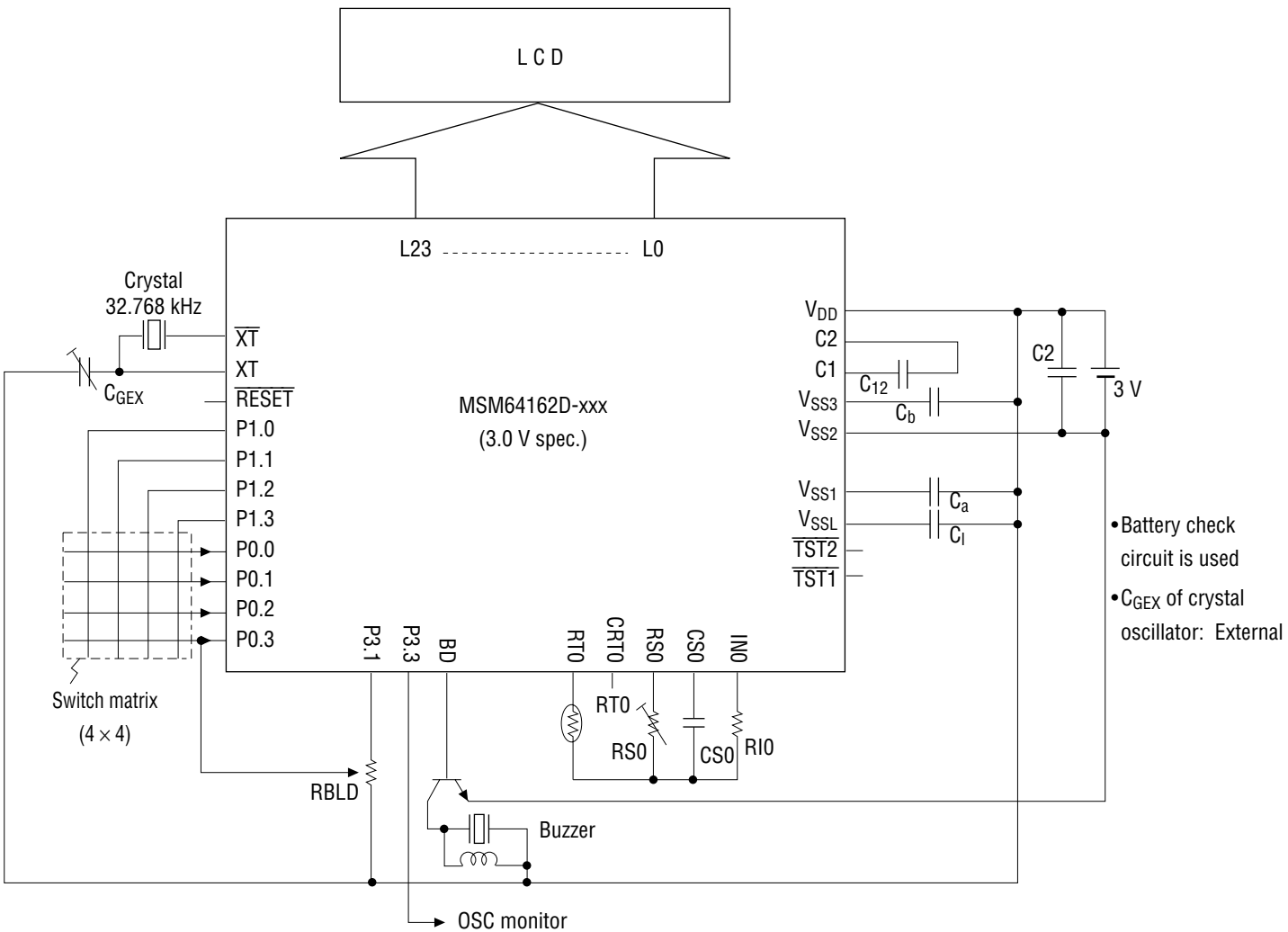
The battery check circuit (BC) detects the level of the supply voltage by comparing the voltage generated by an external supply-voltage dividing resistor (RBLD) with the internal reference voltage (Vrb).

APPLICATION CIRCUITS



1.5 V Spec. Application Circuit

APPLICATION CIRCUITS (continued)

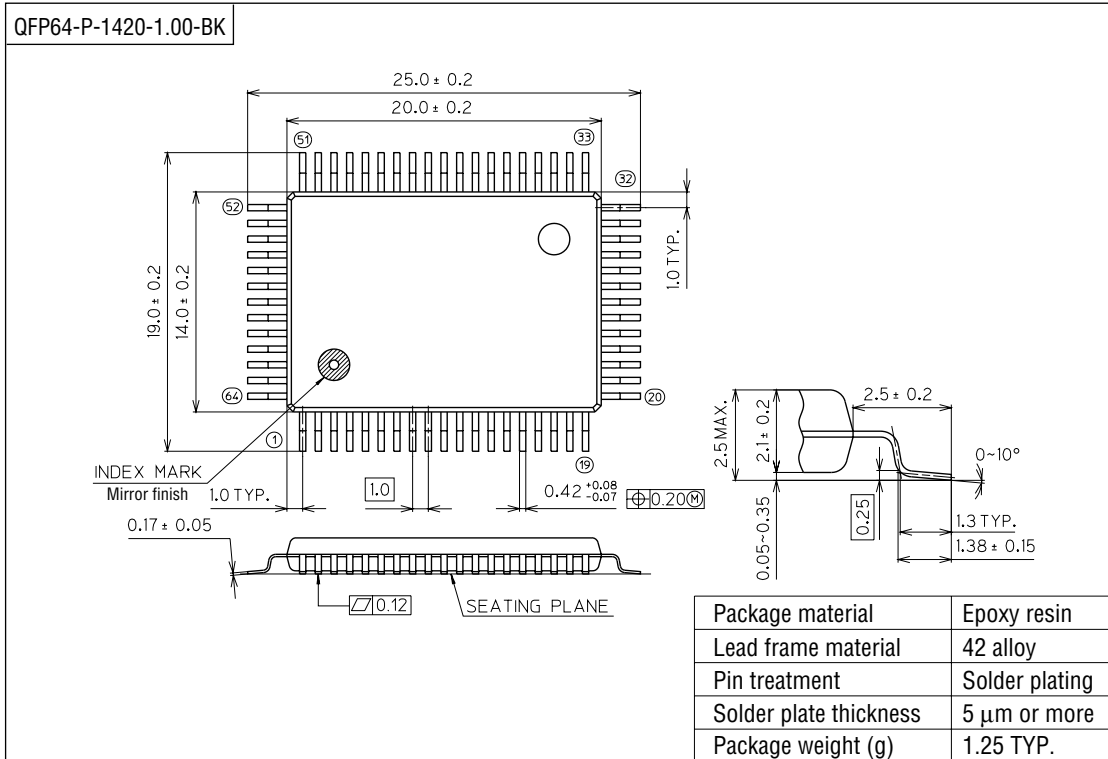


- Battery check circuit is used
- CGEX of crystal oscillator: External

3.0 V Spec. Application Circuit

PACKAGE DIMENSIONS

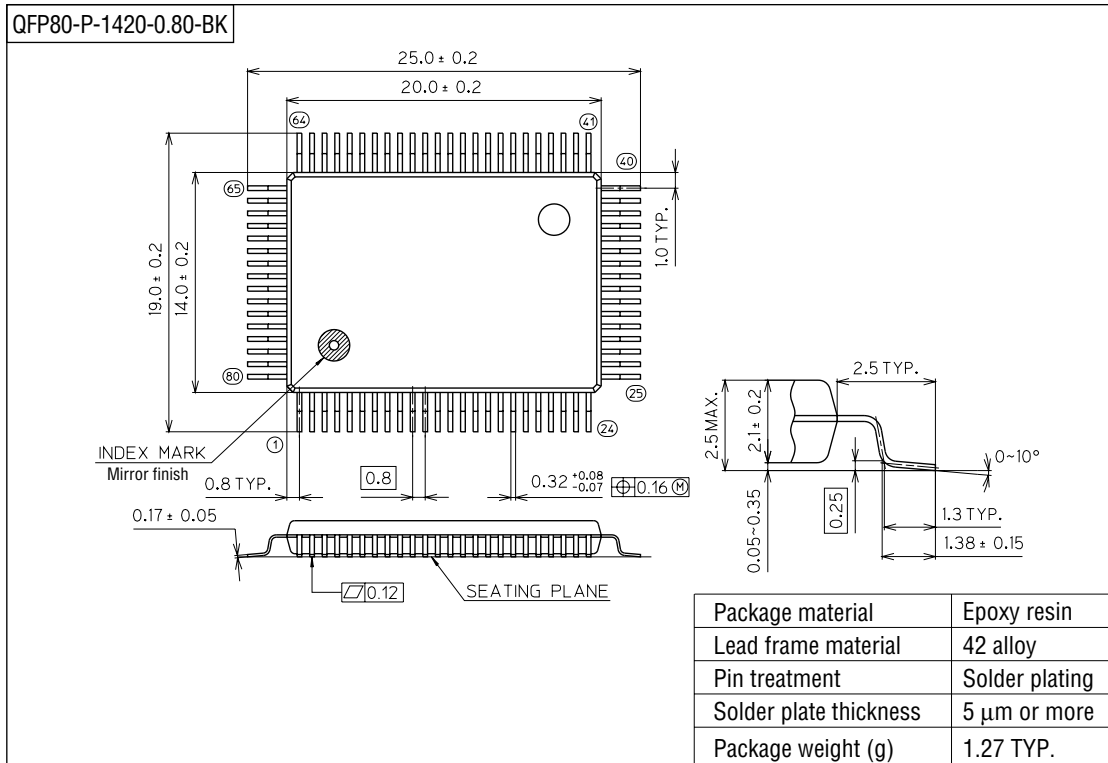
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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