

OKI Semiconductor

MSM6791

DRAM Interface IC

GENERAL DESCRIPTION

The MSM6791 can be used as a memory for voice data by connecting OKI solid-state recording and playback ICs (MSM6688 and MSM6788).

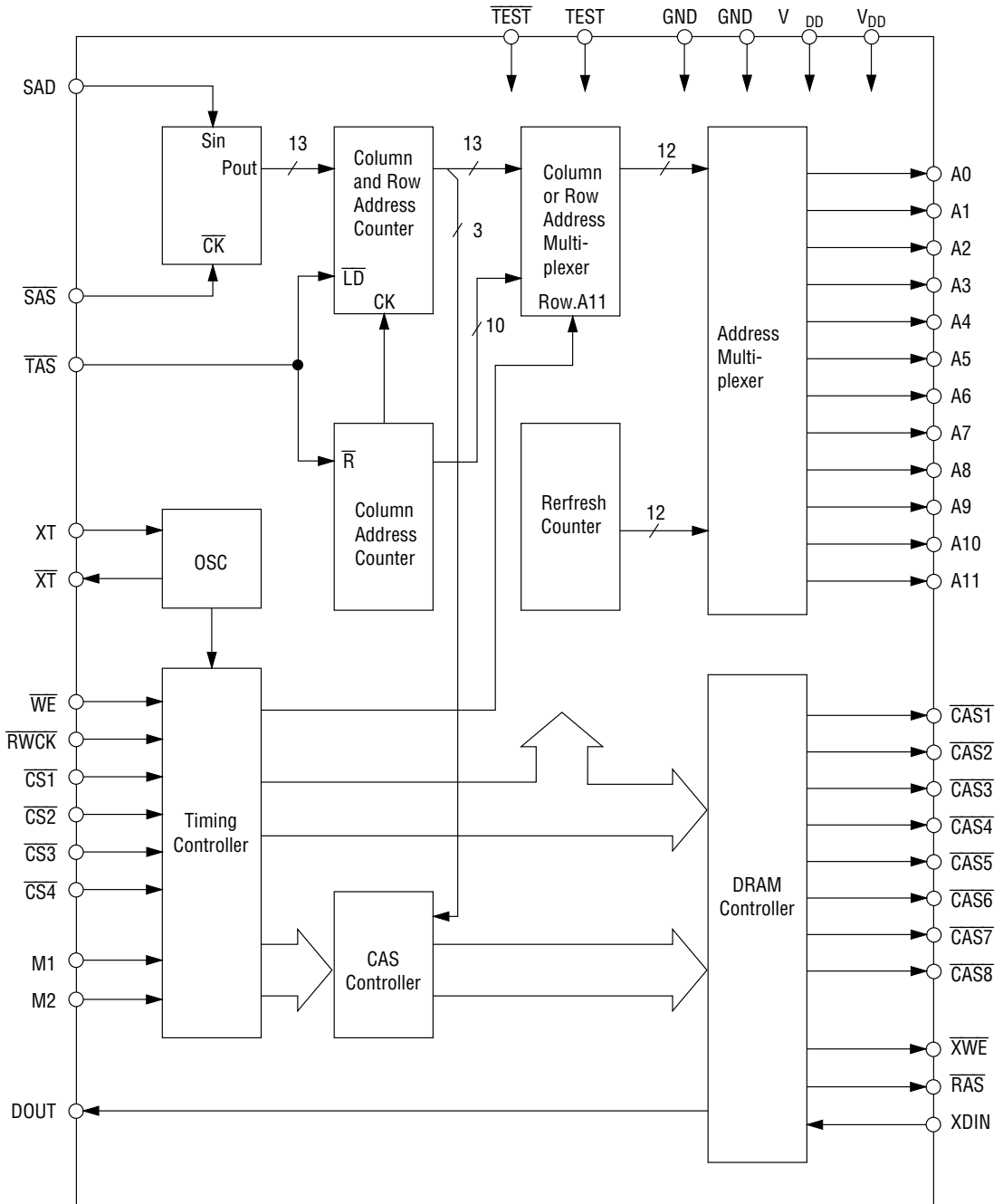
FEATURES

- DRAM (× 1-bit configuration)
 - 1M-bit DRAM (MSM511000A, MSM511001A) : 8 pcs. can be connected.
 - 4M-bit DRAM (MSM514100A, MSM514101A) : 8 pcs. can be connected.
 - 16M-bit DRAM (MSM5116100A) : 2 pcs. can be connected.

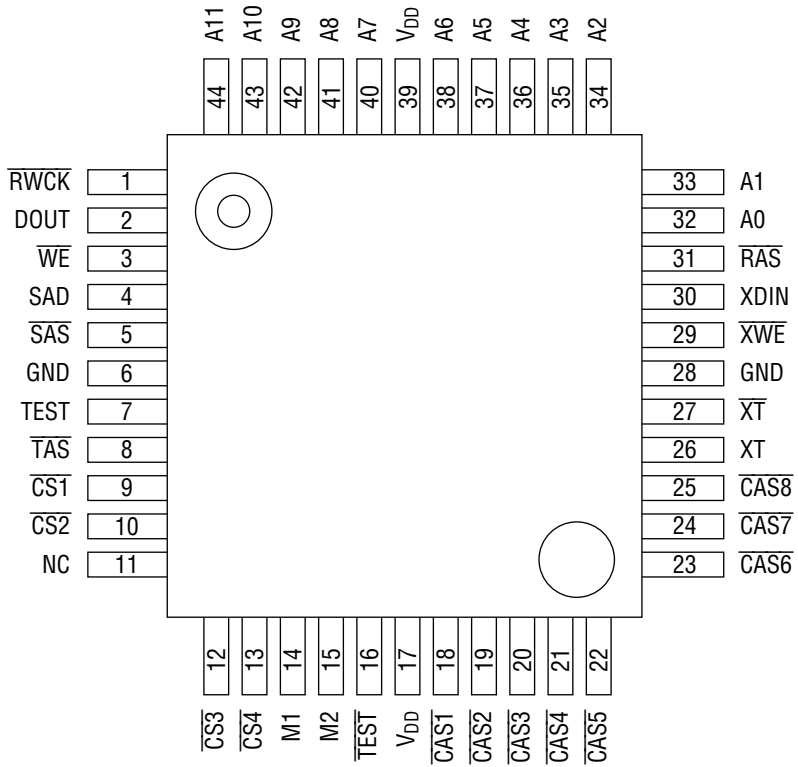
Note: MSM511002A/MSM514102A that corresponds to a static column mode cannot be used.

- Power supply voltage : 5V single rail
- Built-in refresh circuit (RAS only refresh)
- Original oscillation frequency: 8MHz
- Bit rates: 10kbps, 12.5kbps, 16kbps in MSM6788 connection (8kHz sampling fixation)
7.5kbps, 9.4kbps, 12kbps in MSM6788 connection (6kHz sampling fixation)
16kbps~32kbps in MSM6688 connection (4kHz~8kHz sampling)
- Package: 44-pin plastic QFP (QFP44-P-910-2K) (Product name : MSM6791GS-2K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



44-Pin Plastic QFP

NC: No-connection pin

PIN DESCRIPTION

Symbol	Type	Description																				
V _{DD}	-	Power supply																				
GND	-	Ground																				
XT	I	Oscillator																				
\overline{XT}	O	Oscillator																				
TEST	I	IC test. Use this pin by setting to 'L' level.																				
\overline{TEST}	I	IC test. Use this pin by setting to 'H' level.																				
SAD	I	Read/write head address																				
\overline{SAS}	I	Clock to take the serial address data in the internal register																				
\overline{TAS}	I	Serial address data taken in the address register to the internal address counter																				
\overline{RWCK}	I	Clock to read and write the information of the data register. The internal operation starts by the fall edge of \overline{RWCK} . In a read mode, the data taken in XDIN is latched and it is output to the DOUT pin. In a write mode, the DI/O output data of MSM6688/6788/6789 is taken in the DIN pin of the DRAM. In addition, the internal address counter automatically increments by the fall edge of \overline{RWCK} and the address data output from A0 to A11.																				
\overline{WE}	I	Select a read mode and write mode.																				
\overline{XWE}	O	DRAM control																				
A0~A11	O	DRAM address																				
\overline{RAS}	O	DRAM control																				
$\overline{CAS1}$ ↕ $\overline{CAS8}$	O	DRAM control																				
XDIN	I	Data input																				
DOUT	O	Data output																				
$\overline{CS1}$ $\overline{CS2}$ $\overline{CS3}$ $\overline{CS4}$	I	Chip select data in connecting DRAM By inputting a "L" level signal to each pin, up to 32M-bit of memory (8M-bit of memory for each pin) can be controlled for four Pins. These pins become the input pins to select the highest address in 16M-bit DRAM connection.																				
M1 M2	I	Set the connecting pattern of DRAM. <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Connecting Mode</th> <th>M2</th> <th>M1</th> <th>DRAM Connecting Pattern</th> </tr> </thead> <tbody> <tr> <td>Mode 0</td> <td>L</td> <td>L</td> <td>1M-bit DRAM × 1~8pcs. connectable</td> </tr> <tr> <td>Mode 1</td> <td>L</td> <td>H</td> <td>4M-bit DRAM × 1~8pcs. connectable</td> </tr> <tr> <td>Mode 2</td> <td>H</td> <td>L</td> <td>(4M-bit DRAM × 1pcs.) + (1M-bit DRAM × 0~3pcs.) connectable</td> </tr> <tr> <td>Mode 3</td> <td>H</td> <td>H</td> <td>16M-bit DRAM × 1~2pcs. connectable</td> </tr> </tbody> </table>	Connecting Mode	M2	M1	DRAM Connecting Pattern	Mode 0	L	L	1M-bit DRAM × 1~8pcs. connectable	Mode 1	L	H	4M-bit DRAM × 1~8pcs. connectable	Mode 2	H	L	(4M-bit DRAM × 1pcs.) + (1M-bit DRAM × 0~3pcs.) connectable	Mode 3	H	H	16M-bit DRAM × 1~2pcs. connectable
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Mode 3	H	H	16M-bit DRAM × 1~2pcs. connectable																			

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	$T_a = 25^\circ\text{C}$	-0.5 to +7	V
Input Voltage	V_I		-0.5 to $V_{DD}+0.5$	V
Output Voltage	V_O		-0.5 to $V_{DD}+0.5$	V
Input Current	I_I	GND = 0V	-10 to +10	mA
Output Current	I_O		-20 to +20	mA
Storage Temperature	T_{STG}	—	-65 to +150	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

GND = 0V

Parameter	Symbol	Range	Unit
Supply Voltage	V_{DD}	4.5 to 5.5	V
Operating Temperature	T_{OP}	-40 to +85	$^\circ\text{C}$
Oscillation Frequency	f_{OSC}	8	MHz

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = -40 to +85 $^\circ\text{C}$, $V_{DD} = 5V \pm 10\%$ GND = 0V)

Parameter	Symbol	Condition	Min.	Typ. *1	Max.	Unit
"H" Level Input Voltage	V_{IH}	—	3.5	—	$V_{DD}+0.3$	V
"L" Level Input Voltage	V_{IL}	—	-0.3	—	1.5	V
"H" Level Input Current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	10	μA
"L" Level Input Current	I_{IL}	$V_{IL} = \text{GND}$	-10	-0.01	—	μA
3-state Output Leak Current (includes open-drain output)	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	10	μA
	I_{OZL}	$V_{OL} = \text{GND}$	-10	-0.01	—	μA
"H" Level Output Voltage	V_{OH}	$I_{OH} = -5.0 \text{ mA}$	2.4	4.20	V_{DD}	V
"L" Level Output Voltage	V_{OL}	$I_{OL} = 5.0 \text{ mA}$	V_{SS}	0.24	0.5	V
Operational Current Consumption	I_{DD}	Output open $f_{OSC} = 8\text{MHz}$ $V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$	—	—	3	mA

*1 TYP means $V_{DD}=5.0\text{V}$, $T_a=25^\circ\text{C}$

APPLICATION CIRCUITS

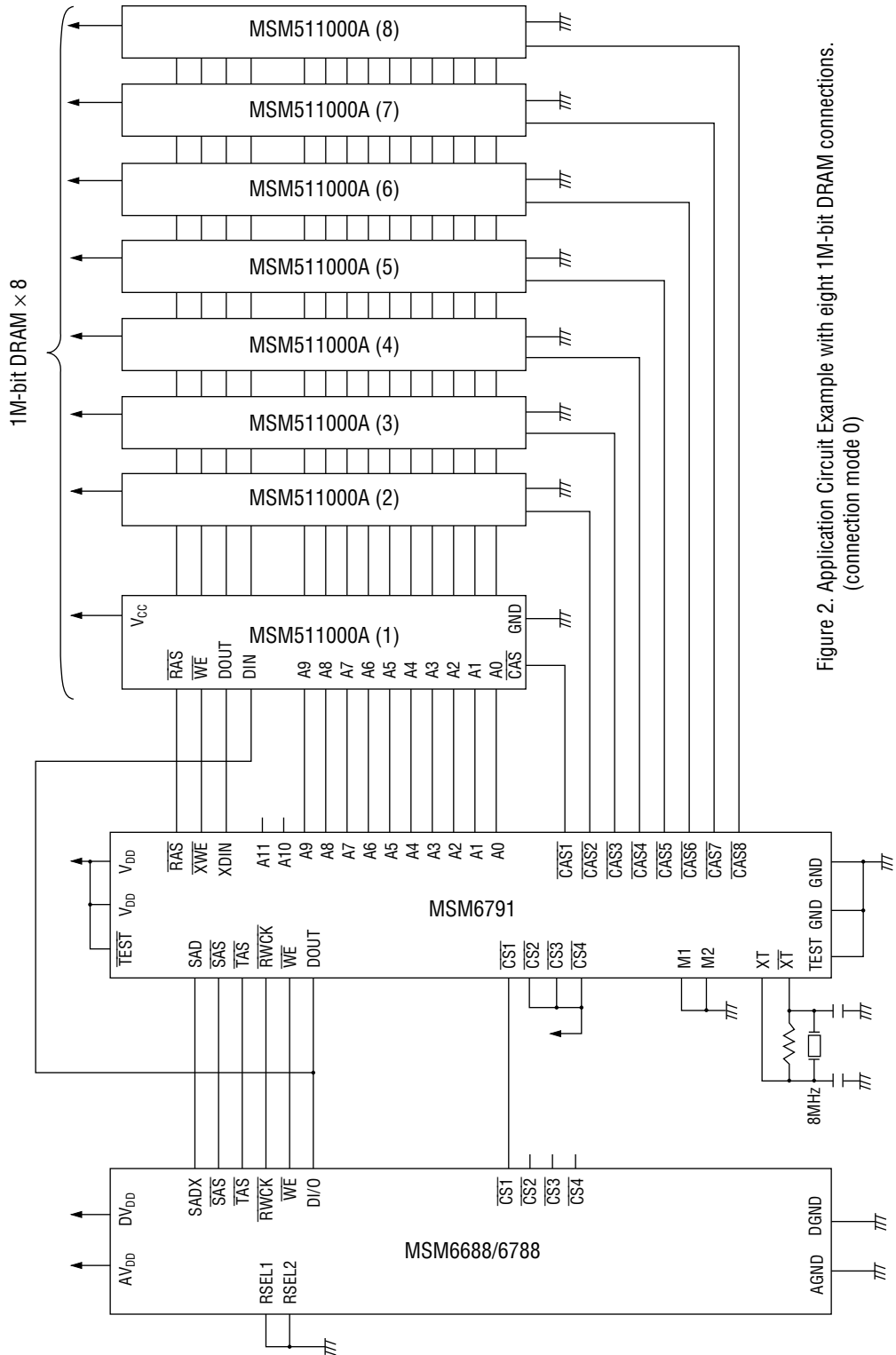


Figure 2. Application Circuit Example with eight 1M-bit DRAM connections.
(connection mode 0)

APPLICATION CIRCUITS (Continued)

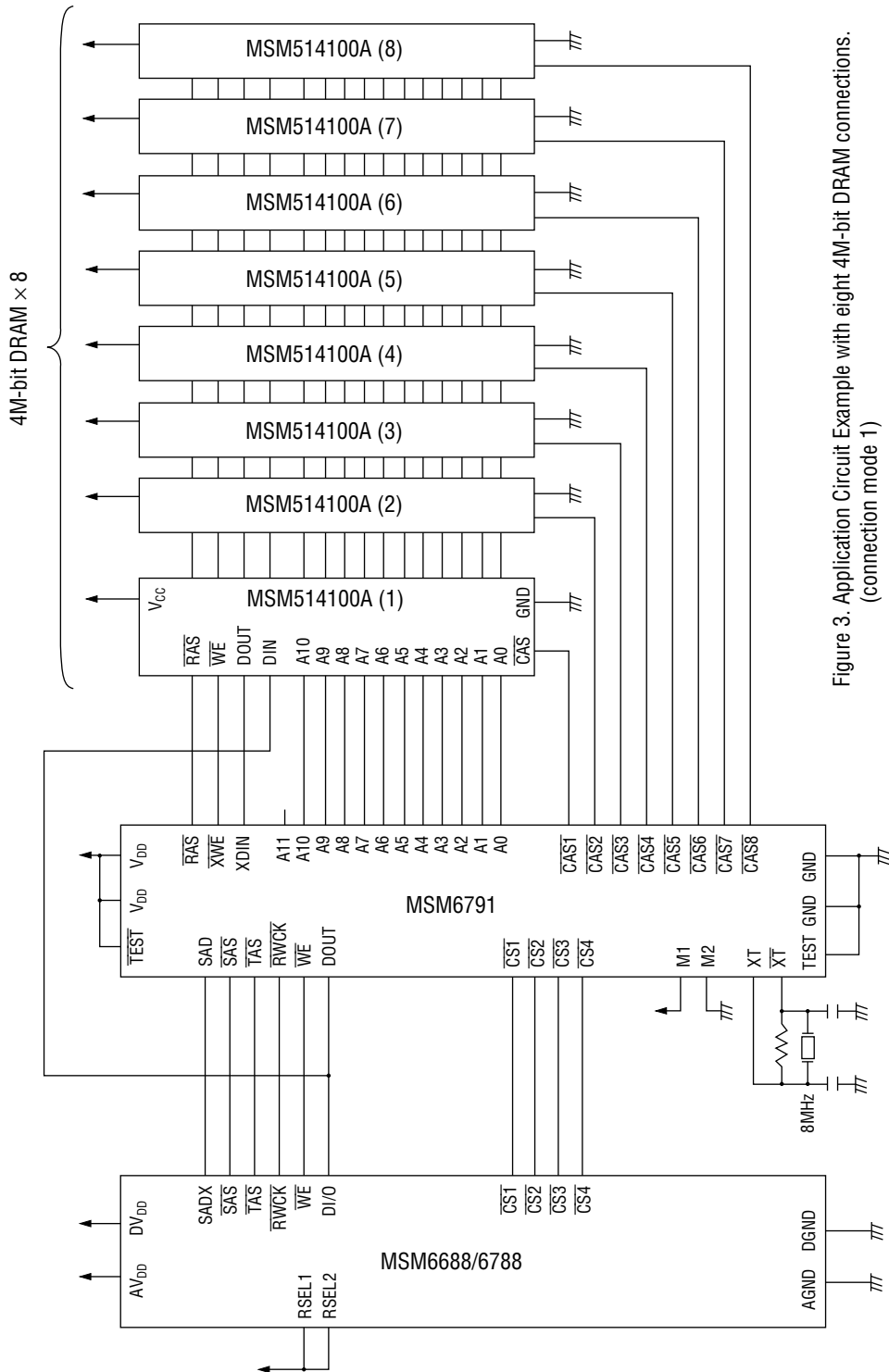


Figure 3. Application Circuit Example with eight 4M-bit DRAM connections. (connection mode 1)

APPLICATION CIRCUITS (Continued)

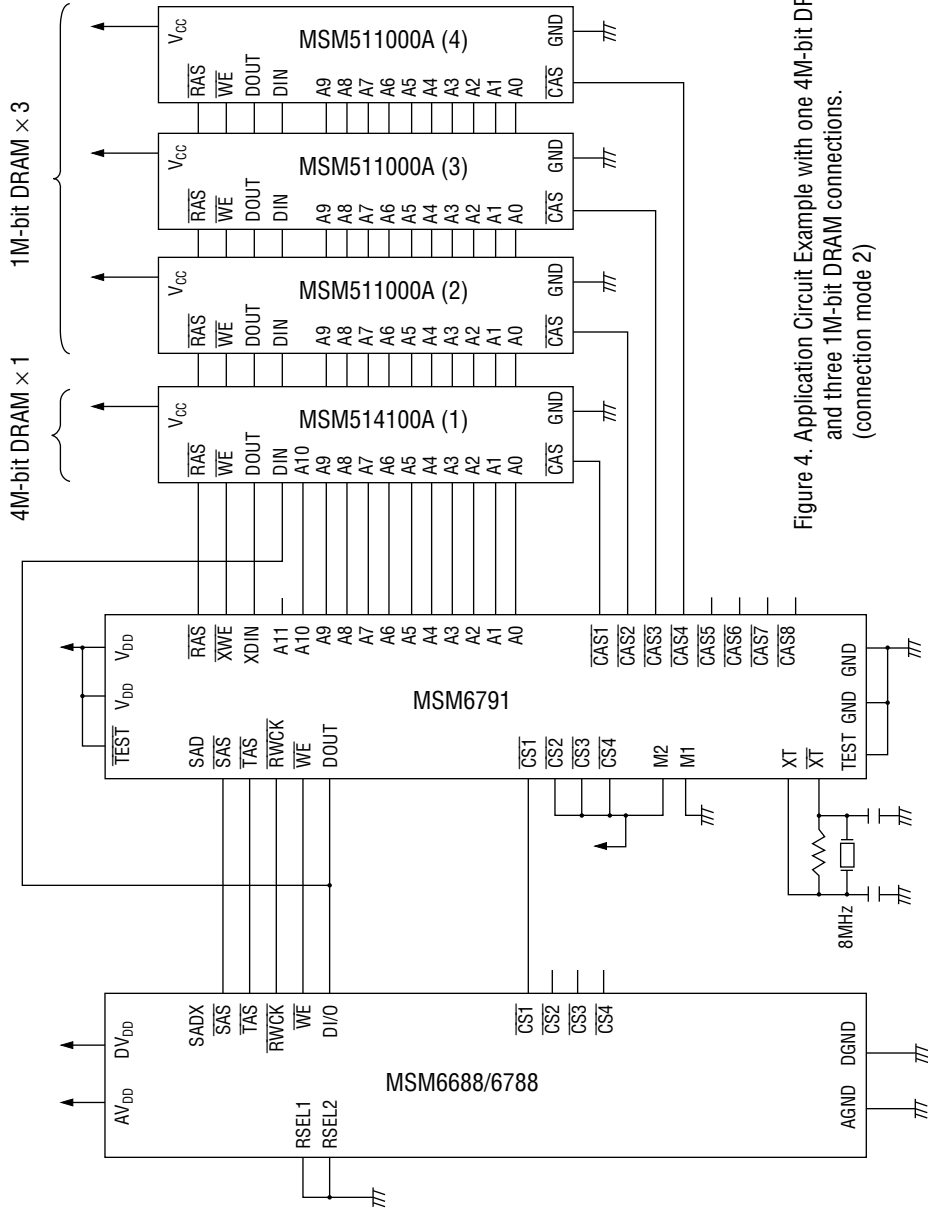


Figure 4. Application Circuit Example with one 4M-bit DRAM and three 1M-bit DRAM connections. (connection mode 2)

APPLICATION CIRCUITS (Continued)

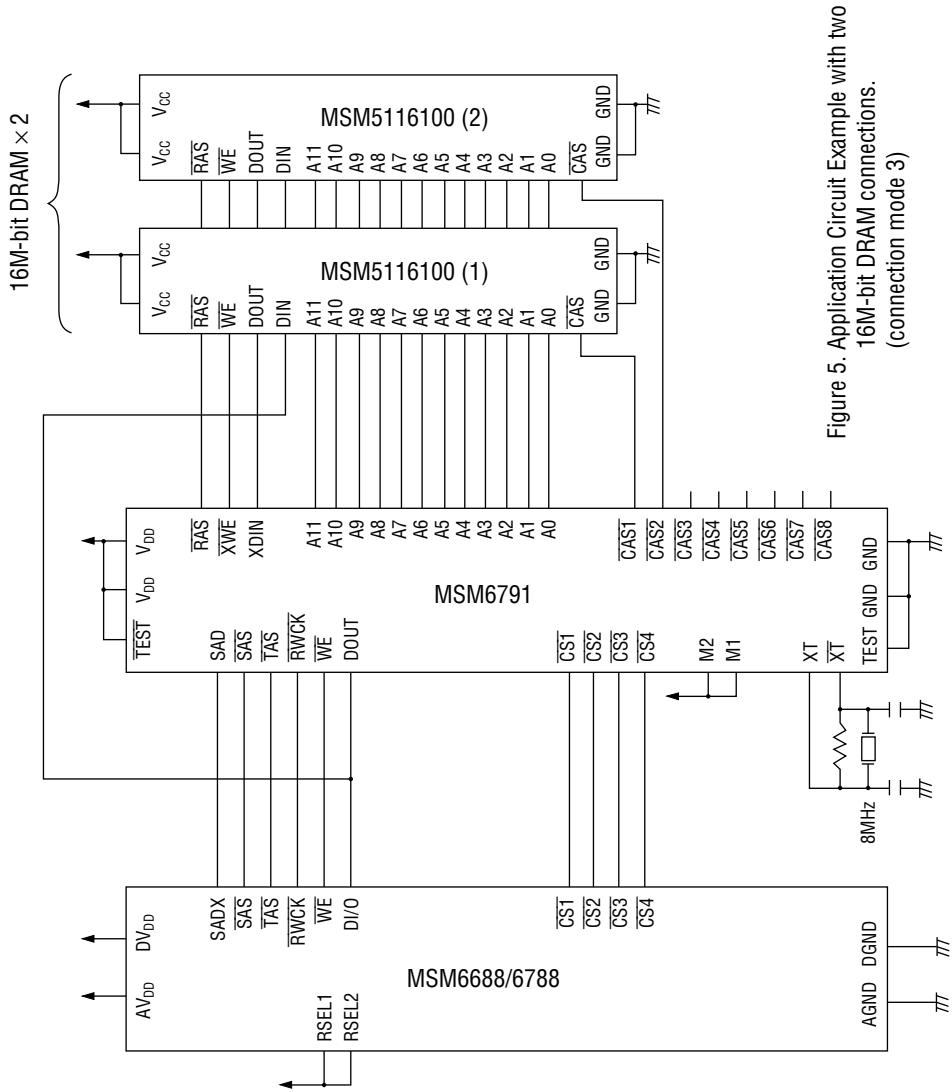


Figure 5. Application Circuit Example with two 16M-bit DRAM connections. (connection mode 3)

APPLICATION CIRCUITS (Continued)

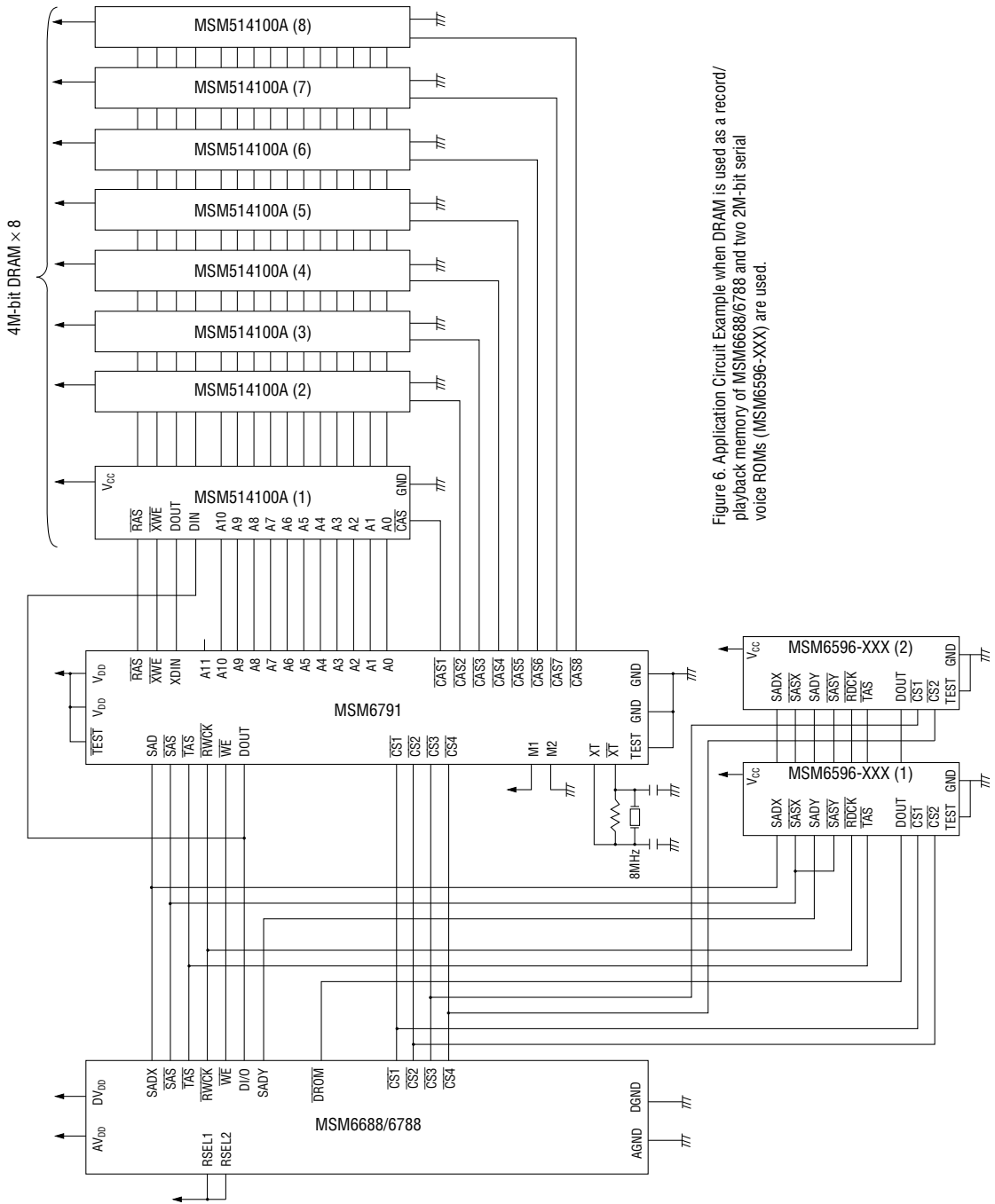


Figure 6. Application Circuit Example when DRAM is used as a record/playback memory of MSM6688/6788 and two 2M-bit serial voice ROMs (MSM6596-XXX) are used.