OKI Semiconductor

This version: Nov. 1999
Previous version: Aug. 1998

MSM7540/7560

Single Rail ADPCM CODEC

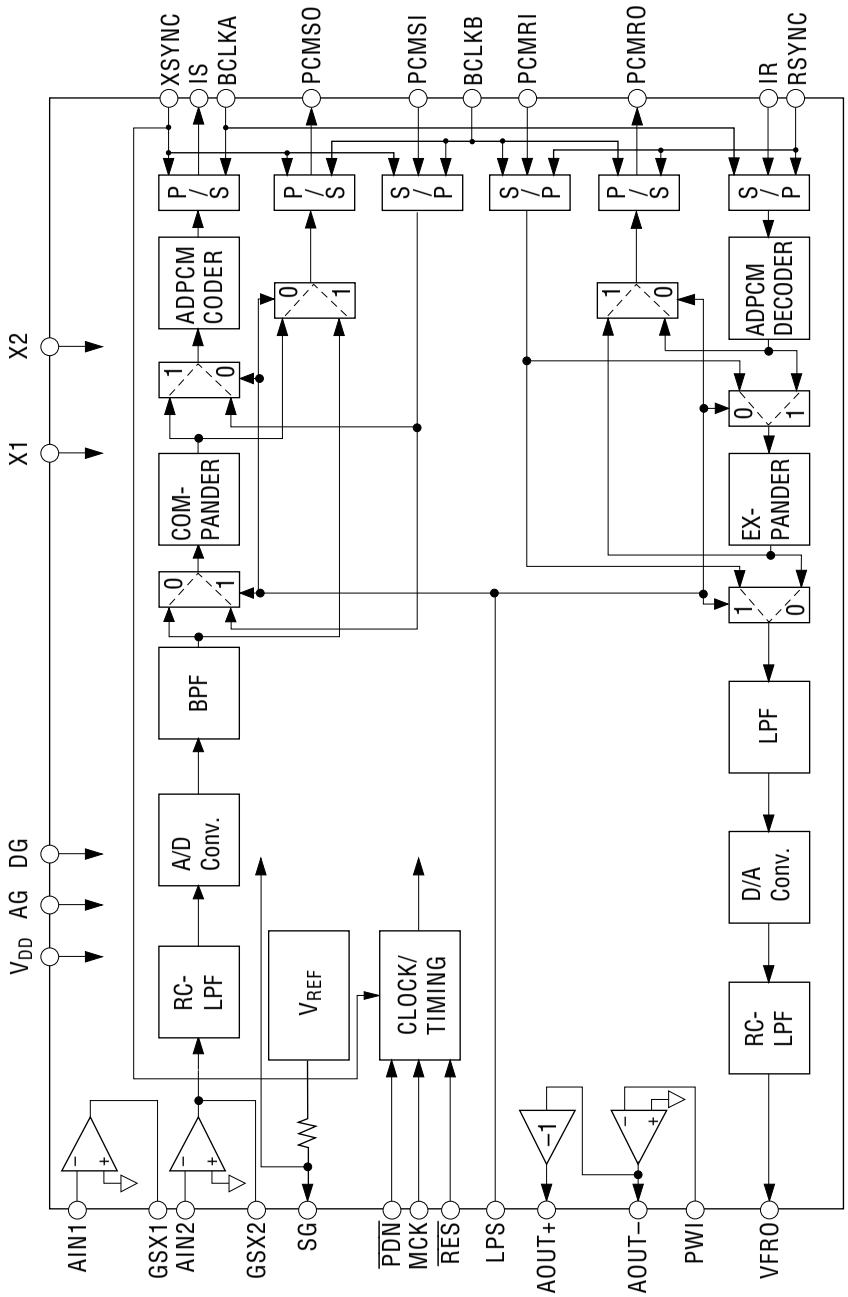
GENERAL DESCRIPTION

The MSM7540/7560 are single channel ADPCM CODEC ICs which perform mutual transcoding between an analog voice band signal 300 to 3400 Hz and 32 kbps ADPCM serial data.
Using advanced circuit technology, these devices operate using a single 5 V power supply and have low power consumption.
The MSM7540/7560 are optimized for advanced digital cordless telephone system applications.

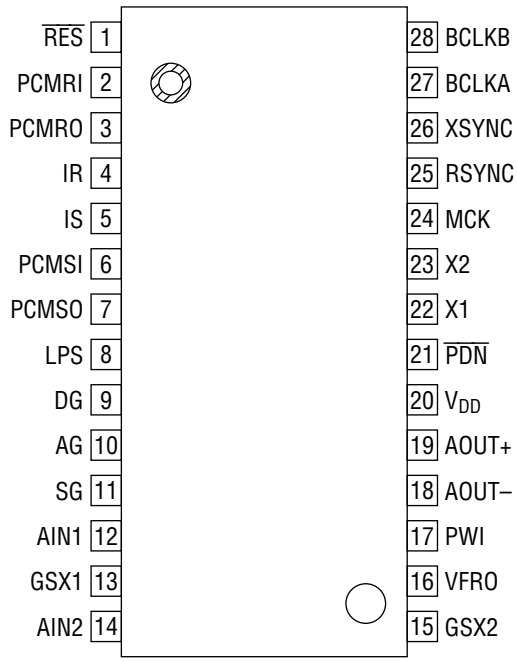
FEATURES

- Single 5 V Power Supply Operation
- ADPCM Algorithm : Complies completely with 1988's version ITU-T G.721 (32 kbps)
- Transmit/Receive Full-Duplex Operation
- Transmit/Receive Synchronous Mode Only
- Serial ADPCM Transmission Data Rate : 32 kbps to 2048 kbps
- Serial PCM Transmission Data Rate : 64 kbps to 2048 kbps
- PCM Interface Coding Format
  - MSM7540 : A-law or Linear (14-bit, 2's compliment) Selectable
  - MSM7560 : μ-law or Linear (14-bit, 2's compliment) Selectable
- Low Power Consumption
  - Operating Mode : 60 mW Typ.
  - Power-Down Mode : 1.0 mW Typ.
- Two Analog Input Amplifier Stages : Externally Adjustable Gain
- Analog Output Stage : Push-pull Drive (direct drive of 350 Ω + 120 nF)
- Built-in Crystal Oscillator (10.368 MHz)
- Built-in Reference Voltage Supply
- Option Reset Specified by ITU-T G. 721/ADPCM
- Package:
  28-pin plastic SOP (SOP28-P-430-1.27-K) (Product name: MSM7540GS-K)
  (Product name: MSM7560GS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



28-Pin Plastic SOP

PIN AND FUNCTIONAL DESCRIPTIONS

AIN1, AIN2, GSX1, GSX2

Transmit analog inputs and the output for transmit gain adjustment.
AIN1 (AIN2) connects to the inverting input of the internal transmit amplifier. GSX1 (GSX2) connects to the internal transmit amplifier output. Refer to Fig. 1 for gain adjustment.

VFRO, AOUT+, AOUT–, PWI

Receive analog output and the output for receive gain adjustment.
VFRO is the receive filter output. AOUT+ and AOUT– are differential analog signal outputs which can directly drive Z_L = 350 Ω + 120 nF. Refer to Fig. 1 for gain adjustment.

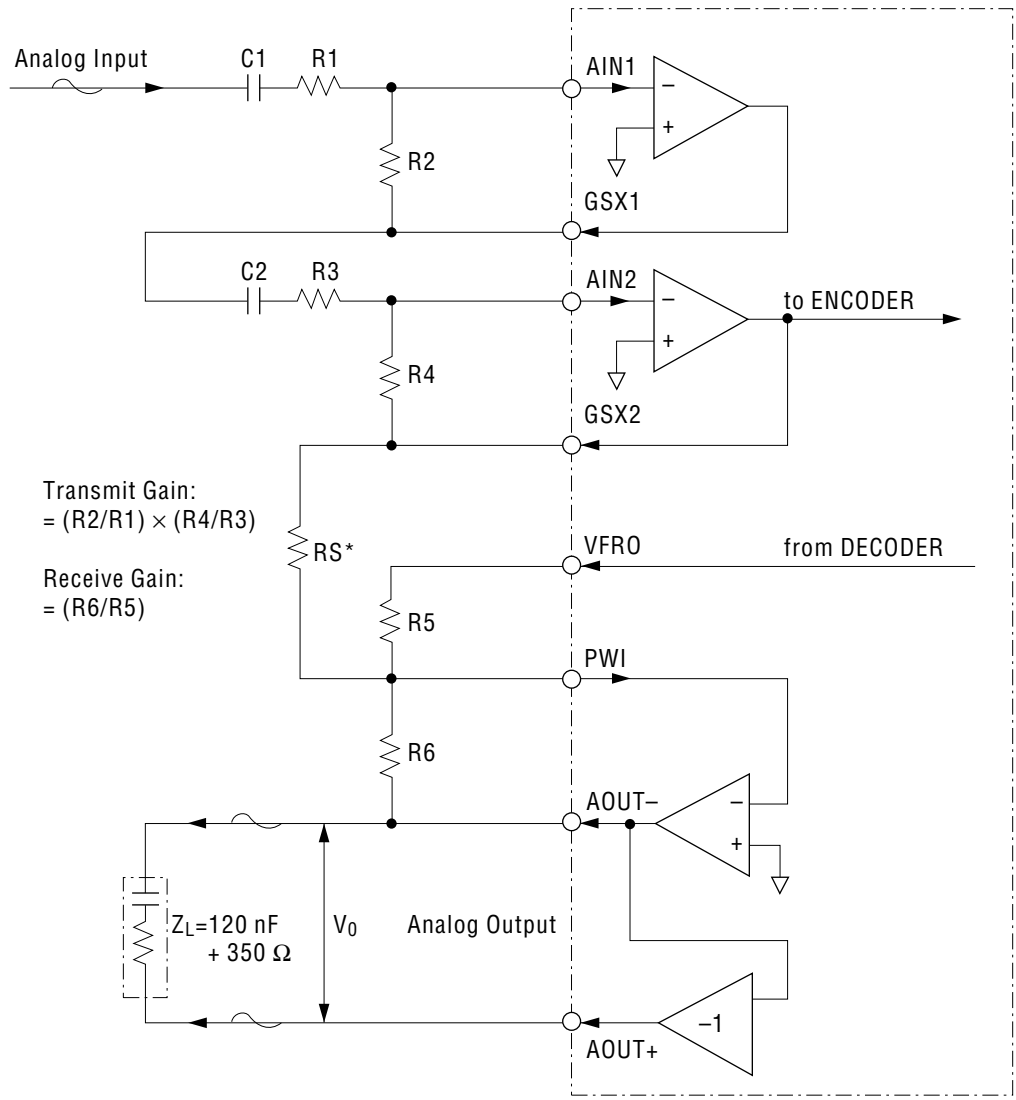


Figure 1 Analog Input/Output Interface

SG

Analog signal ground voltage output.
The output voltage of this pin is approximately 2.4 V. Put bypass capacitors between this pin and the AG pin. During power-down this output voltage is 0 V. The external SG voltage, if necessary, should be used via a buffer.

AG

Analog ground.

DG

Digital ground.
This ground is separated internally from the analog signal ground pin (AG). The DG pin must be kept as close as possible to AG on the PCB.

V_{DD}

+5 V power supply.

LPS

PCM coding law selection.
MSM7540 only ; if this pin goes to a "0" level, PCMSO, PCMSI, PCMRO, and PCMRI become the A-law character signal, and if these pins goes to a "1" level, the signal becomes a linear value character signal (2's complement).
MSM7560 only ; if this pin goes to a "0" level, PCMSO, PCMSI, PCMRO, and PCMRI become the μ-law character signal, and if these pins goes to a "1" level, the signal becomes a linear value character signal (2's complement).

$\overline{PDN}$

Power down control input.
If this pin is "0", this device is in the power-down state.
Normally, this pin is set to "1".

$\overline{RES}$

Optional reset input specified by ITU-T Recommendation G. 721.
If this pin is "0", the device is in the reset state. The reset width (during "L") should be 125μs or more.

MCK

Master clock input.
The frequency must be 10.368 MHz. The master clock signal may be asynchronous to BCLKA, BCLKB, XSYNC, and RSYNC.

PCMSO

Transmit PCM data output.
PCM is output from MSB in synchronization with the rising edge of BCLKB and XSYNC.

PCMSI

Transmit PCM data input.
This signal is converted to the transmit ADPCM data. PCM is shifted in synchronization with the falling edge of BCLKB. Normally, this pin is connected to PCMSO.

PCMRO

Receive PCM data output.
PCM is the output signal after ADPCM decoder processing. This signal is output serially from MSB in synchronization with the rising edge of BCLKB and RSYNC.

PCMRI

Receive PCM data input.
PCM is shifted on the falling edge of the BCLKB and input from MSB. Normally, this pin is connected to PCMRO.

IS

Transmit ADPCM signal output.
After having encoded PCM with ADPCM, this signal is output from MSB in synchronization with the rising edge of BCLKA and XSYNC . This pin is an open drain output and remains in a high impedance state during power-down. IS requires a pull-up resistor.

IR

Receive ADPCM signal input.
The ADPCM signal is shifted in series and synchronization with the falling edge of BCLKA and RSYNC, starting with MSB.

BCLKB

Shift clock input for the PCM data (PCMSO, PCMSI, PCMRO, PCMRI).
The frequency is set in the 64 kHz to 2048 kHz range.

XSYNC

8 kHz synchronous signal input for transmit PCM and ADPCM data.
Synchronize this signal with BCLKA and BCLKB signal. XSYNC is used to indicate the MSB of the serial PCM and ADPCM data stream.
Be sure to input the XSYNC signal because it is also used as the input of the timing generator.

RSYNC

8 kHz synchronous signal input for receive PCM and ADPCM data.
Synchronize this signal with BCLKA and BCLKB signal. RSYNC is used to indicate the MSB of the serial PCM and ADPCM data stream.

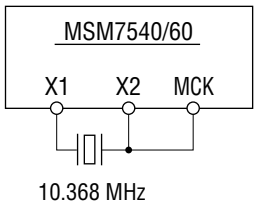
BCLKA

Shift clock input for the ADPCM data (IS, IR).
The frequency is set in the range of 32 kHz to 2048 kHz.

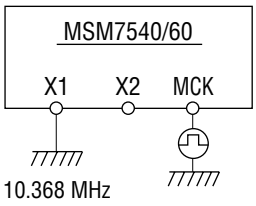
X1, X2

Crystal oscillator (10.368 MHz) connection.
Connect X2, the clock output pin, directly to the MCK pin.
When using a conventional external clock of 10.368 MHz, X1 should be connected to the ground, leave X2 open, and provide the external clock through the MCK pin.

<Using a self-oscilation circuit>



<Using an external clock>



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	—	–0.3 to +7	V
Analog Input Voltage	V_{AIN}	—	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	—	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	Voltage must be fixed	4.5	—	5.5	V
Operating Temperature	Ta	—	–25	+25	+70	°C
Input High Voltage	V_{IH}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLKA, BCLKB, IR, LPS, PDN, RES	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLKA, BCLKB, IR, LPS, PDN, RES	0	—	0.6	V
Master Clock Frequency	f_{MCK}	MCK	–0.01%	10.368	+0.01%	MHz
Bit Clock Freqency	f_{BCKA}	BCLKA	32	—	2048	kHz
	f_{BCKB}	BCLKB	64	—	2048	kHz
Synchronous Signal Frequency	f_{SYMC}	XSYNC, RSYNC	—	8.0	—	kHz
Clock Duty Ratio	D_C	MCK, BCLKA, BCLKB	30	50	70	%
Digital Input Rise Time	t_{Ir}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLKA, BCLKB, IR, LPS, PDN, RES	—	—	50	ns
Digital Input Fall Time	t_{If}	MCK, XSYNC, RSYNC, PCMRI, PCMSI, BCLKA, BCLKB, IR, LPS, PDN, RES	—	—	50	ns
Transmit Sync Signal Setting Time	t_{XS}	BCLKA, BCLKB to XSYNC	100	—	—	ns
	t_{XS}	XSYNC to BCLKA, BCLKB	100	—	—	ns
Receive Sync Signal Setting Time	t_{RS}	BCLKA, BCLKB to RSYNC	100	—	—	ns
	t_{SR}	RSYNC to BCLKA, BCLKB	100	—	—	ns
Synchronous Signal Width	t_{WS}	XSYNC, RSYNC	1 BCLK	—	100	µs
PCM, ADPCM Set-up Time	t_{DS}	—	100	—	—	ns
PCM, ADPCM Hold Time	t_{DH}	—	100	—	—	ns
Digital Output Load	R_{DL}	IS (Pull-up Resistor)	500	—	—	Ω
	C_{DL}	IS, PCMSO, PCMRO	—	—	100	pF
Bypass Capacitor for SG	C_{SG}	SG↔GND	—	10 + 0.1	—	µF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating Mode, (When no signal, and V_{DD} = 5.0 V)	—	12	24	mA
	I_{DD2}	Power Down Mode (When V_{DD} = 5.0 V)	—	0.2	0.5	mA
Input High Voltage	V_{IH}	—	2.2	—	V_{DD}	V
Input Low Voltage	V_{IL}	—	0.0	—	0.6	V
Input Leakage Current	I_{IH}	$V_I = V_{DD}$	—	—	2.0	µA
	I_{IL}	V_I = 0 V	—	—	0.5	µA
Output Low Voltage	V_{OL}	1 LSTTL, Pull-up: 500 Ω	0.0	0.2	0.4	V
Output Leakage Current	I_O	IS	—	—	10	µA
Input Capacitance	C_{IN}	—	—	5	—	pF

Transmit Analog Interface Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	AIN1, AIN2	10	—	—	MΩ
Output Load Resistance	R_{LGX}	GSX1, GSX2	50	—	—	kΩ
Output Load Capacitance	C_{LGX}	GSX1, GSX2	—	—	100	pF
Output Amplitude	V_{OGX}	GSX1, GSX2, R_L = 50 kΩ	—	—	*2.226	V_{PP}
Input Offset Voltage	V_{OFGX}	Pre–OPAMPs	–20	—	+20	mV
SG Output Voltage	V_{SG}	—	—	2.4	—	V
SG Output Impedance	R_{SG}	—	—	40	80	kΩ
SG Rise Time	T_{SG}	SG↔GND 10 µF + 0.1 µF (Rise time to 90% of max. level)	—	700	—	ms

* –3 dBm (600 Ω) = 0 dBm0, + 3.14 dBm0 = 2.226 V_{PP} (MSM7540)
–3 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 2.226 V_{PP} (MSM7560)

Receive Analog Interface Characteristics

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Input Resistance	R_{INPW}	PWI		10	—	—	MΩ
Output Load Resistance	R_{LVF}	VFRO		50	—	—	kΩ
	R_{LAO}	AOUT+, AOUT–		1.2	—	—	kΩ
Output Capacitance	C_{LVF}	VFRO		—	—	100	pF
	C_{LAO}	AOUT+, AOUT–		—	—	100	pF
Output Voltage Level	V_{OVF}	VFRO	R_L = 50 kΩ	—	—	*2.226	V_{PP}
	V_{OAO}	AOUT+, AOUT–	R_L = 1.2 kΩ	—	—	*2.226	V_{PP}
			Z_L = 350 Ω + 120 nF(See Fig.1)	—	—	*2.226	V_{PP}
Offset Voltage	V_{OFVF}	VFRO		–100	—	+100	mV
	V_{OFAO}	AOUT+, AOUT– (GAIN = 0 dB), Power amp only		–20	—	+20	mV
Open Loop Gain	G_{DB}	Power amp (0.3 to 3.4 kHz, Z_L = 350 Ω + 120 nF)(See Fig.1)		40	—	—	dB

* –3 dBm (600 Ω) = 0 dBm0, + 3.14 dBm0 = 2.226 V_{PP} (MSM7540)
–3 dBm (600 Ω) = 0 dBm0, + 3.17 dBm0 = 2.226 V_{PP} (MSM7560)

AC Chracteristics

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Transmit Frequency Response	L_{OSS} T1	0 to 60	0	—	25	—	—	dB
	L_{OSS} T2	300 to 3000			–0.15	—	+0.20	dB
	L_{OSS} T3	1020			Reference			dB
	L_{OSS} T4	3300			–0.15	—	+0.80	dB
	L_{OSS} T5	3400			0	—	0.80	dB
	L_{OSS} T6	3968.75			14	—	—	dB
Receive Frequency Response	L_{OSS} R1	0 to 3000	0	—	–0.15	—	+0.20	dB
	L_{OSS} R2	1020			Reference			dB
	L_{OSS} R3	3300			–0.15	—	+0.80	dB
	L_{OSS} R4	3400			0	—	0.80	dB
	L_{OSS} R5	3968.75			14	—	—	dB
Transmit Signal to Distortion Ratio	SD T1	1020	3	(*1)	35	—	—	dB
	SD T2		0		35	—	—	dB
	SD T3		–30		35	—	—	dB
	SD T4		–40		28	—	—	dB
	SD T5		–45		23	—	—	dB
Receive Signal to Distortion Ratio	SD R1	1020	3	(*1)	35	—	—	dB
	SD R2		0		35	—	—	dB
	SD R3		–30		35	—	—	dB
	SD R4		–40		28	—	—	dB
	SD R5		–45		23	—	—	dB
Transmit Gain Tracking	GT T1	1020	3	—	–0.2	—	+0.2	dB
	GT T2		–10		Reference			dB
	GT T3		–40		–0.2	—	+0.2	dB
	GT T4		–50		–0.5	—	+0.5	dB
	GT T5		–55		–1.2	—	+1.2	dB
Receive Gain Tracking	GT R1	1020	3	—	–0.2	—	+0.2	dB
	GT R2		–10		Reference			dB
	GT R3		–40		–0.2	—	+0.2	dB
	GT R4		–50		–0.5	—	+0.5	dB
	GT R5		–55		–1.2	—	+1.2	dB

*1 Use the P-message weighted filter

AC Characteristics (Continued)

(V_{DD} = 4.5 V to 5.5 V, Ta = –25°C to +70°C)

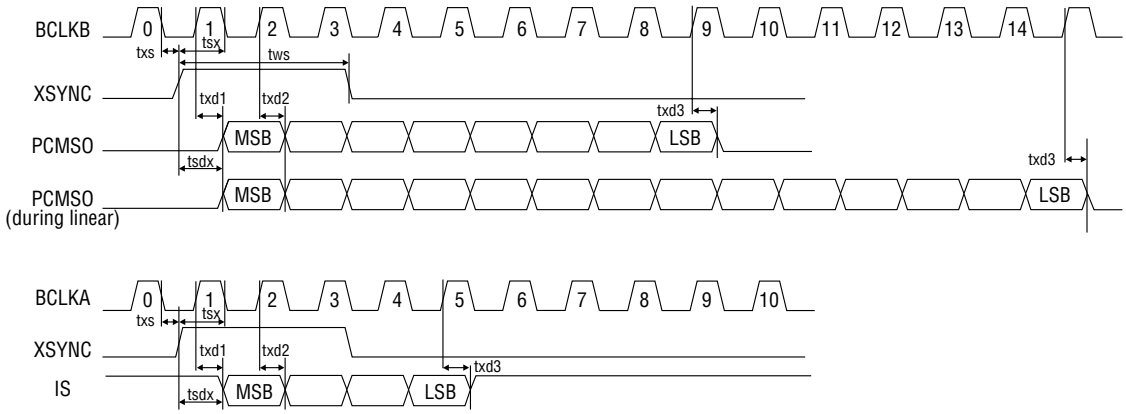
Parameter	Symbol	Condition			Min.	Typ.	Max.	Unit
		Freq. (Hz)	Level (dBm0)	Others				
Idle Channel Noise	N_{IDLT}	—	AIN = SG	(*1)	—	—	–69 (–72)	dBm0p (dBmp)
	N_{IDLR}	—	—	(*1) (*2)	—	—	–72 (–75)	
Absolute Signal Amplitude	A_{VT}	1020	0	GSX2	0.488	0.548 (*3)	0.615	Vrms
	A_{VR}			VFRO	0.488	0.548 (*3)	0.615	Vrms
Power Supply Noise Rejection Ratio	P_{SRRT}	Noise Freq. : 0 to 50 kHz	Noise Level : 50 mV_{PP}	—	30	—	—	dB
	P_{SRRR}				30	—	—	dB
Digital Output Delay Time	t_{SDX}	—	1 LSTTL + 100 pF, Pull-up: 500 Ω	—	50	—	200	ns
	t_{SDR}				50	—	200	ns
	t_{XD1}, t_{RD1}				50	—	200	ns
	t_{XD2}, t_{RD2}				50	—	200	ns
	t_{XD3}, t_{RD3}				50	—	200	ns

*1 Use the P-message weighted filter
*2 PCMRI input code "11010101"(MSM7540)
"11111111"(MSM7560)
*3 0.548 Vrms = 0 dBm0= –3 dBm

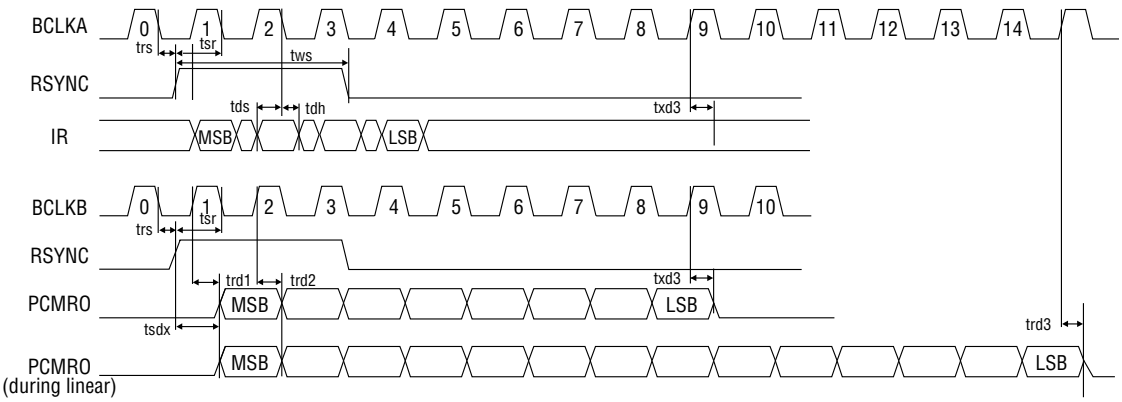
Note: All ADPCM coder and decoder characteristics comply with ITU-T Recommendation G.721.

TIMING DIAGRAM

Transmit Side PCM/ADPCM Data Interface



Receive Side PCM/ADPCM Data Interface

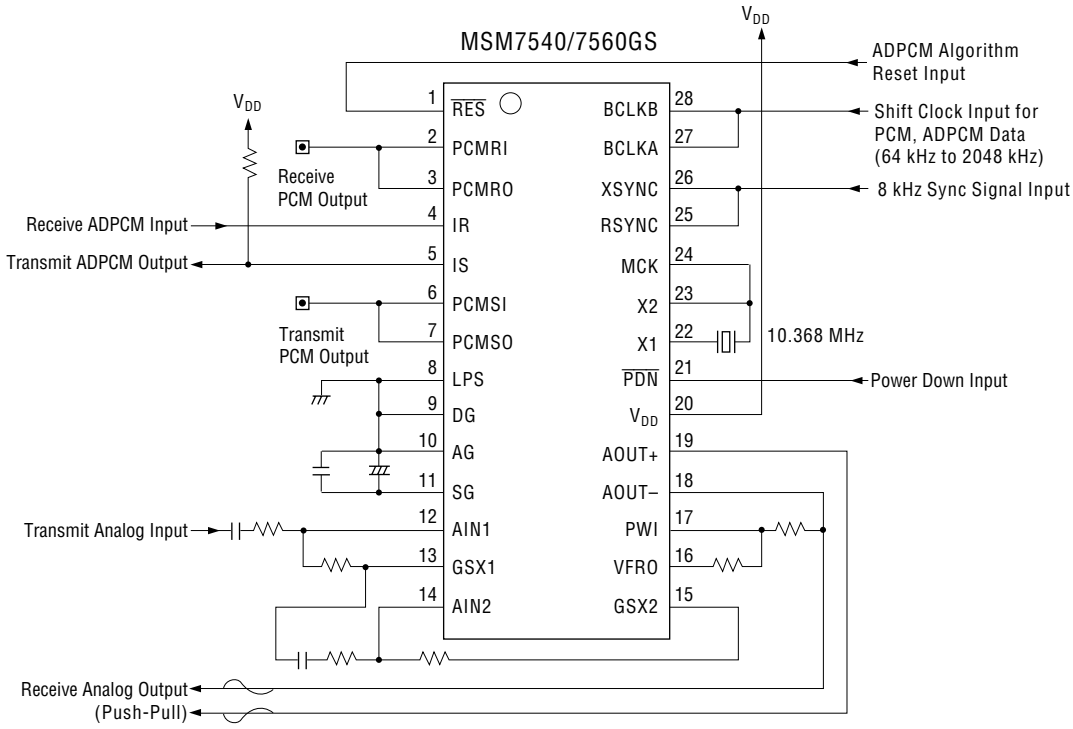


Note: Linear format

A code of an input/output level is determined by the 14-bit 2'compliment.
Refer to the table below for code format.

Input/Output level	MSB to LSB
+Full-scall	01111111111111
0	00000000000000
–Full-scall	10000000000000

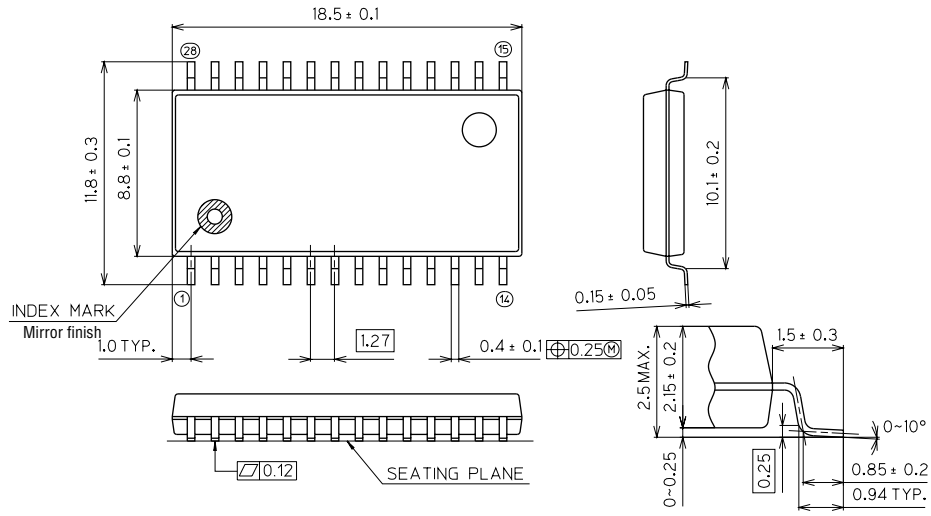
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

(Unit : mm)

SOP28-P-430-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.75 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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