# **OKI** Semiconductor

# MSM9554/MSM9555

**LSI Devices for FM Multiplex Data Demodulation**

## GENERAL DESCRIPTION

The MSM9554 and MSM9555 are LSI devices which demodulate FM character multiplex signals in the DARC (DAta Radio Channel)[*1] format to acquire digital data. The MSM9554 and MSM9555 operate on 5V and 3V, respectively. In the DARC format, baseband signals at ordinary FM broadcasting frequencies are multiplexed with 16k-bps digital data which are L-MSK-modulated at 76kHz.

Each of the MSM9554 and MSM9555 has a bandpass filter consisting of SCF, frame synchronization circuit, and error correction circuit, on a single chip.

So, a system for acquisition of digital data can be easily constructed by externally mounting an FM receiver tuner, microcontroller for control, and memory for temporary storage of data.

The MSM9554 and MSM9555 have a simple configuration, and are equipped with only necessary functions. By making changes to software for the external microcontroller, the MSM9554 and MSM9555 can meet the various requirements of FM multiplex broadcasting services which will be offered in future.

These devices are best suited to the car radios and car navigation systems supporting VICSs (Vehicle Information and Communication System)[*2] that have been serviced since Aprit, 1996.

*1 DARC is a registered trademark of NHK ENGINEERING SERVICES, INC.
Note that a contract needs to be made with NHK Engineering Service if a manufacturer produces/sells electronic equipment utilizing the DARC technology.
*2 If samples or detail documents are to be provided, contracts with VICS center are reqired beforehand.

## FEATURES

- Built-in discrambler supporting VICS
- Pin compatible with MSM9552/MSM9553
- Built-in bandpass filter (SCF)
- Built-in timer internal to block
- Built-in block synchronization circuit and frame synchronization circuit
- Setting of the number of synchronization protecting stages
- Regeneration of data clocks by digital PLL
- 1T delay detection
- Built-in error correction circuit
- Built-in layer 4 and layer 2 CRC check circuit
- Microcontroller parallel interface
- Clock output for external devices (64kHz to 8.192MHz selectable)
- International standard frame format
- Power source: 5V (MSM9554), 3V (MSM9555)
- Package
  44-pin plastic QFP (QFP44-P-910-0.80-2K) (Product name: MSM9554GS-2K/MSM9555GS-2K)
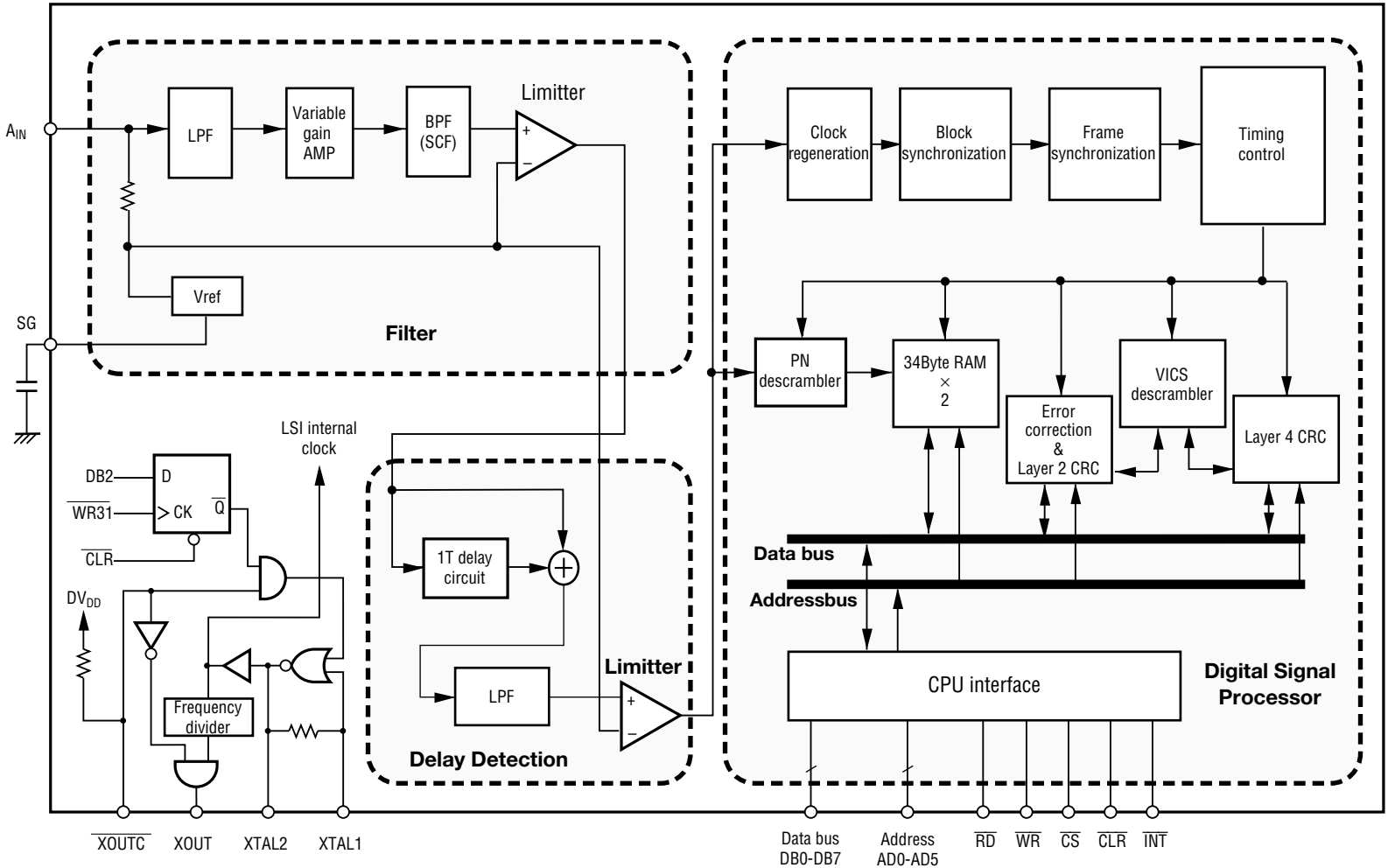
## PIN CONFIGURATION (TOP VIEW)
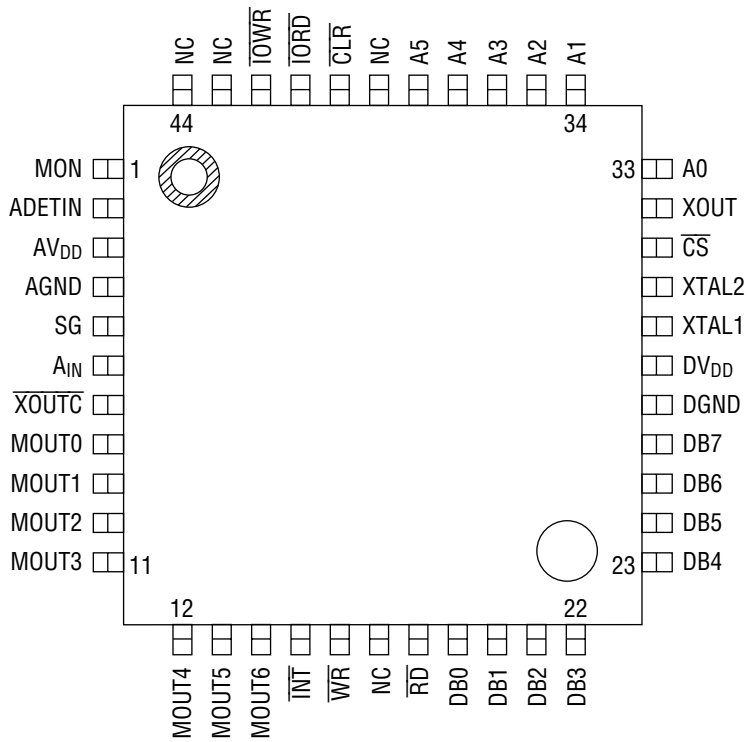


Note: Leave the NC pins open.

**44-Pin Plastic QFP**

## PIN DESCRIPTION

| Function | Pin | Symbol | Type | Description |
|---|---|---|---|---|
| Micro-controller interface | 16 | $\overline{\text{WR}}$ | I | Write signal to internal register |
| | 18 | $\overline{\text{RD}}$ | I | Read signal to internal register |
| | 15 | $\overline{\text{INT}}$ | O | Interrupt signal to microcontroller. "L": Occurrence of an interrupt |
| | 31 | $\overline{\text{CS}}$ | I | Chip select signal. "L": Read, write, and data bus signals valid |
| | 40 | $\overline{\text{CLR}}$ | I | "L" initializes internal registers, and the device enters power down mode |
| | 33 to 38 | A0 to A5 | I | Address signal to internal register |
| | 19 to 26 | DB0 to DB7 | I/O | Data bus signal to internal register |
| Tuner interface | 6 | $A_{IN}$ | I | FM multiplex signal input |
| | 5 | SG | O | Analog reference voltage output pin. To prevent noise, connect a capacitor between this pin and analog ground. |
| Analog section test | 1 | MON | O | Analog section waveform monitor pin. The analog block is specified by the analog control register. |
| | 2 | ADETIN | I | Analog signal input pin for testing |
| Digital section test | 41<br>42 | $\overline{\text{IORD}}$<br>$\overline{\text{IOWR}}$ | I | Digital section test signal input pins. Internally pulled up. |
| | 8 to 14 | MOUT0 to MOUT6 | O | Digital section test signal output and monitor output pins |
| Clock | 29 | XTAL1 | I | 8.192MHz crystal oscillator connection pin |
| | 30 | XTAL2 | O | 8.192MHz crystal oscillator connection pin |
| | 32 | XOUT | O | Pin for supply of 64kHz to 8.192MHz clock to the outside |
| | 7 | $\overline{\text{XOUTC}}$ | I | XOUT output control pin. "L"=Clock output, "H"=Output disabled. Pulled up internally. |
| Power supply | 3 | $AV_{DD}$ | — | Analog section power supply pin |
| | 4 | AGND | — | Analog ground pin |
| | 28 | $DV_{DD}$ | — | Digital section power supply pin |
| | 27 | DGND | — | Digital ground pin |

## ABSOLUTE MAXIMUM RATINGS (MSM9554)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $AV_{DD}$ $DV_{DD}$ | $AV_{DD}=DV_{DD}$ Ta=25°C | −0.3 to +7.0 | V |
| Input voltage Output voltage | $V_I$ $V_O$ | | −0.3 to $AV_{DD}$+0.3 −0.3 to $DV_{DD}$+0.3 | |
| Maximum power dissipation | $P_D$ | Ta=25°C per package | 400 | mW |
| | | Ta=25°C per output | 50 | |
| Storage temperature | $T_{STG}$ | — | −55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS (MSM9554)

| Parameter | Symbol | Condition | Range | Unit | Applied Pin |
|---|---|---|---|---|---|
| Power supply voltage | $AV_{DD}$ $DV_{DD}$ | $AV_{DD}=DV_{DD}$ | 4.5 to 5.5 | V | $AV_{DD}$ $DV_{DD}$ |
| Crystal frequency | $f_{XTAL}$ | — | 8.192MHz ±100ppm | — | XTAL1 XTAL2 |
| FM multiplex signal input voltage | $V_{AIN}$ | Composite signals, including multiplex signals | 0.5 to 2 | $V_{P-P}$ | $A_{IN}$ |
| Operating temperature | $T_{OP}$ | — | −40 to +85 | °C | — |

## ELECTRICAL CHARACTERISTICS (MSM9554)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit | Applied Pin |
|---|---|---|---|---|---|---|---|
| Current consumption | $I_{DD}$ | During operation, No load f=8.192MHz | — | 18 | 34 | mA | $AV_{DD}$ $DV_{DD}$ |
| | | During power down, No load | — | — | 20 | µA | |
| BPF pass band attenuation | GAIN1 | 72 - 80kHz Variable gain amplifier gain: 0dB | — | — | 3.0 | dB | MON |
| BPF reject band attenuation | GAIN2 | 0 - 53kHz Variable gain amplifier gain: 0dB | 50 | — | — | dB | MON |
| BPF reject band attenuation | GAIN3 | 100 - 500kHz Variable gain amplifier gain: 0dB | 50 | — | — | dB | MON |

## ABSOLUTE MAXIMUM RATINGS (MSM9555)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $AV_{DD}$ $DV_{DD}$ | $AV_{DD}=DV_{DD}$ Ta=25°C | −0.3 to +7.0 | V |
| Input voltage Output voltage | $V_I$ $V_O$ | | −0.3 to $AV_{DD}$+0.3 −0.3 to $DV_{DD}$+0.3 | |
| Maximum power dissipation | $P_D$ | Ta=25°C per package | 400 | mW |
| | | Ta=25°C per output | 50 | |
| Storage temperature | $T_{STG}$ | — | −55 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS (MSM9555)

| Parameter | Symbol | Condition | Range | Unit | Applied Pin |
|---|---|---|---|---|---|
| Power supply voltage | $AV_{DD}$ $DV_{DD}$ | $AV_{DD}=DV_{DD}$ | 2.7 to 3.3 | V | $AV_{DD}$ $DV_{DD}$ |
| Crystal frequency | $f_{XTAL}$ | — | 8.192MHz ±100ppm | — | XTAL1 XTAL2 |
| FM multiplex signal input voltage | $V_{AIN}$ | Composite signals, including multiplex signals | 0.2 to 0.9 | $V_{P-P}$ | $A_{IN}$ |
| Operating temperature | $T_{OP}$ | — | −20 to +75 | °C | — |

## ELECTRICAL CHARACTERISTICS (MSM9555)

| Parameter | Symbol | Condition | MIN | TYP | MAX | Unit | Applied Pin |
|---|---|---|---|---|---|---|---|
| Current consumption | $I_{DD}$ | During operation, No load f=8.192MHz | — | 14 | 23 | mA | $AV_{DD}$ $DV_{DD}$ |
| | | During power down, No load | — | — | 10 | μA | |
| BPF pass band attenuation | GAIN1 | 72 - 80kHz Variable gain amplifier gain: 0dB | — | — | 3.0 | dB | MON |
| BPF reject band attenuation (1) | GAIN2 | 0 - 53kHz Variable gain amplifier gain: 0dB | 50 | — | — | dB | MON |
| BPF reject band attenuation (2) | GAIN3 | 100 - 500kHz Variable gain amplifier gain: 0dB | 50 | — | — | dB | MON |

MSM9554 or MSM9555

8 bit

FM tuner

FM multiplex data demodulation device

PLL

MCU

SRAM

Font ROM

Display

Keys