



**MT4C4001J(L)**  
**1 MEG x 4 DRAM**

# DRAM

# 1 MEG x 4 DRAM

STANDARD OR LOW POWER,  
EXTENDED REFRESH

DRAM

## FEATURES

- 1,024-cycle refresh distributed across 16ms (MT4C4001J) or 128ms (MT4C4001J L)
- Industry-standard x4 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS-ONLY, CAS-BEFORE-RAS (CBR), HIDDEN and BATTERY BACKUP (BBU) (MT4C4001J only)
- FAST-PAGE-MODE access cycle
- Low power, 1mW standby; 275mW active, typical (MT4C4001J L)

## OPTIONS

- Timing
- 60ns access
- 70ns access
- 80ns access

## MARKING

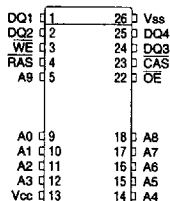
- Packages
 

Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)*	TG
Plastic ZIP (400 mil)	Z
- Version
 

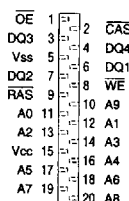
1,024-cycle refresh in 16ms	None
1,024-cycle refresh in 128ms	L
- Part Number Example: MT4C4001JDJ-6 L

## PIN ASSIGNMENT (Top View)

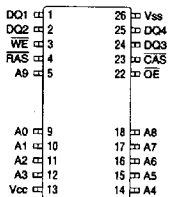
### 20-Pin SOJ (DC-1)



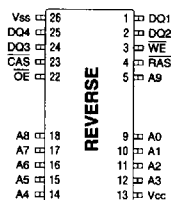
### 20-Pin ZIP (DB-2)



### 20-Pin TSOP (DD-1)



### 20-Pin TSOP\* (DD-1)



\*Consult factory on availability of reverse pinout TSOP packages.

## GENERAL DESCRIPTION

The MT4C4001J L is a randomly accessed solid-state memory containing 4,194,304 bits organized in a x4 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. RAS is used to latch the first 10 bits and CAS the latter 10 bits. READ and WRITE cycles are selected with the WE input. A logic HIGH on WE dictates READ mode while a logic LOW on WE dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE or CAS, whichever occurs last. If WE goes LOW prior to CAS going LOW, the output pin(s) remain open (High-Z) until the next CAS cycle. If WE goes LOW after data reaches the output pins, the outputs (Qs) are activated and retain the selected cell data as long as CAS remains LOW (regardless of WE or RAS). This late WE pulse results in a

READ-WRITE cycle. The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by WE and OE.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by RAS followed by a column-address strobed-in by CAS. CAS may be toggled-in by holding RAS LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS HIGH terminates the FAST-PAGE-MODE operation.

Returning RAS and CAS HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the



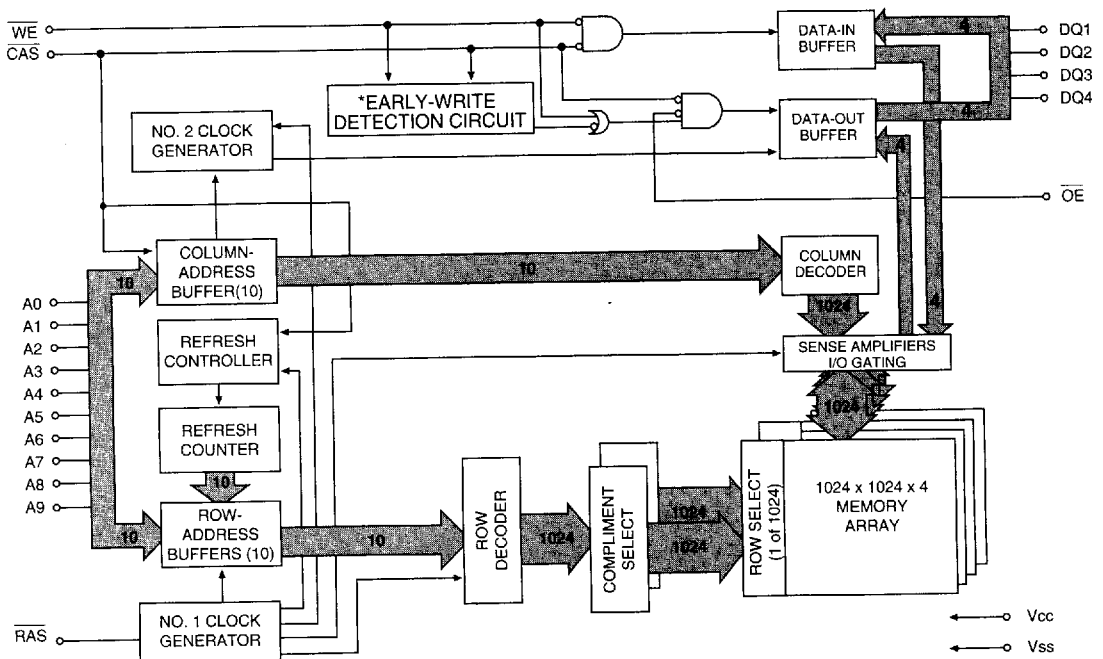
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$\overline{\text{RAS}}$  HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE) or  $\overline{\text{RAS}}$  REFRESH cycle ( $\overline{\text{RAS}}$ -ONLY, CBR, or HIDDEN) so that all 1,024 combinations of  $\overline{\text{RAS}}$  ad-

resses (A0-A9) are executed at least every 16ms for the MT4C4001J and every 128ms for the MT4C4001L, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic  $\overline{\text{RAS}}$  addressing.

**FUNCTIONAL BLOCK DIAGRAM**  
**FAST-PAGE-MODE**



- \*NOTE:**
1.  $\overline{\text{WE}}$  LOW prior to  $\overline{\text{CAS}}$  LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
  2.  $\overline{\text{CAS}}$  LOW prior to  $\overline{\text{WE}}$  LOW, EW detection circuit output is a LOW (LATE-WRITE)



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**TRUTH TABLE**

FUNCTION	RAS	CAS	WE	OE	ADDRESSES		DATA-IN/OUT
					'R	'C	DQ1-DQ4
Standby	H	H→X	X	X	X	X	High-Z
READ	L	L	H	L	ROW	COL	Data-Out
EARLY-WRITE	L	L	L	X	ROW	COL	Data-In
READ-WRITE	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ	1st Cycle L	H→L	H	L	ROW	COL	Data-Out
FAST-PAGE-MODE READ	2nd Cycle L	H→L	H	L	n/a	COL	Data-Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle L	H→L	L	X	ROW	COL	Data-In
FAST-PAGE-MODE EARLY-WRITE	2nd Cycle L	H→L	L	X	n/a	COL	Data-In
FAST-PAGE-MODE READ-WRITE	1st Cycle L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
FAST-PAGE-MODE READ-WRITE	2nd Cycle L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS-ONLY REFRESH	L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ L→H→L	L	H	L	ROW	COL	Data-Out
HIDDEN REFRESH	WRITE L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH	H→L	L	H	X	X	X	High-Z
BBU REFRESH (MT4C4001J L only)	H→L	L	H	X	X	X	High-Z



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**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to V<sub>SS</sub> ..... -1V to +7V  
 Operating Temperature, T<sub>A</sub> (ambient) ..... 0°C to +70°C  
 Storage Temperature (plastic) ..... -55°C to +150°C  
 Power Dissipation ..... 1W  
 Short Circuit Output Current ..... 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(Notes: 1, 3, 4, 6, 7) (V<sub>CC</sub> = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V <sub>CC</sub>	4.5	5.5	V	1
Input High (Logic 1) Voltage, all inputs	V <sub>IH</sub>	2.4	V <sub>CC</sub> +1	V	1
Input Low (Logic 0) Voltage, all inputs	V <sub>IL</sub>	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ 6.5V (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V <sub>OUT</sub> ≤ 5.5V)	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS Output High Voltage (I <sub>OUT</sub> = -5mA)	V <sub>OH</sub>	2.4		V	
Output Low Voltage (I <sub>OUT</sub> = 4.2mA)	V <sub>OL</sub>		0.4	V	

PARAMETER/CONDITION	VERSION	SYMBOL	MAX			UNITS	NOTES
			-6	-7	-8		
STANDBY CURRENT: (TTL) (RAS = CAS = V <sub>IH</sub> )		I <sub>CC1</sub>	2	2	2	mA	
STANDBY CURRENT: (CMOS) (RAS = CAS = V <sub>CC</sub> - 0.2V)	MT4C4001J	I <sub>CC2</sub>	1	1	1	mA	
	MT4C4001J L	I <sub>CC2</sub>	200	200	200	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS, CAS, Single Address Cycling: t <sub>RC</sub> = t <sub>RC</sub> [MIN])		I <sub>CC3</sub>	110	100	90	μA	3, 4, 30
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current (RAS = V <sub>IL</sub> , CAS, Address Cycling: t <sub>PC</sub> = t <sub>PC</sub> [MIN])		I <sub>CC4</sub>	80	70	60	μA	3, 4, 30
REFRESH CURRENT: RAS-ONLY Average power supply current (RAS Cycling, CAS = V <sub>IH</sub> : t <sub>RC</sub> = t <sub>RC</sub> [MIN])		I <sub>CC5</sub>	110	100	90	μA	3, 30
REFRESH CURRENT: CBR Average power supply current (RAS, CAS, Address Cycling: t <sub>RC</sub> = t <sub>RC</sub> [MIN])		I <sub>CC6</sub>	110	100	90	μA	3, 5
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: CAS = 0.2V or CBR cycling; RAS = t <sub>RAS</sub> (MIN) to 300ns; WE, A0-A9 and D <sub>IN</sub> = V <sub>CC</sub> - 0.2V or 0.2V; (D <sub>IN</sub> may be left open); t <sub>RC</sub> = 125μs (1,024 rows at 125μs = 128ms)	MT4C4001J L	I <sub>CC7</sub>	300	300	300	μA	3, 5, 7, 28



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**CAPACITANCE**

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9	C <sub>I1</sub>		5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C <sub>I2</sub>		7	pF	2
Input/Output Capacitance: DQ	C <sub>I0</sub>		7	pF	2

**DRAM**

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) (V<sub>CC</sub> = 5V ±10%)

AC CHARACTERISTICS	PARAMETER	SYM	-6		-7		-8		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	t <sub>RC</sub>		110		130		150		ns	
READ-WRITE cycle time	t <sub>RWC</sub>		150		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t <sub>PC</sub>		35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t <sub>PRWC</sub>		85		100		105		ns	
Access time from RAS	t <sub>RAC</sub>			60		70		80	ns	14
Access time from CAS	t <sub>CAC</sub>			15		20		20	ns	15
Output Enable	t <sub>OE</sub>			15		20		20	ns	23
Access time from column-address	t <sub>AA</sub>			30		35		40	ns	
Access time from CAS precharge	t <sub>CPA</sub>			35		40		45	ns	
RAS pulse width	t <sub>RAS</sub>	60	100,000	70	100,000	80	100,000		ns	
RAS pulse width (FAST-PAGE-MODE)	t <sub>RASP</sub>	60	200,000	70	200,000	80	200,000		ns	
RAS hold time	t <sub>RSH</sub>	15		20		20			ns	
RAS precharge time	t <sub>RP</sub>	40		50		60			ns	
CAS pulse width	t <sub>CAS</sub>	15	100,000	20	100,000	20	100,000		ns	
CAS hold time	t <sub>CSH</sub>	60		70		80			ns	
CAS precharge time (CBR REFRESH)	t <sub>CPN</sub>	10		10		10			ns	16
CAS precharge time (FAST-PAGE-MODE)	t <sub>CP</sub>	10		10		10			ns	
RAS to CAS delay time	t <sub>RCD</sub>	20	45	20	50	20	60		ns	17
CAS to RAS precharge time	t <sub>CRP</sub>	10		10		10			ns	
Row-address setup time	t <sub>ASR</sub>	0		0		0			ns	
Row-address hold time	t <sub>RAH</sub>	10		10		10			ns	
RAS to column-address delay time	t <sub>RAD</sub>	15	30	15	35	15	40		ns	18
Column-address setup time	t <sub>ASC</sub>	0		0		0			ns	
Column-address hold time	t <sub>CAH</sub>	10		15		15			ns	
Column-address hold time (referenced to RAS)	t <sub>AR</sub>	50		55		60			ns	
Column-address to RAS lead time	t <sub>RAL</sub>	30		35		40			ns	
Read command setup time	t <sub>RCS</sub>	0		0		0			ns	
Read command hold time (referenced to CAS)	t <sub>RCH</sub>	0		0		0			ns	19
Read command hold time (referenced to RAS)	t <sub>RRH</sub>	0		0		0			ns	19
CAS to output in Low-Z	t <sub>CLZ</sub>	0		0		0			ns	
Output buffer turn-off delay	t <sub>OFF</sub>	3	15	3	20	3	20		ns	20, 29

**MICRON****MT4C4001J(L)**  
**1 MEG x 4 DRAM****ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes: 6, 7, 8, 9, 10, 11, 12, 13, 23) ( $V_{CC} = 5V \pm 10\%$ )**DRAM**

AC CHARACTERISTICS	PARAMETER	SYM	-6		-7		-8		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
WE command setup time	$t_{WCS}$	0		0		0		ns	21, 27	
Write command hold time	$t_{WCH}$	10		15		15		ns		
Write command hold time (referenced to RAS)	$t_{WCR}$	45		55		60		ns		
Write command pulse width	$t_{WP}$	10		15		15		ns		
Write command to RAS lead time	$t_{RWL}$	15		20		20		ns		
Write command to CAS lead time	$t_{CWL}$	15		20		20		ns		
Data-in setup time	$t_{DS}$	0		0		0		ns	22	
Data-in hold time	$t_{DH}$	10		15		15		ns	22	
Data-in hold time (referenced to RAS)	$t_{DHR}$	45		55		60		ns		
RAS to WE delay time	$t_{RWD}$	90		100		110		ns	21	
Column-address to WE delay time	$t_{AWD}$	55		65		70		ns	21	
CAS to WE delay time	$t_{CWD}$	40		50		50		ns	21	
Transition time (rise or fall)	$t_T$	3	50	3	50	3	50	ns	9, 10	
Refresh period (1,024 cycles) MT4C4001J / MT4C4001J L	$t_{REF}$		16 / 128		16 / 128		16 / 128	ms		
RAS to CAS precharge time	$t_{RPC}$	0		0		0		ns		
CAS setup time (CBR REFRESH)	$t_{CSR}$	10		10		10		ns	5	
CAS hold time (CBR REFRESH)	$t_{CHR}$	10		10		10		ns	5	
WE hold time (CBR REFRESH)	$t_{WRH}$	10		10		10		ns	25	
WE setup time (CBR REFRESH)	$t_{WRP}$	10		10		10		ns	25	
WE hold time (WCBR test cycle)	$t_{WTH}$	10		10		10		ns	25	
WE setup time (WCBR test cycle)	$t_{WTS}$	10		10		10		ns	25	
OE setup prior to RAS during HIDDEN REFRESH cycle	$t_{ORD}$	0		0		0		ns		
Output disable	$t_{OD}$		15		20		20	ns	27	
OE hold time from WE during READ-MODIFY-WRITE cycle	$t_{OEH}$	15		20		20		ns	26	

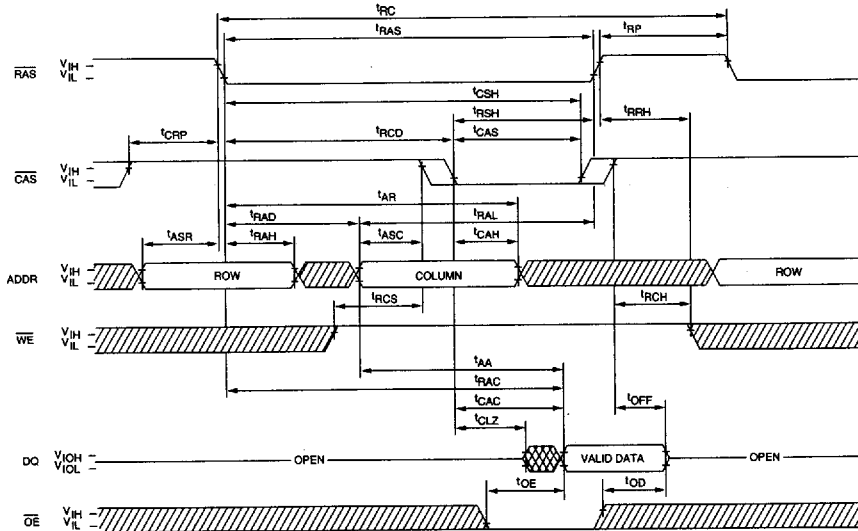
**MICRON**  
SEMICONDUCTOR INC
**MT4C4001J(L)**  
**1 MEG x 4 DRAM**
**DRAM**

## NOTES

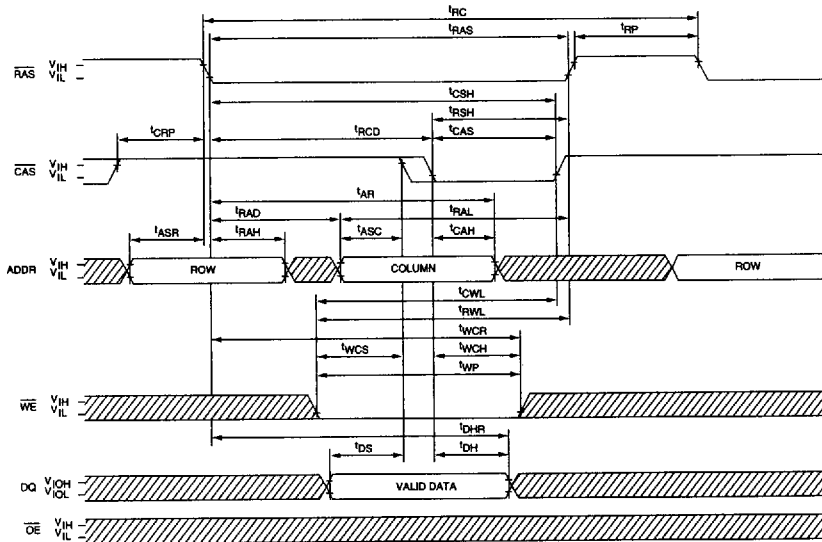
- All voltages referenced to V<sub>SS</sub>.
- This parameter is sampled. V<sub>CC</sub> = 5V ±10%; f = 1 MHz.
- I<sub>CC</sub> is dependent on cycle rates.
- I<sub>CC</sub> is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
- An initial pause of 100μs is required after power-up followed by eight RAS refresh cycles (RAS-ONLY or CBR with  $\overline{WE}$  HIGH) before proper device operation is assured. The eight RAS cycle wake-ups should be repeated any time the  $\overline{REF}$  refresh requirement is exceeded.
- AC characteristics assume  $t_T = 5ns$ .
- V<sub>IH</sub> (MIN) and V<sub>IL</sub> (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>).
- In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
- If  $\overline{CAS} = V_{IH}$ , data output is High-Z.
- If  $\overline{CAS} = V_{IL}$ , data output may contain data from the last valid READ cycle.
- Measured with a load equivalent to two TTL gates and 100pF.
- Assumes that  $t_{RCD} < t_{RCD} (MAX)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
- Assumes that  $t_{RCD} \geq t_{RCD} (MAX)$ .
- If  $\overline{CAS}$  is LOW at the falling edge of  $\overline{RAS}$ , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{CAS}$  must be pulsed HIGH for  $t_{CPN}$ .
- Operation within the  $t_{RCD} (MAX)$  limit ensures that  $t_{RAC} (MAX)$  can be met.  $t_{RCD} (MAX)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD} (MAX)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
- Operation within the  $t_{RAD} (MAX)$  limit ensures that  $t_{RAC} (MIN)$  and  $t_{CAC} (MIN)$  can be met.  $t_{RAD} (MAX)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD} (MAX)$  limit, then access time is controlled exclusively by  $t_{AA}$ .
- Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
- $t_{OFF} (MAX)$  defines the time at which the output achieves the open circuit condition, and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.  $t_{WCS}$  applies to EARLY-WRITE cycles.  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  apply to READ-MODIFY-WRITE cycles. If  $t_{WCS} \geq t_{WCS} (MIN)$ , the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD} (MIN)$ ,  $t_{AWD} \geq t_{AWD} (MIN)$  and  $t_{CWD} \geq t_{CWD} (MIN)$ , the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate.  $\overline{OE}$  held HIGH and  $\overline{WE}$  taken LOW after  $\overline{CAS}$  goes LOW results in a LATE-WRITE ( $\overline{OE}$ -controlled) cycle.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not applicable in a LATE-WRITE cycle.
- These parameters are referenced to  $\overline{CAS}$  leading edge in EARLY-WRITE cycles and  $\overline{WE}$  leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
- If  $\overline{OE}$  is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
- A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case,  $\overline{WE} = LOW$  and  $\overline{OE} = HIGH$ .
- $t_{WTS}$  and  $t_{WTH}$  are setup and hold specifications for the  $\overline{WE}$  pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverses of  $t_{WRP}$  and  $t_{WRH}$  in the CBR refresh cycle.
- LATE-WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OD}$  and  $t_{OEH}$  met ( $\overline{OE}$  HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If  $\overline{OE}$  is taken back LOW while  $\overline{CAS}$  remains LOW, the DQs will remain open.
- The DQs open during READ cycles once  $t_{OD}$  or  $t_{OFF}$  occur. If  $\overline{CAS}$  goes HIGH before  $\overline{OE}$ , the DQs will open regardless of the state of  $\overline{OE}$ . If  $\overline{CAS}$  stays LOW while  $\overline{OE}$  is brought HIGH, the DQs will open. If  $\overline{OE}$  is brought back LOW ( $\overline{CAS}$  still LOW), the DQs will provide the previously read data.
- BBU current is reduced as  $t_{RAS}$  is reduced from its maximum specification during the BBU cycle.
- The 3ns minimum is a parameter guaranteed by design.
- Column-address changed once while  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .

**DRAM**

**READ CYCLE**



**EARLY-WRITE CYCLE**



DON'T CARE  
 UNDEFINED

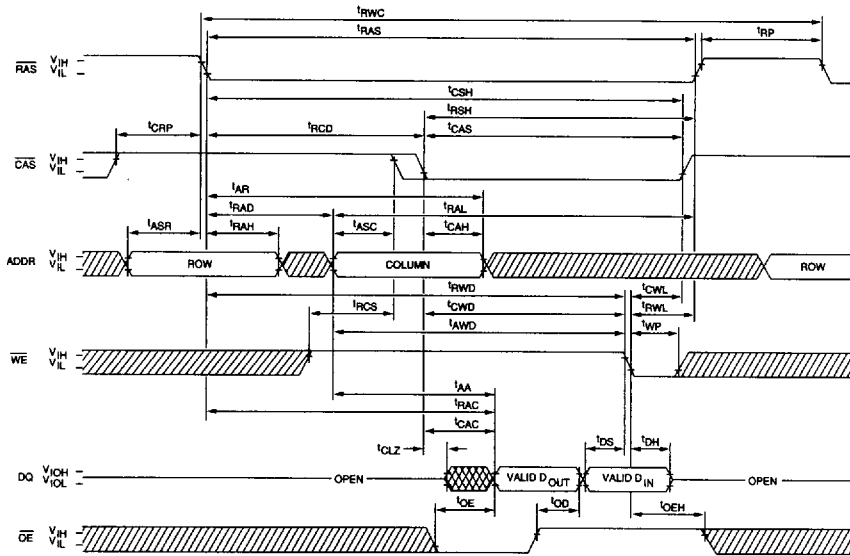




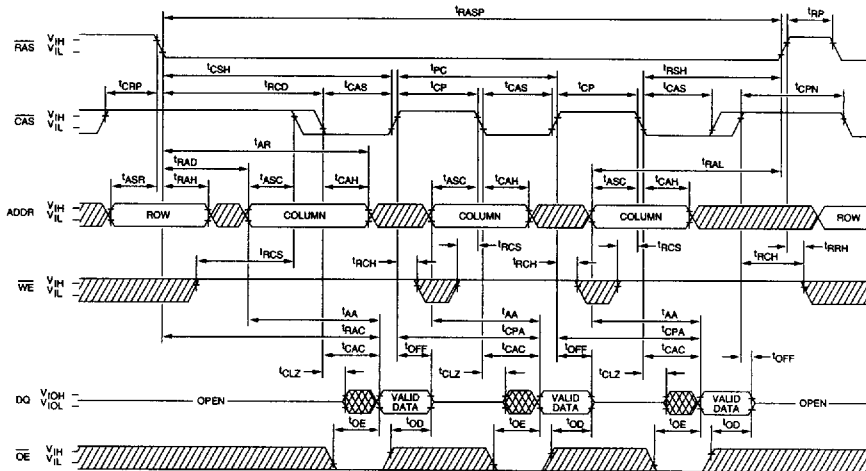
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1 MEG x 4 DRAM

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**READ-WRITE CYCLE**  
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



**FAST-PAGE-MODE READ CYCLE**

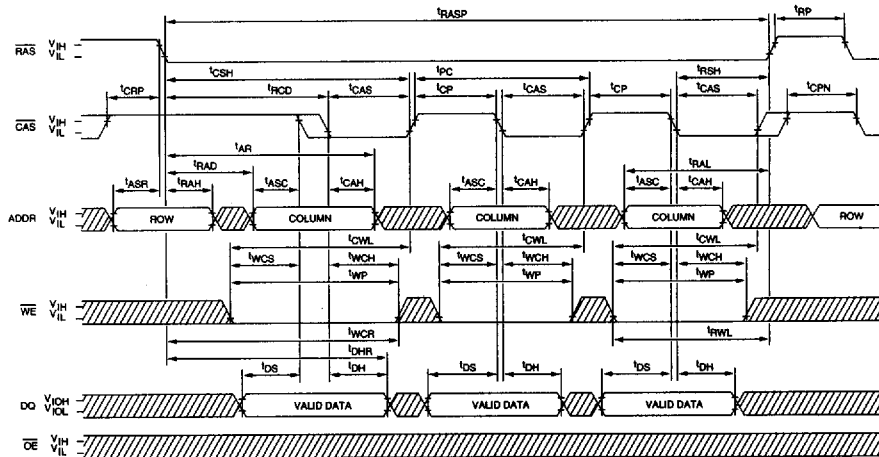


▨ DON'T CARE  
▩ UNDEFINED

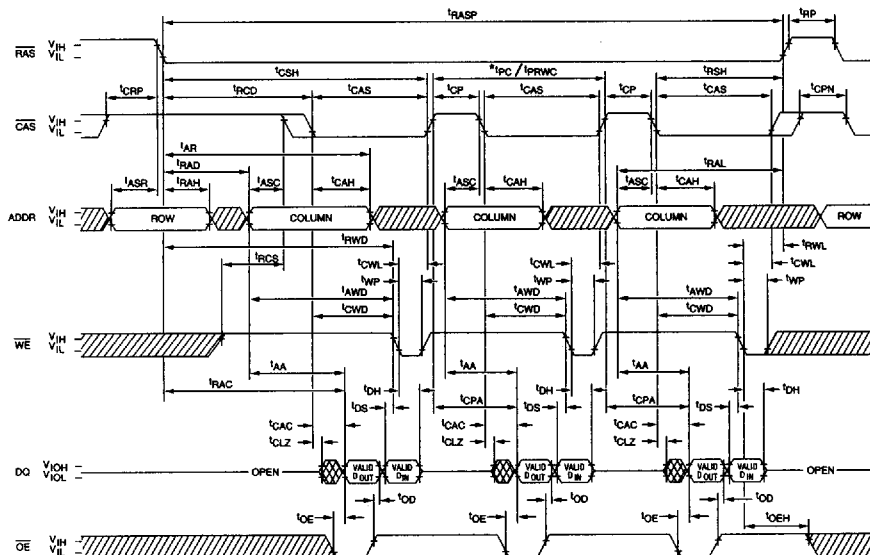


MT4C4001J(L)  
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### FAST-PAGE-MODE EARLY-WRITE CYCLE



### FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)

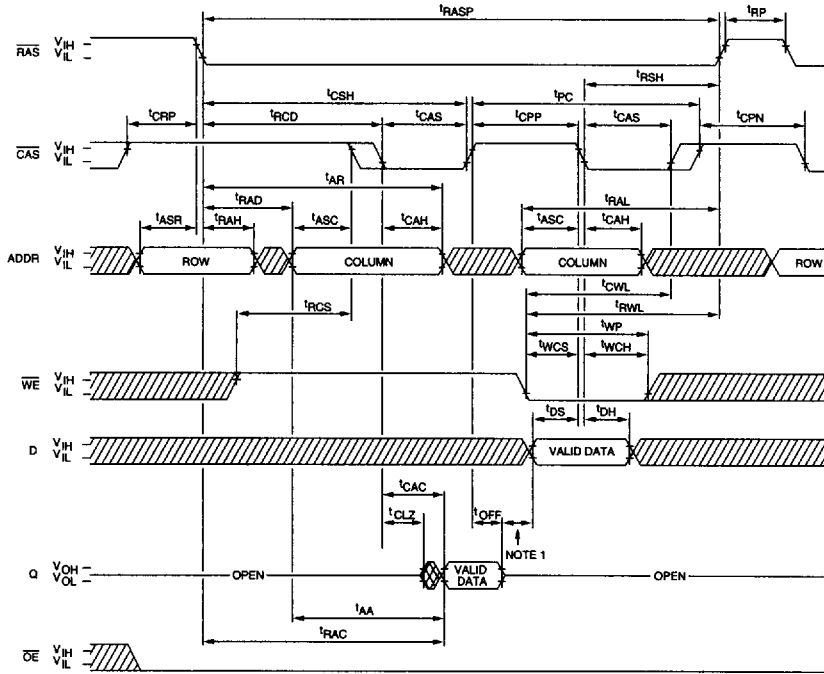


 DON'T CARE  
 UNDEFINED

\*tPC is for LATE-WRITE only.

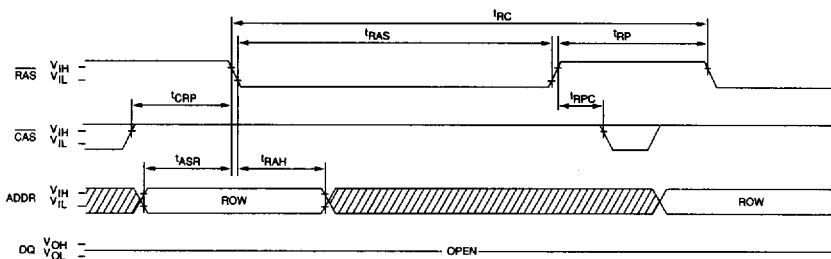
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**FAST-PAGE-MODE READ-EARLY-WRITE CYCLE**  
(Pseudo READ-MODIFY-WRITE)



**NOTE:** 1. Do not drive data prior to tristate:  $t_{CPP}(\text{MIN})$  or  $t_{CP}(\text{whichever is greater}) + t_{DS}(\text{MIN})$  + any guardband between data-out and driving the bus with the new data-in.

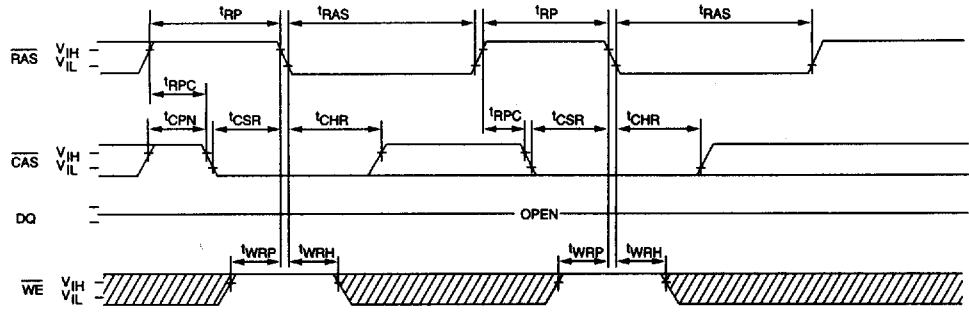
**RAS-ONLY REFRESH CYCLE**  
(ADDR = A0-A9; WE = DON'T CARE)



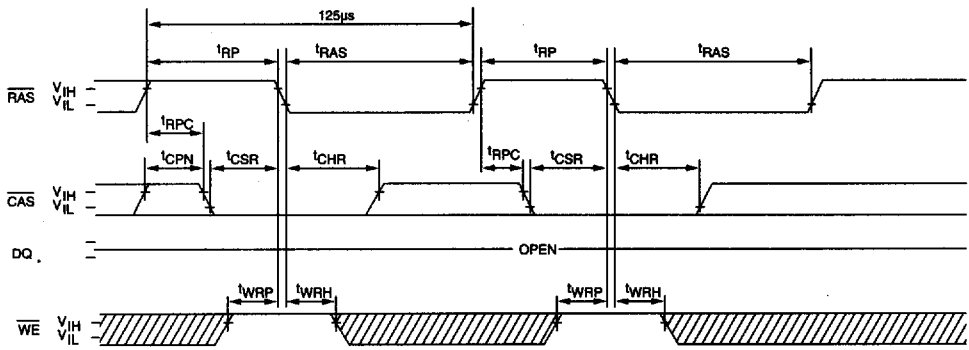
▨ DON'T CARE  
▩ UNDEFINED

**CBR REFRESH CYCLE**  
 (A0-A9 and  $\overline{OE}$  = DON'T CARE)

**DRAM**



**BBU REFRESH CYCLE (MT4C4001J L only)**  
 (A0-A9 and  $\overline{OE}$  = DON'T CARE)



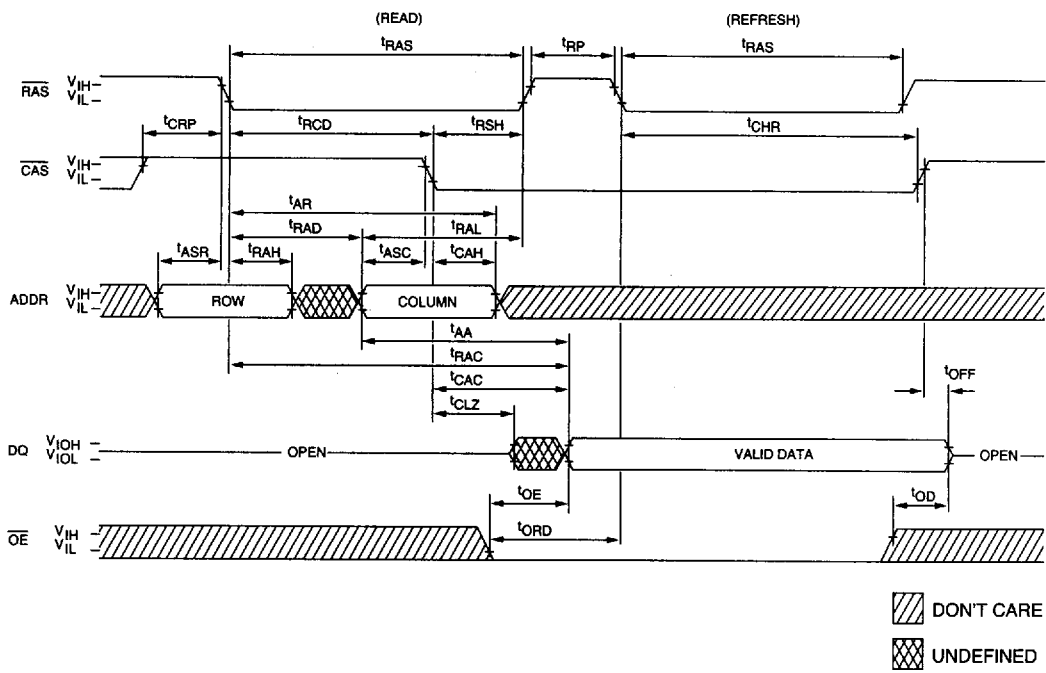
 DON'T CARE  
 UNDEFINED



MT4C4001J(L)  
1 MEG x 4 DRAM

DRAM

**HIDDEN REFRESH CYCLE<sup>24</sup>**  
(WE = HIGH; OE = LOW)





MT4C4001J(L)  
1 MEG x 4 DRAM

DRAM

### 4 MEG POWER-UP AND REFRESH CONSTRAINTS

The EIA/JEDEC 4 Meg DRAM introduces two potential incompatibilities compared to the previous generation 1 Meg DRAM. The incompatibilities involve refresh and power-up. Understanding these incompatibilities and providing for them will offer the designer and system user greater compatibility between the 1 Meg and 4 Meg.

### REFRESH

The most commonly used refresh cycle of the 1 Meg is the CBR REFRESH cycle. The CBR for the 1 Meg specifies the  $\overline{WE}$  pin as a "don't care." The 4 Meg, on the other hand, specifies the CBR REFRESH mode with the  $\overline{WE}$  pin held at a voltage HIGH level.

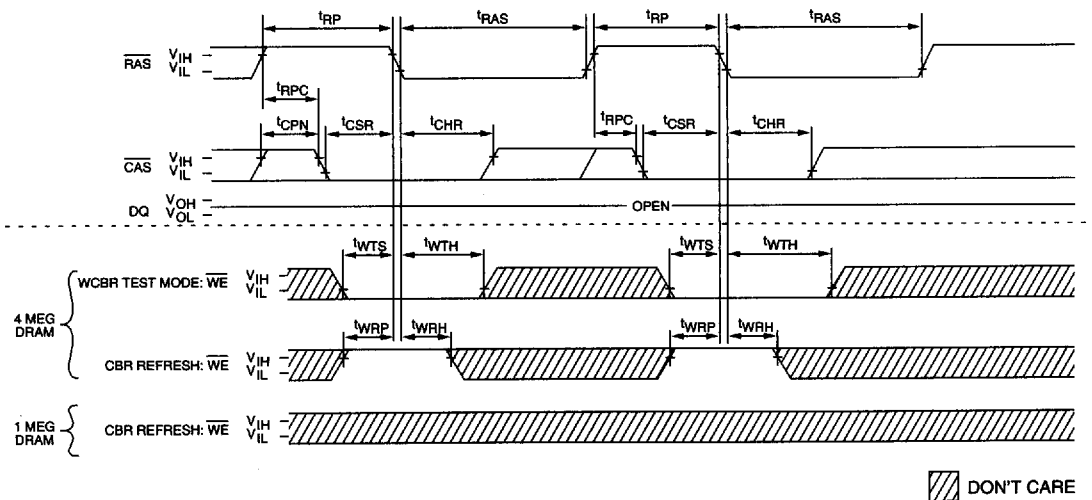
A CBR cycle with  $\overline{WE}$  LOW will put the 4 Meg into the JEDEC-specified test mode (WCBR).

### POWER-UP

The 4 Meg JEDEC test mode constraint may introduce another problem. The 1 Meg POWER-UP cycle requires a 100 $\mu$ s delay followed by any eight  $\overline{RAS}$  cycles. The 4 Meg POWER-UP is more restrictive in that eight  $\overline{RAS}$ -ONLY REFRESH or CBR REFRESH ( $\overline{WE}$  held HIGH) cycles must be used. The restriction is needed since the 4 Meg may power-up in the JEDEC-specified test mode and must exit out of the test mode. The only way to exit the 4 Meg JEDEC test mode is with either a  $\overline{RAS}$ -ONLY REFRESH cycle or a CBR REFRESH cycle ( $\overline{WE}$  held HIGH).

### SUMMARY

1. The 1 Meg CBR REFRESH allows the  $\overline{WE}$  pin to be "don't care" while the 4 Meg CBR requires  $\overline{WE}$  to be HIGH.
2. The eight  $\overline{RAS}$  wake-up cycles on the 1 Meg may be any valid  $\overline{RAS}$  cycle while the 4 Meg may only use  $\overline{RAS}$ -ONLY or CBR REFRESH cycles ( $\overline{WE}$  held HIGH).



### COMPARISON OF 4 MEG TEST MODE AND WCBR TO 1 MEG CBR