

DRAM

MT4LC16M4A7, MT4LC16M4T8

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/mti/msp/html/datasheet.html

FEATURES

- Single +3.3V $\pm 0.3V$ power supply
- Industry-standard x4 pinout, timing, functions, and packages
- 13 row, 11 column addresses (A7)
12 row, 12 column addresses (T8)
- High-performance CMOS silicon-gate process
- All inputs, outputs and clocks are LVTTTL-compatible
- FAST-PAGE-MODE (FPM) access
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) REFRESH distributed across 64ms
- Optional self refresh (S) for low-power data retention

OPTIONS

- Refresh Addressing
4,096 (4K) rows
8,192 (8K) rows
- Plastic Packages
32-pin SOJ (400 mil)
32-pin TSOP (400 mil)
- Timing
50ns access
60ns access
- Refresh Rates
Standard Refresh
Self Refresh (128ms period)

MARKING

T8
A7

DJ
TG

None
S*

NOTE: 1. The 16 Meg x 4 FPM DRAM base number differentiates the offerings in one place—MT4LC16M4A7. The fifth field distinguishes various options: A7 designates an 8K refresh and T8 designates a 4K refresh for FPM DRAMs.
2. The # symbol indicates signal is active LOW.

*Contact factory for availability

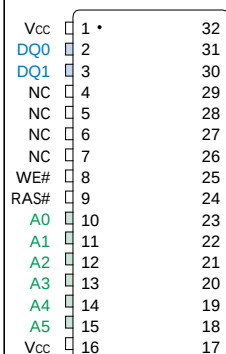
Part Number Example:
MT4LC16M4A7DJ

KEY TIMING PARAMETERS

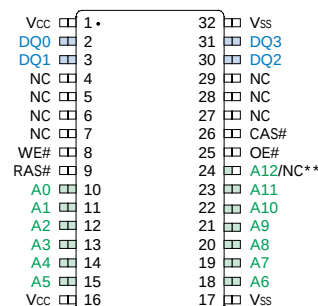
SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}
-5	90ns	50ns	30ns	25ns	13ns
-6	110ns	60ns	35ns	30ns	15ns

PIN ASSIGNMENT (Top View)

32-Pin SOJ



32-Pin TSOP



**A12 on A7 version and NC on T8 version

16 MEG x 4 FPM DRAM PART NUMBERS

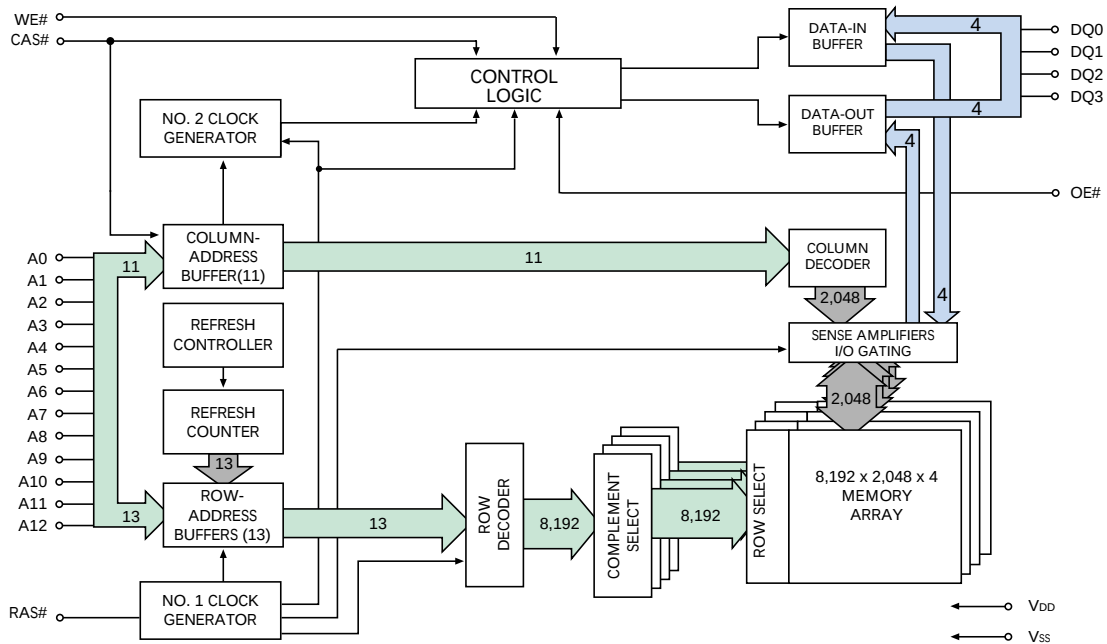
PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC16M4A7DJ-x	8K	SOJ	Standard
MT4LC16M4A7DJ-x S	8K	SOJ	Self
MT4LC16M4A7TG-x	8K	TSOP	Standard
MT4LC16M4A7TG-x S	8K	TSOP	Self
MT4LC16M4T8DJ-x	4K	SOJ	Standard
MT4LC16M4T8DJ-x S	4K	SOJ	Self
MT4LC16M4T8TG-x	4K	TSOP	Standard
MT4LC16M4T8TG-x S	4K	TSOP	Self

x = speed

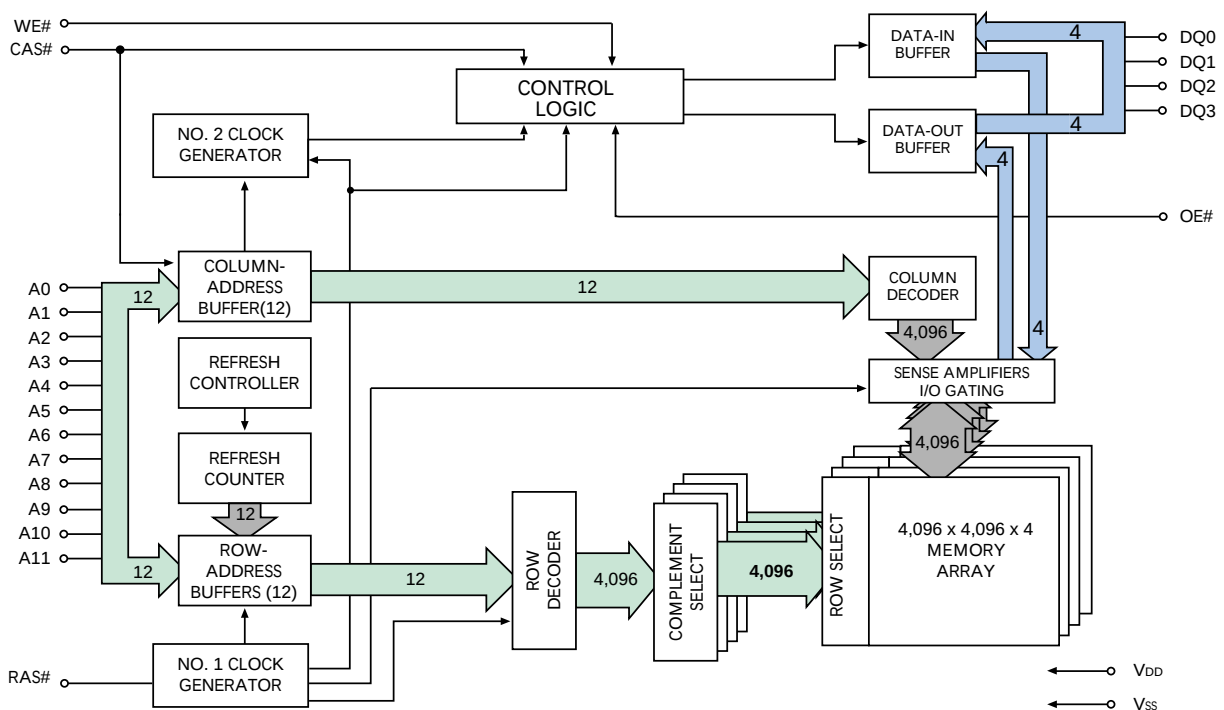
GENERAL DESCRIPTION

The 16 Meg x 4 DRAMs are high-speed CMOS, dynamic random-access memory devices containing 67,108,864 bits organized in a x4 configuration. The MT4LC16M4A7 and MT4LC16M4T8 are functionally organized as 16,777,216 locations containing four bits each. The 16,777,216 memory locations are arranged in 8,192 rows by 2,048 columns for the MT4LC16M4A7 or 4,096 rows by 4,096 columns for the MT4LC16M4T8. During READ or WRITE cycles, each location is uniquely

FUNCTIONAL BLOCK DIAGRAM MT4LC16M4A7 (13 row addresses)



FUNCTIONAL BLOCK DIAGRAM MT4LC16M4T8 (12 row addresses)



GENERAL DESCRIPTION (continued)

addressed via the address bits. First, the row address is latched by the RAS# signal, then the column address by CAS#. Both devices provide FAST-PAGE-MODE operation, allowing for fast successive data operations (READ, WRITE, or READ-MODIFY-WRITE) within a given row.

The MT4LC16M4A7 and MT4LC16M4T8 must be refreshed periodically in order to retain stored data.

FAST PAGE MODE ACCESS

Each location in the DRAM is uniquely addressable as mentioned in the General Description. The data for each location is accessed via the four I/O pins (DQ0-DQ3). The WE# signal must be activated to execute a WRITE operation; otherwise, a READ operation will be performed. The OE# signal must be activated to enable the DQ output drivers for a read access and can be deactivated to disable output data if necessary.

FAST-PAGE-MODE operations are always initiated with a row address strobed in by the RAS# signal, followed by a column address strobed in by CAS#, just like for single location accesses. However, subsequent column locations within the row may then be accessed at the page mode cycle time. This is accomplished by cycling CAS# while holding RAS# LOW and entering new column addresses with each CAS# cycle. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

DRAM REFRESH

The supply voltage must be maintained at the specified levels, and the refresh requirements must be met in order to retain stored data in the DRAM. The refresh requirements are met by refreshing all 8,192 rows (A7) or all 4,096 rows (T8) in the DRAM array at least once every 64ms. The recommended procedure is to execute 4,096 CBR REFRESH cycles, either uniformly spaced or grouped in bursts, every 64ms. The MT4LC16M4A7 internally refreshes two rows for every CBR cycle,

whereas the MT4LC16M4T8 refreshes one row for every CBR cycle. So with either device, executing 4,096 CBR cycles covers all rows. The CBR refresh will invoke the internal refresh counter for automatic RAS# addressing. Alternatively, RAS#-ONLY REFRESH capability is inherently provided. However, with this method only one row is refreshed at a time; so for the MT4LC16M4A7, 8,192 RAS#-ONLY REFRESH cycles must be executed every 64ms to cover all rows. Some compatibility issues may become apparent. JEDEC strongly recommends the use of CBR REFRESH for this device.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified t_{RASS}. The "S" option allows for an extended refresh period of 128ms, or 31.25μs per row for a 4K refresh and 15.625μs per row for an 8K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of t_{RPS}. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed CBR refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes RAS#-ONLY or burst CBR refresh sequence, all rows must be refreshed within the average internal refresh rate prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Relative to V_{SS} -1V to +4.6V
 Voltage on NC, Inputs or I/O Pins

Relative to V_{SS} -1V to +4.6V
 Operating Temperature, T_A (ambient) ... 0°C to +70°C
 Storage Temperature (plastic) -55°C to +150°C
 Power Dissipation 1W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V _{CC}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V _{IH}	2	V _{CC} + 0.3	V	26
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V _{IL}	-0.3	0.8	V	26
INPUT LEAKAGE CURRENT: Any input at V _{IN} (0V ≤ V _{IN} ≤ V _{CC} + 0.3V); All other pins not under test = 0V	I _I	-2	2	μA	
OUTPUT HIGH VOLTAGE: I _{OUT} = -2mA	V _{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I _{OUT} = 2mA	V _{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V _{OUT} (0V ≤ V _{OUT} ≤ V _{CC} + 0.3V); DQ is disabled and in High-Z state	I _{OZ}	-5	5	μA	

ICC OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 2, 3, 5, 6) ($V_{CC} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	SPEED	4K REFRESH	8K REFRESH	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I _{cc1}	ALL	1	1	mA	
STANDBY CURRENT: CMOS (RAS# = CAS# $\geq V_{CC} - 0.2V$, DQs may be left open, other inputs: $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$)	I _{cc2}	ALL	500	500	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I _{cc3}	-5 -6	170 160	130 120	mA	25
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC} [MIN]$)	I _{cc4}	-5 -6	100 90	100 90	mA	25
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH} : $t_{RC} = t_{RC} [MIN]$)	I _{cc5}	-5 -6	170 160	130 120	mA	22
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I _{cc6}	-5 -6	170 160	130 120	mA	4, 7
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = $t_{RAS} (MIN)$; WE# = $V_{CC} - 0.2V$; A0-A11, OE# and $D_{IN} = V_{CC} - 0.2V$ or 0.2V (D_{IN} may be left open)	I _{cc7}	ALL	400	400	μA	4, 7
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# $\geq t_{RASS} (MIN)$ and CAS# held LOW; WE# = $V_{CC} - 0.2V$; A0-A11, OE# and $D_{IN} =$ $V_{CC} - 0.2V$ or 0.2V (D_{IN} may be left open)	I _{cc8}	ALL	400	400	μA	4, 7

CAPACITANCE

(Note: 2)

PARAMETER	SYMBOL	MAX	UNITS
Input Capacitance: Address pins	C _{I1}	5	pF
Input Capacitance: RAS#, CAS#, WE#, OE#	C _{I2}	7	pF
Input/Output Capacitance: DQ	C _{IO}	7	pF

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t _{AA}		25		30	ns	
Column-address hold time (referenced to RAS#)	t _{AR}	40		45		ns	
Column-address setup time	t _{ASC}	0		0		ns	
Row-address setup time	t _{ASR}	0		0		ns	
Column address to WE# delay time	t _{AWD}	48		55		ns	18
Access time from CAS#	t _{CAC}		13		15	ns	
Column-address hold time	t _{CAH}	8		10		ns	
CAS# pulse width	t _{CAS}	13	10,000	15	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	t _{CHD}	15		15		ns	
CAS# hold time (CBR Refresh)	t _{CHR}	15		15		ns	4
CAS# to output in Low-Z	t _{CLZ}	3		3		ns	
CAS# precharge time (FAST PAGE MODE)	t _{CP}	8		10		ns	13
Access time from CAS# precharge	t _{CPA}		30		35	ns	
CAS# to RAS# precharge time	t _{CRP}	5		5		ns	
CAS# hold time	t _{CSH}	50		60		ns	
CAS# setup time (CBR Refresh)	t _{CSR}	5		5		ns	4
CAS# to WE# delay time	t _{CWD}	36		40		ns	18
WRITE command to CAS# lead time	t _{CWL}	13		15		ns	
Data-in hold time	t _{DH}	8		10		ns	19
Data-in setup time	t _{DS}	0		0		ns	19
Output disable	t _{OD}	3	13	3	15	ns	23, 24
Output enable time	t _{OE}		13		15	ns	20
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t _{OEH}	13		15		ns	24
Output buffer turn-off delay	t _{OFF}	3	13	3	15	ns	17, 23
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t _{ORD}	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t _{PC}	30		35		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t _{PRWC}	76		85		ns	
Access time from RAS#	t _{RAC}		50		60	ns	
RAS# to column-address delay time	t _{RAD}	13		15		ns	15

AC ELECTRICAL CHARACTERISTICS

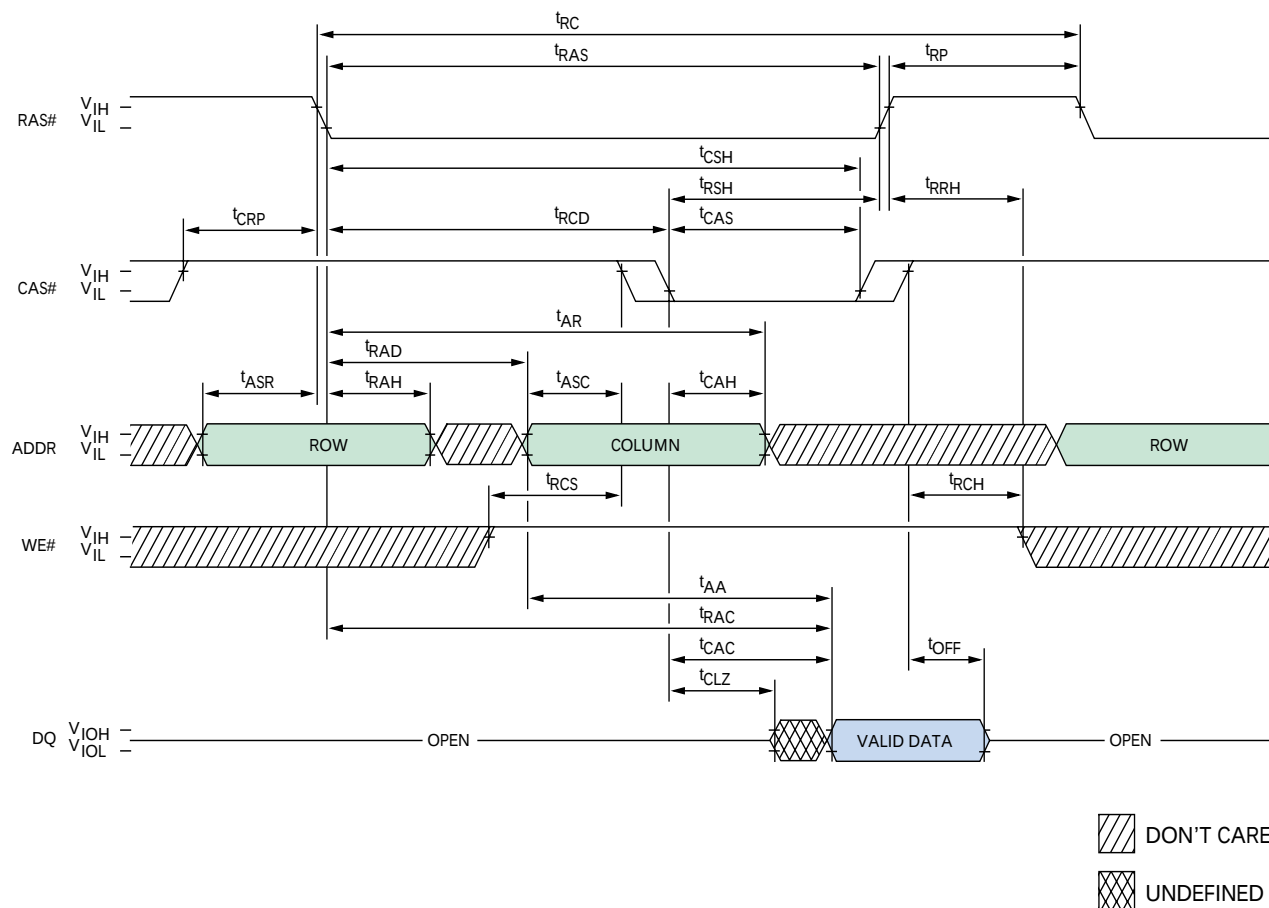
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) ($V_{CC} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Row-address hold time	t_{RAH}	8		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	23
RAS# pulse width during Self Refresh	t_{RASS}	100		100		μs	
Random READ or WRITE cycle time	t_{RC}	90		110		ns	
RAS# to CAS# delay time	t_{RCD}	18		20		ns	14
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	16
READ command setup time	t_{RCS}	0		0		ns	
Refresh period	t_{REF}		64		64	ms	22
Refresh period (4,096 cycles) "S" version	t_{REF}		128		128	ms	4
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	0		0		ns	
RAS# precharge time exiting Self Refresh	t_{RPS}	90		105		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	16
RAS# hold time	t_{RSH}	13		15		ns	
READ-WRITE cycle time	t_{RWC}	131		155		ns	
RAS# to WE# delay time	t_{RWD}	73		85		ns	18
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	40		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	18
WRITE command pulse width	t_{WP}	8		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	10		10		ns	4, 23
WE# setup time (CBR Refresh)	t_{WRP}	10		10		ns	4, 23

NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{CC} = +3.3V$; $f = 1$ MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of 100 μ s is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5$ ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates, 100pF and $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. If CAS# is LOW at the falling edge of RAS#, output data will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} , and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
18. t_{WCS} , t_{RWD} , t_{AWD} , and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. If $t_{WCS} > t_{WCS}(\text{MIN})$, the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. t_{RWD} , t_{AWD} , and t_{CWD} define READ-MODIFY-WRITE cycles. Meeting these limits allows for reading and disabling output data and then applying input data. The values shown were calculated for reference allowing 10ns for the external latching of read data and application of write data. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. RAS#-ONLY REFRESH requires that all 8,192 rows of the MT4LC16M4A7 or all 4,096 rows of the MT4LC16M4T8 be refreshed at least once every 64ms. CBR REFRESH for either device requires that at least 4,096 cycles be completed every 64ms.
23. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If CAS# goes HIGH before OE#, the DQs will open regardless of the state of OE#. If CAS# stays LOW while OE# is brought HIGH, the DQs will open. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If OE# is taken back LOW while CAS# remains LOW, the DQs will remain open.
25. Column address changed once each cycle.
26. V_{IH} overshoot: $V_{IH}(\text{MAX}) = V_{CC} + 2V$ for a pulse width ≤ 10 ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: $V_{IL}(\text{MIN}) = -2V$ for a pulse width ≤ 10 ns, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE

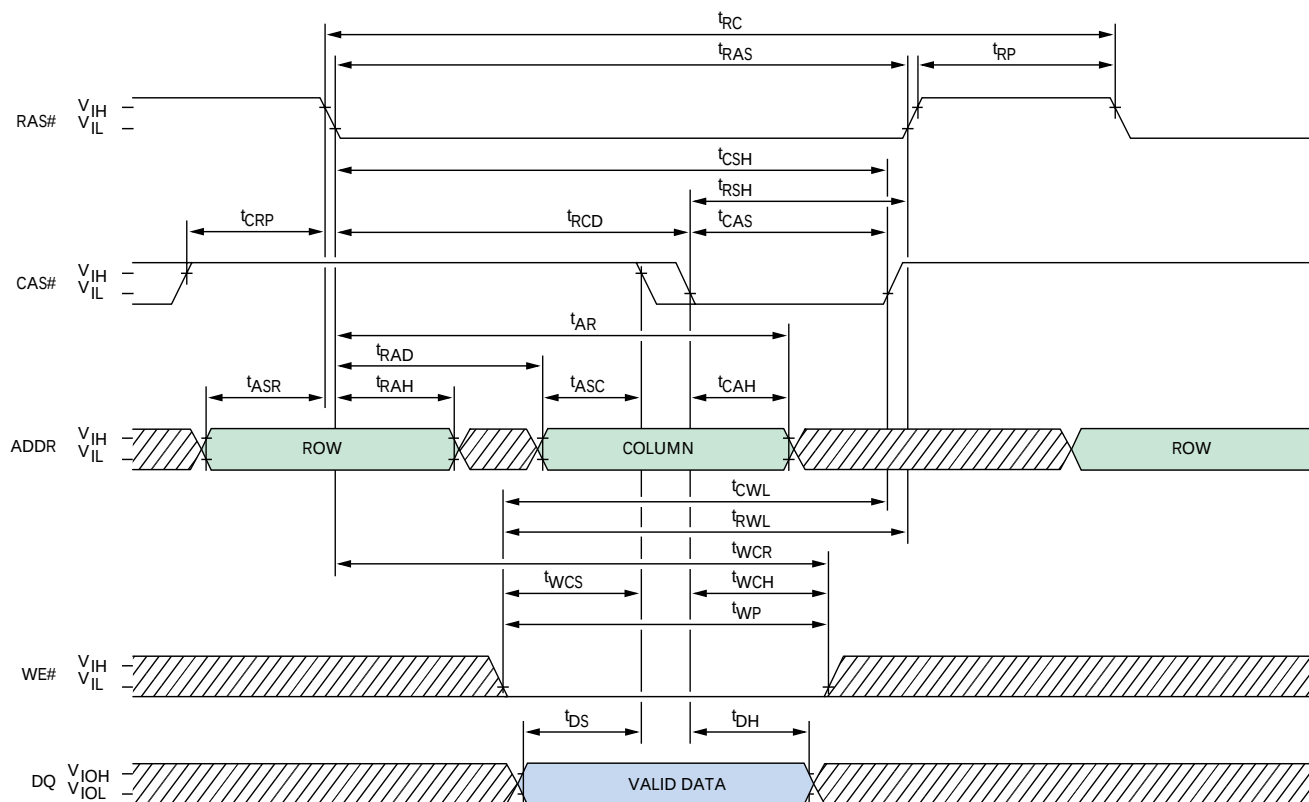


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{AR}	40		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	13	10,000	15	10,000	ns
t_{CLZ}	3		3		ns
t_{CRP}	5		5		ns
t_{CSH}	50		60		ns
t_{OD}	3	13	3	15	ns
t_{OE}		13		15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OFF}	3	13	3	15	ns
t_{RAC}		50		60	ns
t_{RAD}	13		15		ns
t_{RAH}	8		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	90		110		ns
t_{RCD}	18		20		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

EARLY WRITE CYCLE



DON'T CARE

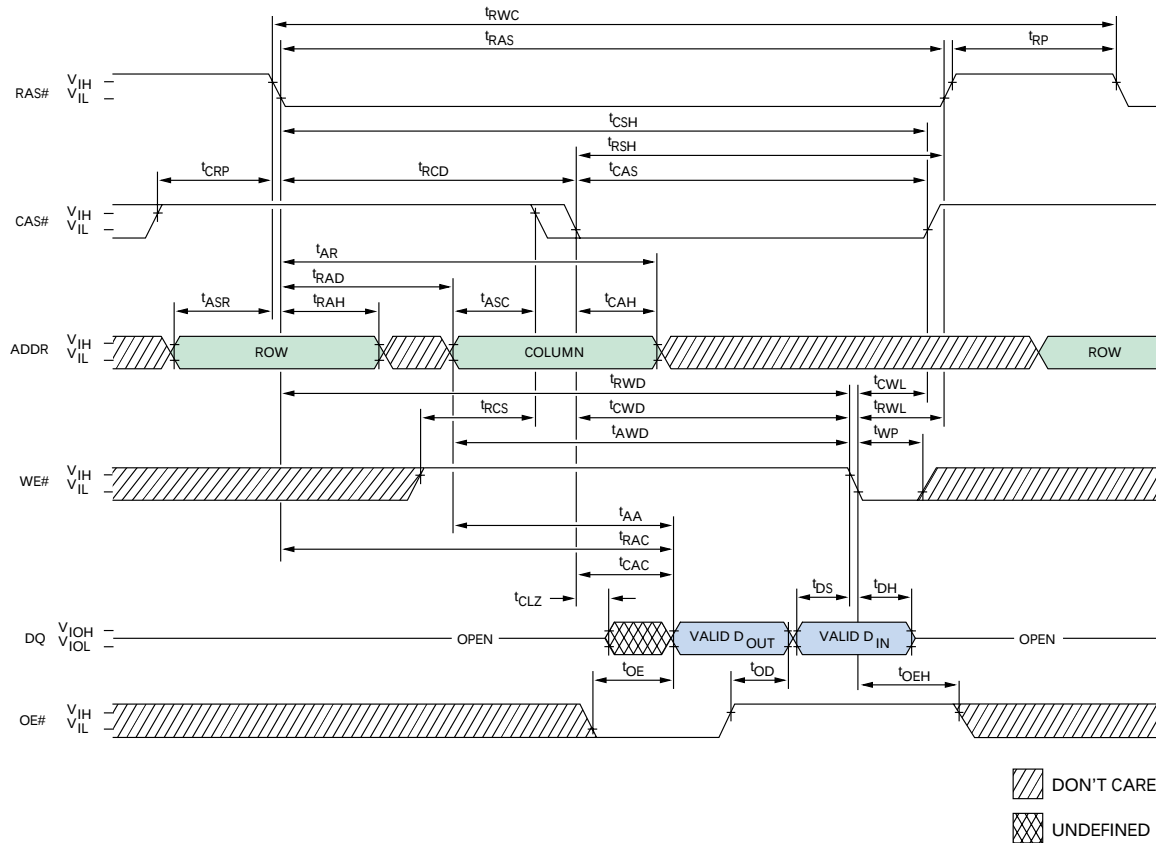
UNDEFINED

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns
tRAD	13		15		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tRAH	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC	90		110		ns
tRCD	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCR	40		45		ns
tWCS	0		0		ns
tWCP	8		10		ns

READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)

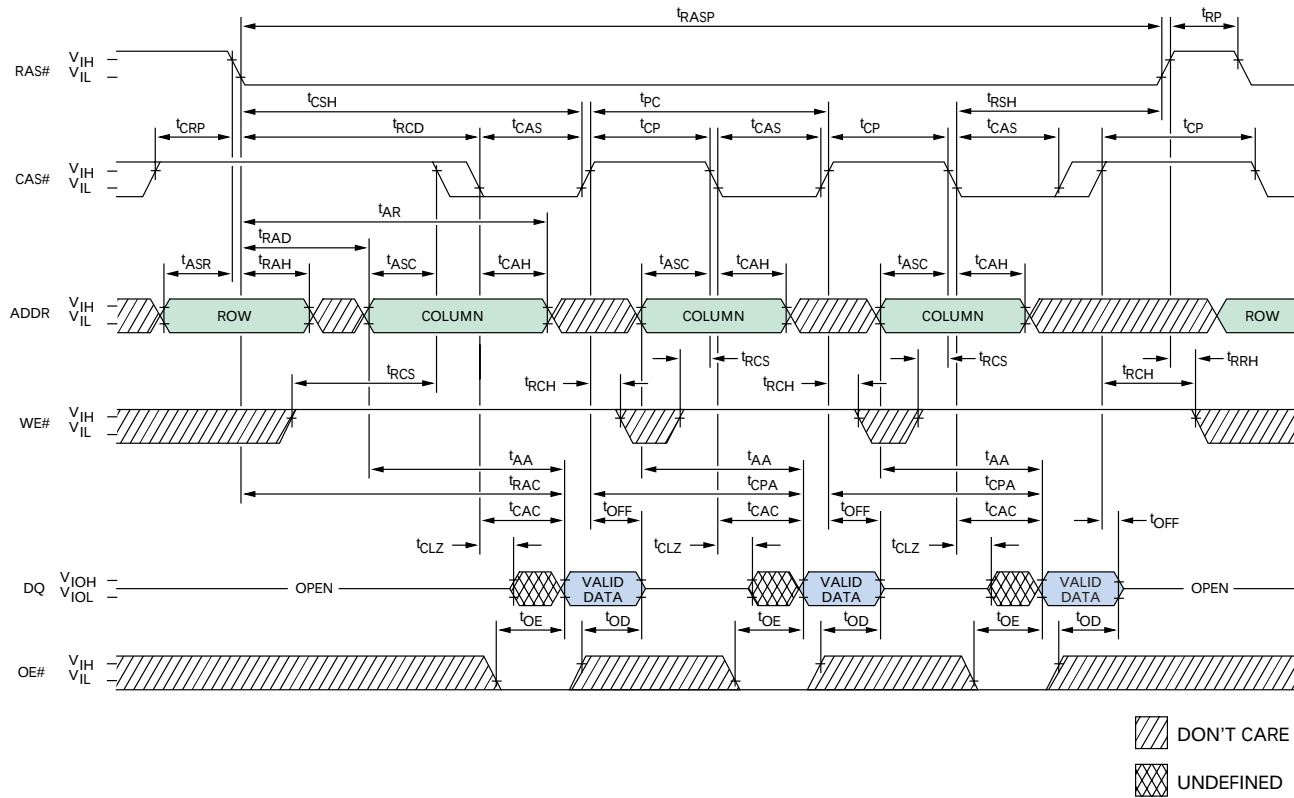


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{AR}	40		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{AWD}	48		55		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	13	10,000	15	10,000	ns
t_{CLZ}	3		3		ns
t_{CRP}	5		5		ns
t_{CSH}	50		60		ns
t_{CWD}	36		40		ns
t_{CWL}	13		15		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OD}	3	13	3	15	ns
t_{OE}		13		15	ns
t_{OEH}	13		15		ns
t_{RAC}		50		60	ns
t_{RAD}	13		15		ns
t_{RAH}	8		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RCD}	18		20		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWC}	131		155		ns
t_{RWD}	73		85		ns
t_{RWL}	13		15		ns
t_{WP}	8		10		ns

FAST-PAGE-MODE READ CYCLE

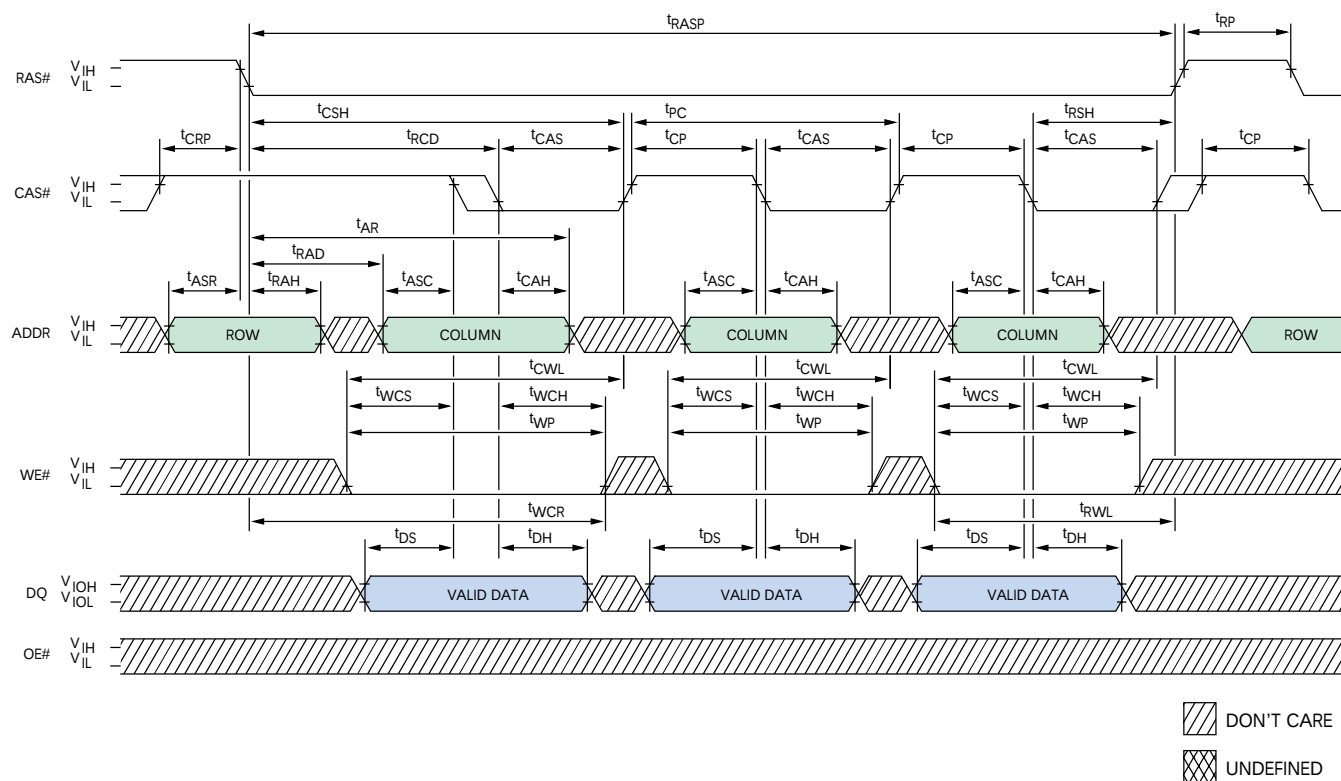


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	40		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CAS}	13	10,000	15	10,000	ns
t _{CLZ}	3		3		ns
t _{CP}	8		10		ns
t _{CPA}		30		35	ns
t _{CRP}	5		5		ns
t _{CSH}	50		60		ns
t _{OD}	3	13	3	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		13		15	ns
t _{OFF}	3	13	3	15	ns
t _{PC}	30		35		ns
t _{RAC}		50		60	ns
t _{RAD}	13		15		ns
t _{RAH}	8		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	18		20		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RRH}	0		0		ns
t _{RSH}	13		15		ns

FAST-PAGE-MODE EARLY WRITE CYCLE



TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AR}	40		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAH}	8		10		ns
t _{CAS}	13	10,000	15	10,000	ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSH}	50		60		ns
t _{CWL}	13		15		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns
t _{PC}	30		35		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RAD}	13		15		ns
t _{RAH}	8		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	18		20		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWL}	13		15		ns
t _{WCH}	8		10		ns
t _{WCR}	40		45		ns
t _{WCS}	0		0		ns
t _{WP}	8		10		ns

The diagram illustrates the timing relationships for a memory device. The signals shown are RAS#, CAS#, ADDR, WE#, DQ, and OE#. The timing parameters are defined as follows:

- t_{RASP} : RAS pulse width
- t_{CRP} : RAS to CAS setup time
- t_{RCD} : RAS to CAS delay
- t_{CAS} : CAS pulse width
- t_{PC} : CAS to RAS setup time
- t_{PRWC} : RAS to CAS setup time
- t_{RSH} : RAS to CAS delay
- t_{CP} : CAS to RAS setup time
- t_{AR} : RAS to CAS delay
- t_{RAD} : RAS to CAS delay
- t_{ASC} : RAS to CAS delay
- t_{CAH} : RAS to CAS delay
- t_{ASR} : RAS to CAS delay
- t_{RAH} : RAS to CAS delay
- t_{RCS} : RAS to CAS delay
- t_{RWD} : RAS to CAS delay
- t_{CWL} : RAS to CAS delay
- t_{WP} : RAS to CAS delay
- t_{AWD} : RAS to CAS delay
- t_{CWD} : RAS to CAS delay
- t_{AA} : RAS to CAS delay
- t_{RAC} : RAS to CAS delay
- t_{DH} : RAS to CAS delay
- t_{DS} : RAS to CAS delay
- t_{CPA} : RAS to CAS delay
- t_{CAC} : RAS to CAS delay
- t_{CLZ} : RAS to CAS delay
- t_{OE} : RAS to CAS delay
- t_{OD} : RAS to CAS delay
- t_{OEh} : RAS to CAS delay
- t_{RP} : RAS pulse width

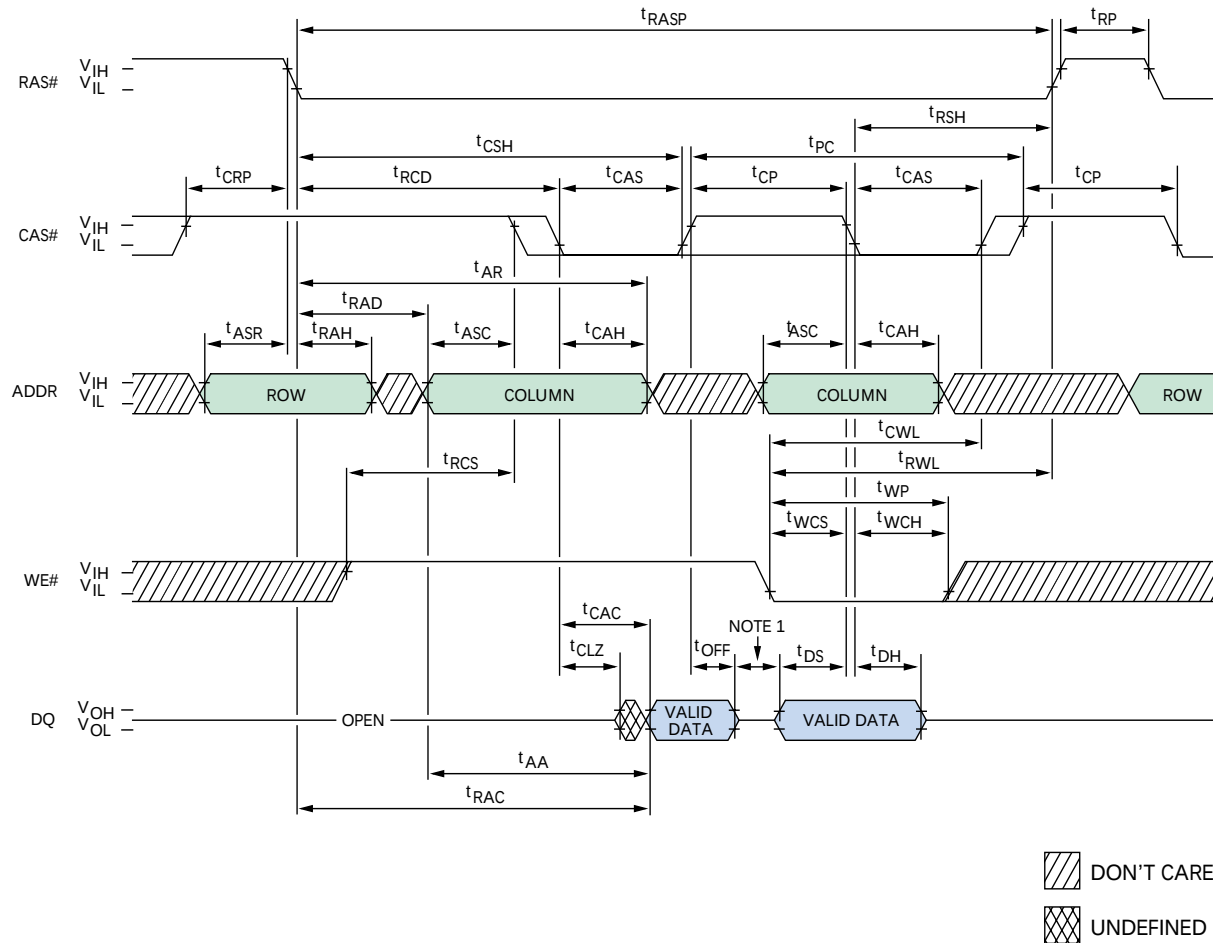
The diagram also includes shaded regions for "DON'T CARE" and "UNDEFINED" states.

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
^t AA		25		30	ns
^t AR	40		45		ns
^t ASC	0		0		ns
^t ASR	0		0		ns
^t AWD	48		55		ns
^t CAC		13		15	ns
^t CAH	8		10		ns
^t CAS	13	10,000	15	10,000	ns
^t CLZ	3		3		ns
^t CP	8		10		ns
^t CPA		30		35	ns
^t CRP	5		5		ns
^t CSH	50		60		ns
^t CWD	36		40		ns
^t CWL	13		15		ns
^t DH	8		10		ns
^t DS	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
^t OD	3	13	3	15	ns
^t OE		13		15	ns
^t OE _H	13		15		ns
^t PC	30		35		ns
^t PRWC	76		85		ns
^t RAC		50		60	ns
^t RAD	13		15		ns
^t RA _H	8		10		ns
^t RASP	50	125,000	60	125,000	ns
^t RCD	18		20		ns
^t RCS	0		0		ns
^t RP	30		40		ns
^t RSH	13		15		ns
^t RWD	73		85		ns
^t RWL	13		15		ns
^t WP	8		10		ns

Micron Technology, Inc., reserves the right to change products or specifications without notice.
©2000, Micron Technology, Inc.

FAST-PAGE-MODE READ EARLY WRITE CYCLE (Pseudo READ-MODIFY-WRITE)



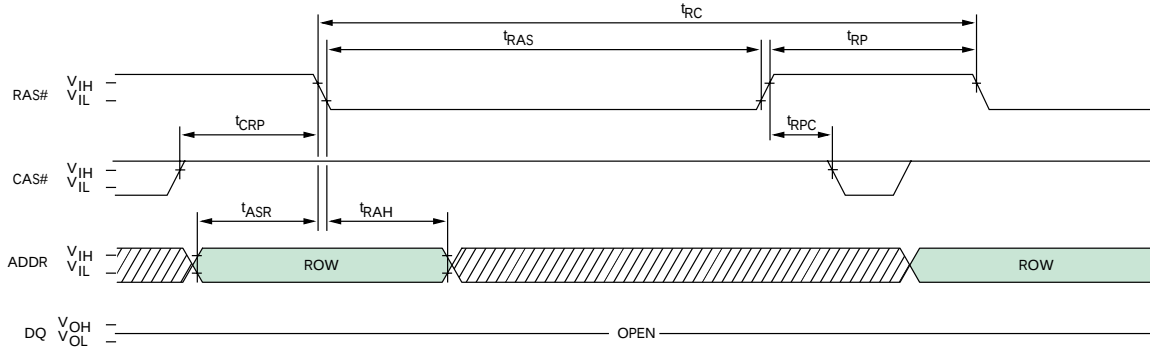
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	40		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CAS}	13	10,000	15	10,000	ns
t _{CLZ}	3		3		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSH}	50		60		ns
t _{CWL}	13		15		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns

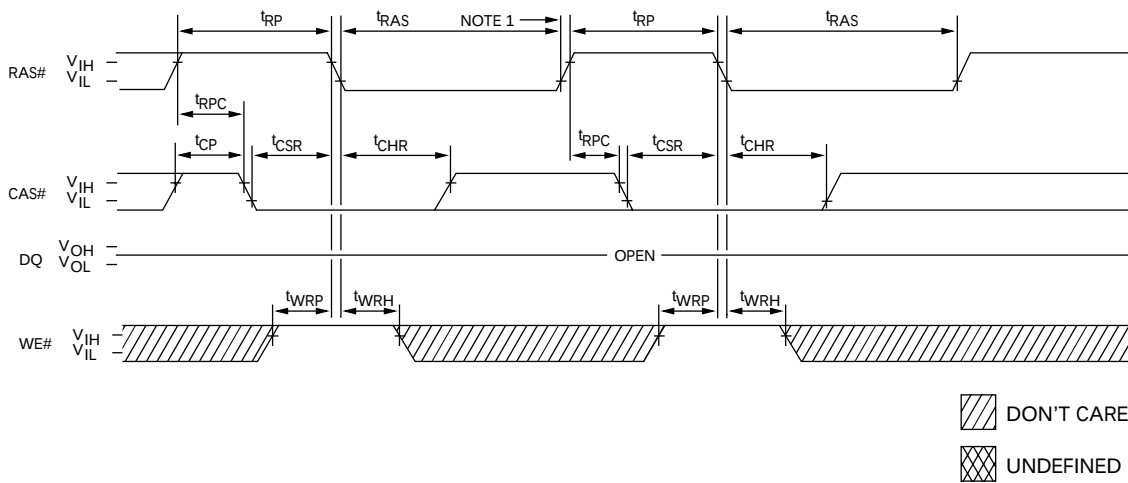
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OFF}	3	13	3	15	ns
t _{PC}	30		35		ns
t _{RAC}		50		60	ns
t _{RAD}	13		15		ns
t _{RAH}	8		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	18		20		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{RWL}	13		15		ns
t _{WCH}	8		10		ns
t _{WCS}	0		0		ns
t _{WP}	8		10		ns

NOTE: 1. Do not drive input data prior to output data going High-Z.

RAS#-ONLY REFRESH CYCLE (OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE (Addresses and OE# = DON'T CARE)



TIMING PARAMETERS

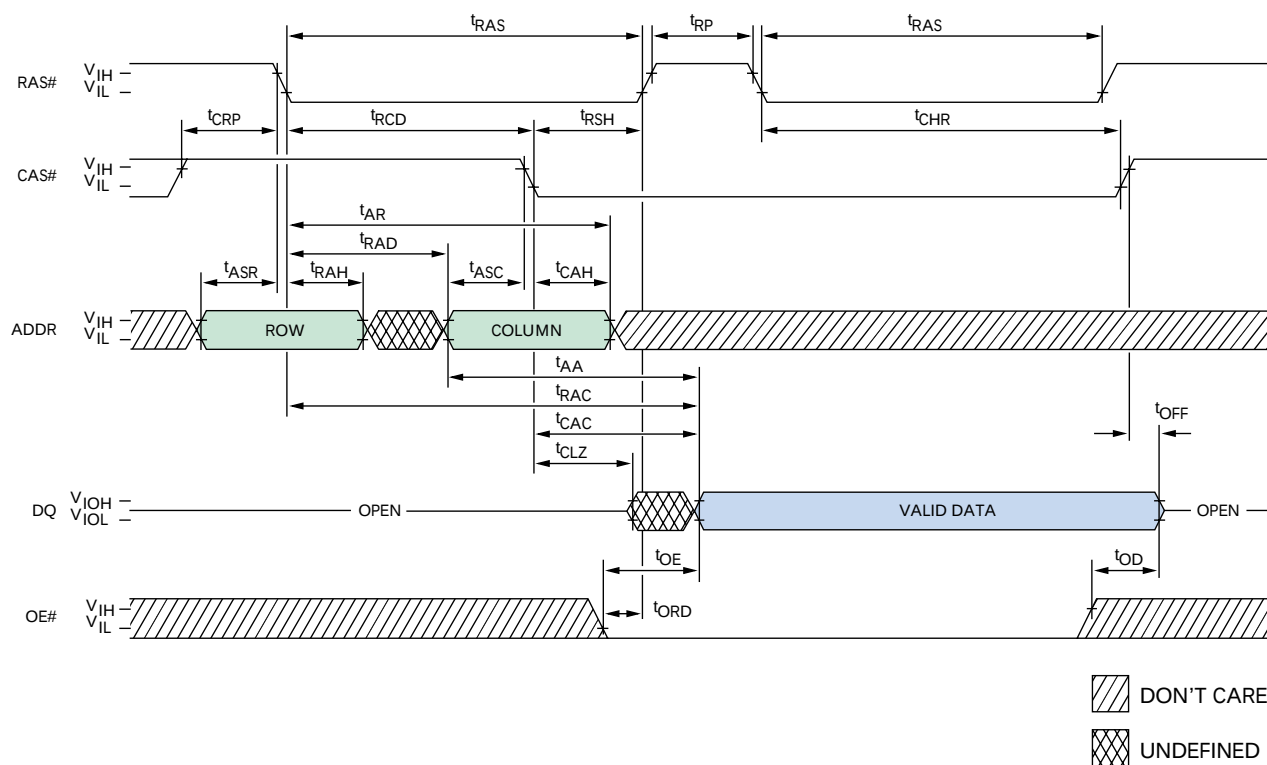
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	0		0		ns
t _{CHR}	15		15		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSR}	5		5		ns
t _{RAH}	8		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RAS}	50	10,000	60	10,000	ns
t _{RC}	90		110		ns
t _{RP}	30		40		ns
t _{RPC}	0		0		ns
t _{WRH}	10		10		ns
t _{WRP}	10		10		ns

NOTE: 1. End of CBR REFRESH cycle.

HIDDEN REFRESH CYCLE ¹

(WE# = HIGH; OE# = LOW)



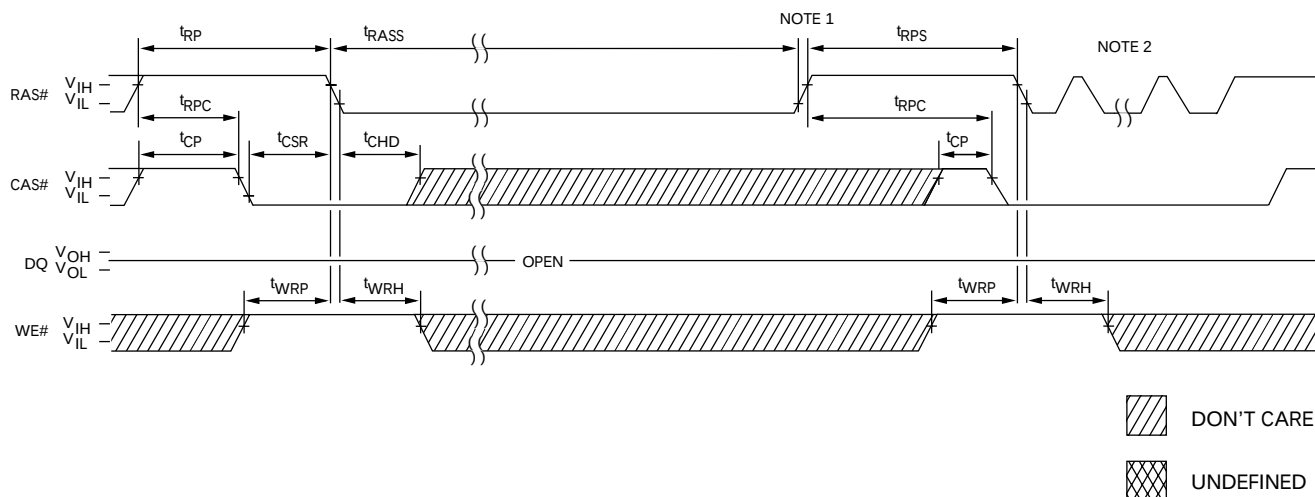
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	40		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CHR}	15		15		ns
t _{CLZ}	3		3		ns
t _{CRP}	5		5		ns
t _{OD}	3	13	3	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		13		15	ns
t _{OFF}	3	13	3	15	ns
t _{ORD}	0		0		ns
t _{RAC}		50		60	ns
t _{RAD}	13		15		ns
t _{RAH}	8		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RCD}	18		20		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns

NOTE: 1. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.

SELF REFRESH CYCLE (Addresses and OE# = DON'T CARE)

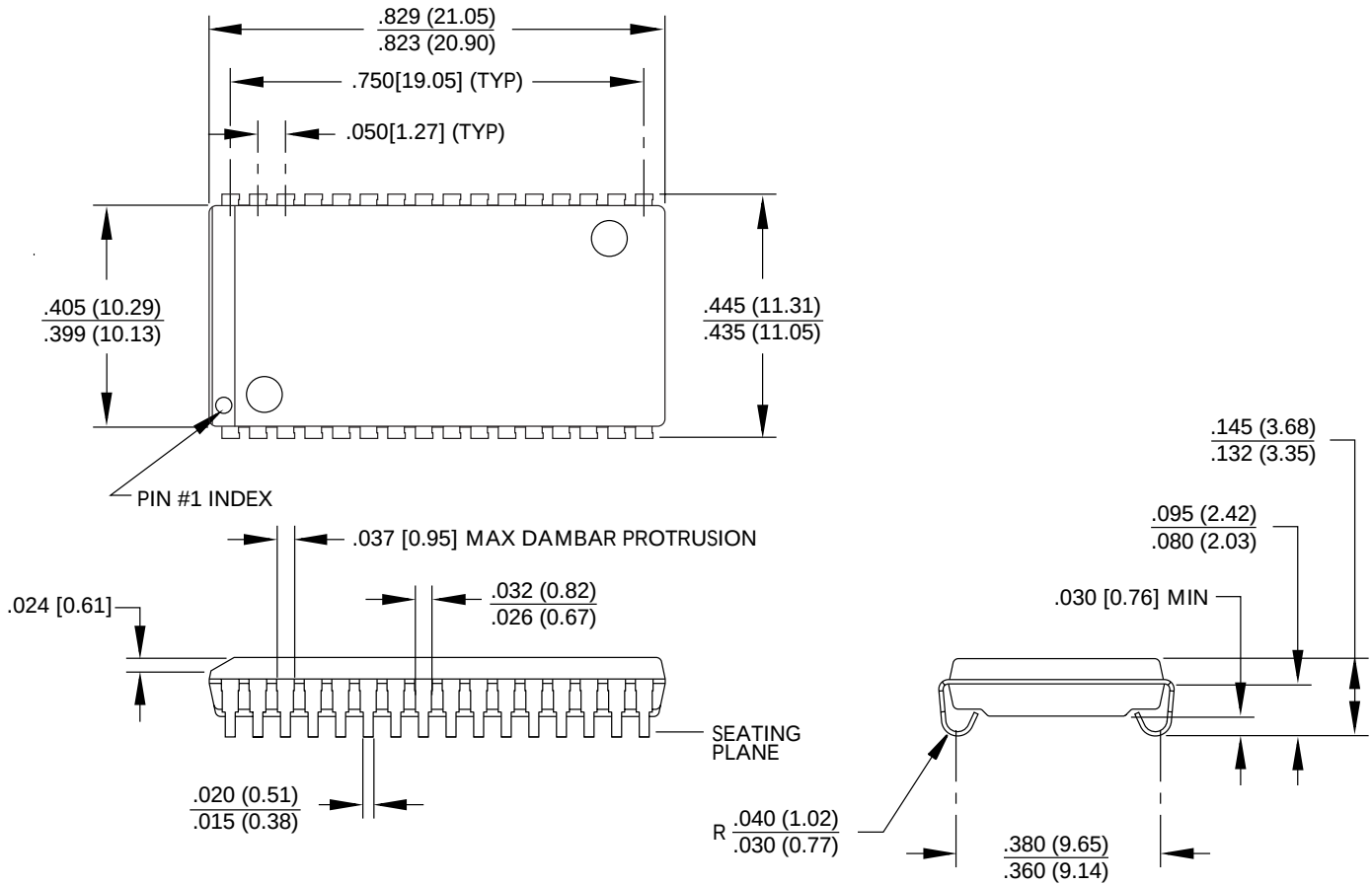


TIMING PARAMETERS

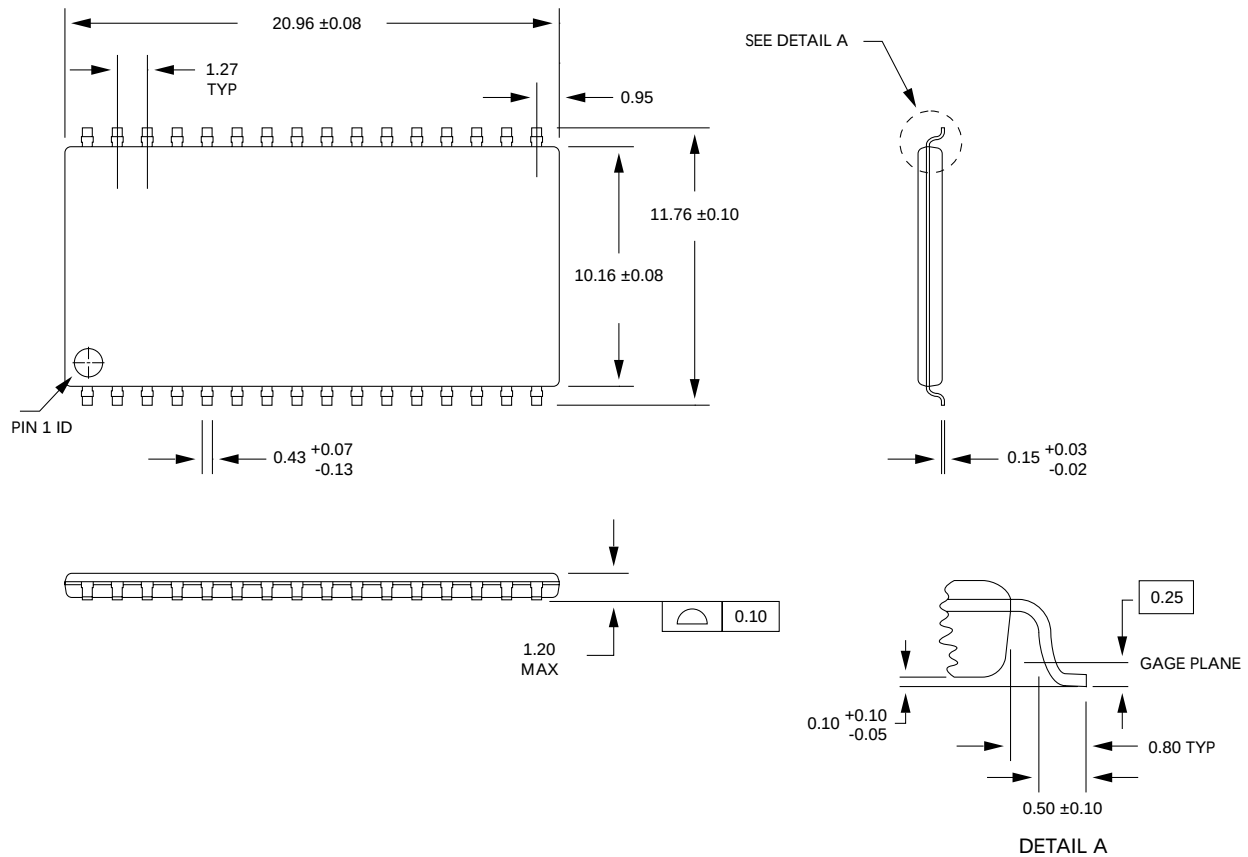
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{CHD}	15		15		ns
t_{CP}	8		10		ns
t_{CSR}	5		5		ns
t_{RAS}	100		100		μ s
t_{RP}	30		40		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RPC}	0		0		ns
t_{RPS}	90		105		ns
t_{WRH}	10		10		ns
t_{WRP}	10		10		ns

NOTE: 1. Once t_{RAS} (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
 2. Once t_{RPS} is satisfied, a complete burst of all rows should be executed, if RAS#-only or burst CBR refresh is used.

32-PIN PLASTIC SOJ (400 mil)


- NOTE:** 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

32-PIN PLASTIC TSOP (400 mil)


- NOTE:** 1. All dimensions in millimeters $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is .25mm per side.



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

E-mail: prodmtg@micron.com, Internet: <http://www.micron.com>, Customer Comment Line: 800-932-4992

Micron is a registered trademark of Micron Technology, Inc.