1M x 1 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-92316
- MIL-STD-883

FEATURES

- High Speed: 20, 25, 35, and 45
- Battery Backup: 2V data retention
- Low power standby
- Single +5V (±10%) Power Supply
- Easy memory expansion with CE\ and OE\ options.
- All inputs and outputs are TTL compatible
- Three-state output

OPTIONS MARKING

- **Timing**

20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*

- **Package(s)**

Ceramic DIP (400 mil)	C	No. 109
Ceramic LCC	EC	No. 207
Ceramic Flatpack	F	No. 303
Ceramic SOJ	DCJ	No. 501

- **Operating Temperature Ranges**

Industrial (-40°C to +85°C)	IT
Military (-55°C to +125°C)	XT

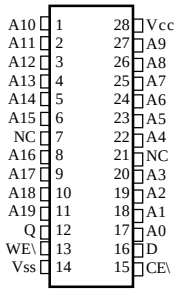
- 2V data retention/low power L

*Electrical characteristics identical to those provided for the 45ns access devices.

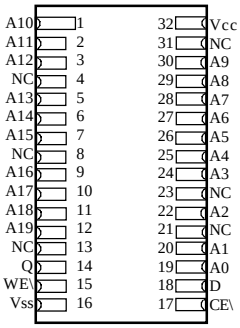
For more products and information please visit our web site at *www.austinsemiconductor.com*

PIN ASSIGNMENT
(Top View)

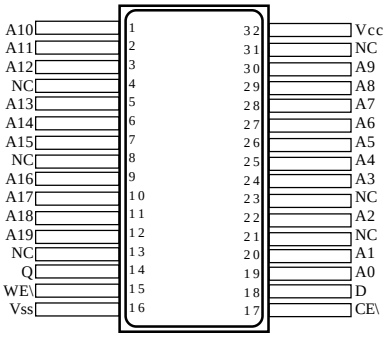
28-Pin DIP (C)
(400 MIL)



32-Pin LCC (EC)
32-Pin SOJ (DCJ)



32-Pin Flat Pack (F)



GENERAL DESCRIPTION

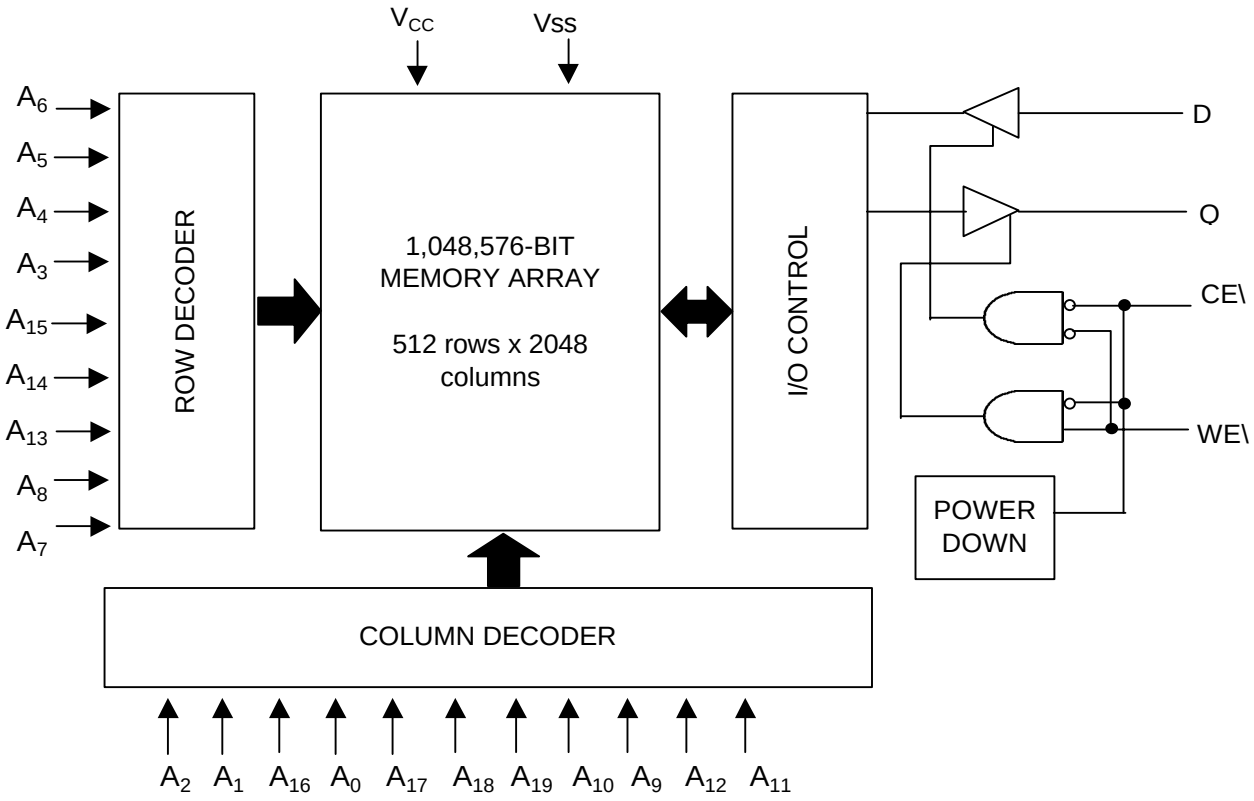
The MT5C1001 employs low power, high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes while CMOS circuitry reduces power consumption and provides for greater reliability.

For flexibility in high-speed memory applications, ASI offers chip enable (CE\) and output enable (OE\) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design. Writing to these devices is accomplished when write enable (WE|) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH while CE\ and OE\ go LOW. The devices offer a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

The "L" version provides an approximate 50 percent reduction in CMOS standby current (I_{SBC2}) over the standard version.

All devices operation from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE\	WE\	OUTPUT	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

PIN ASSIGNMENTS

PIN	ASSIGNMENT
A_0-A_{19}	Address Inputs
WE\	Write Enable
CE\	Chip Enable
D	Data Input
Q	Data Output
NC	No Connection
V_{CC}	+5V Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Input Relative to Vss.....-.5V to +7V
Voltage on Vcc Supply Relative to Vss.....-.5V to +7V
Voltage Applied to Q.....-.5V to +6V
Storage Temperature.....-65°C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....20mA
Lead Temperature (soldering 10 seconds).....+260°C
Junction Temperature.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \leq T_C \leq 125°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	VCC+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq VCC$	IL_I	-5	5	µA	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq VCC$	IL_O	-5	5	µA	
Output High Voltage	$I_{OH} = -4.0mA$	V_{OH}	2.4		V	1
Output Low Voltage	$I_{OL} = 8.0mA$	V_{OL}		0.4	V	1

			MAX					
PARAMETER	CONDITIONS	SYM	-20	-25	-35	-45	UNITS	NOTES
Power Supply Current: Operating	$CE\backslash \leq V_{IL}$; V_{CC} = MAX f = MAX = $1/t_{RC}$ (MIN) Output Open	I_{CC}	125	120	115	110	mA	3
Power Supply Current: Standby	$CE\backslash \geq V_{IH}$; V_{CC} = MAX f = MAX = $1/t_{RC}$ (MIN) Output Open	I_{SBT1}	50	45	40	35	mA	
	$CE\backslash \geq V_{IH}$; All Other Inputs $\leq V_{IH}$ or $\geq V_{IH}$, V_{CC} = MAX f = 0 Hz	I_{SBT2}	25	25	25	25	mA	
	$CE\backslash \geq V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \leq V_{SS}$ +0.2V $V_{IH} \geq V_{CC}$ -0.2V; f = 0 Hz	I_{SBC2}	10	10	10	10	mA	
	"L" Version Only	I_{SBC2}	5	5	5	5	mA	

CAPACITANCE

PARAMETER	CONDITIONS	SYMBOL	MAXIMUM	UNITS	NOTES
Input Capacitance (A3-A5, A15 -A17)	$T_A = 25°C$, f = 1MHz V_{CC} = 5V	C_I	10	pF	4
Output Capactiance (Q)		Co	8	pF	4
Input Capacitance: (All Other Inputs)		C_I	8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{o}C \leq T_C \leq 125^{o}C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	-20		-25		-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE											
READ cycle time	t_{RC}	20		25		35		45		ns	
Address access time	t_{AA}		20		25		35		45	ns	
Chip Enable access time	t_{ACE}		20		25		35		45	ns	
Output hold from address change	t_{OH}	3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		ns	4, 6, 7
Chip disable to output in High-Z	t_{HZCE}		8		10		15		15	ns	4, 6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		20		25		35		45	ns	4
WRITE CYCLE											
WRITE cycle time	t_{WC}	20		25		35		45		ns	
Chip Enable to end of write	t_{CW}	15		16		20		25		ns	
Address valid to end of write	t_{AW}	15		16		20		25		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	1		1		1		1		ns	
WRITE pulse width	t_{WP}	15		16		20		25		ns	
Data setup time	t_{DS}	8		10		13		15		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	3		3		3		3		ns	7
Write Enable to output in High-Z	t_{HZWE}	0	9	0	10	0	13	0	13	ns	4, 6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

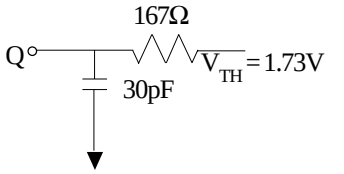


Fig. 1 Output Load Equivalent

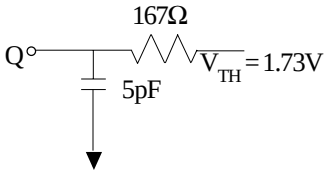


Fig. 2 Output Load Equivalent

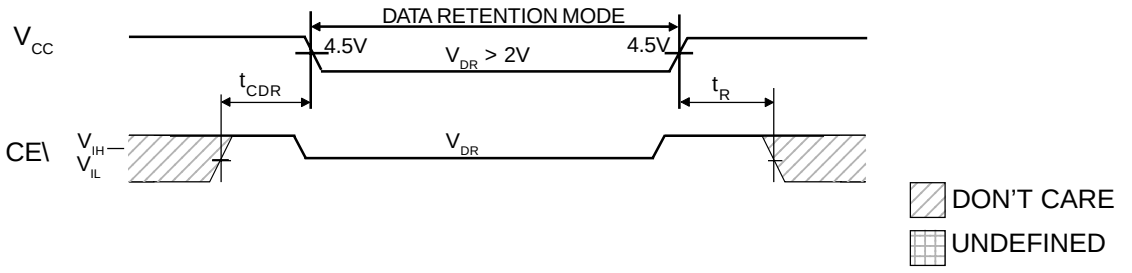
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and f = 1 / t_{RC} (MIN) Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{LZCE}, t_{LZWE}, t_{LOE}, t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} and t_{HZOE} is less than t_{LZOE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

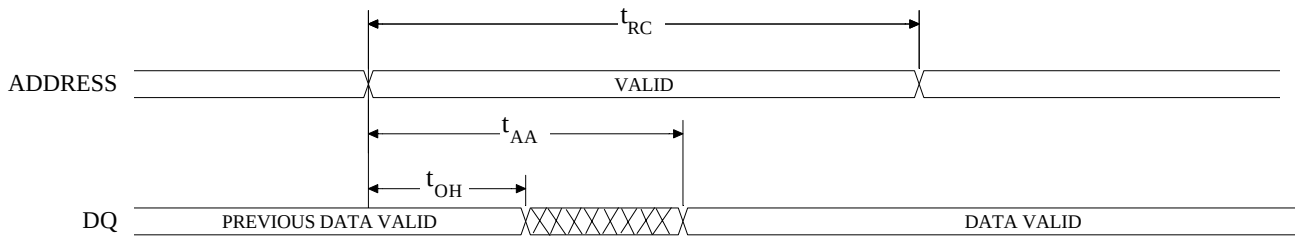
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2	--	V	
Data Retention Current	CE\ ≥ (V_{CC} - 0.2V) and V_{IN} > (V_{CC} - 0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		1.0	mA	
		V_{CC} = 3V			1.5	mA	
Chip Deselect to Data Retention Time			t_{CDR}	0	--	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

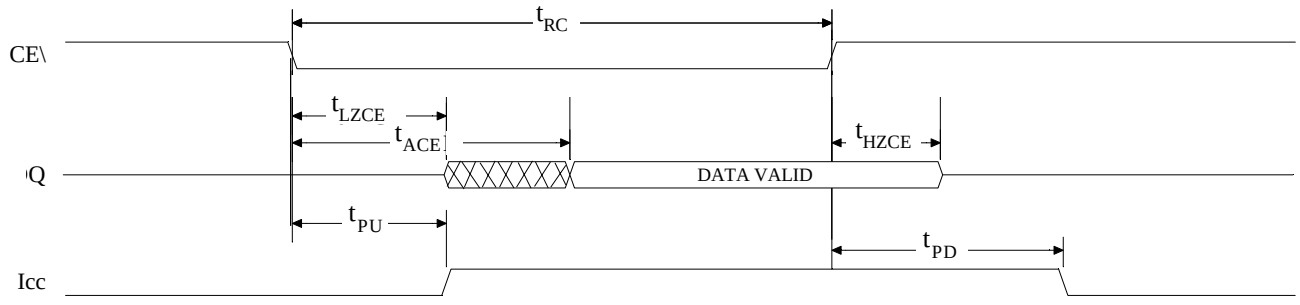
LOW Vcc DATA RETENTION WAVEFORM



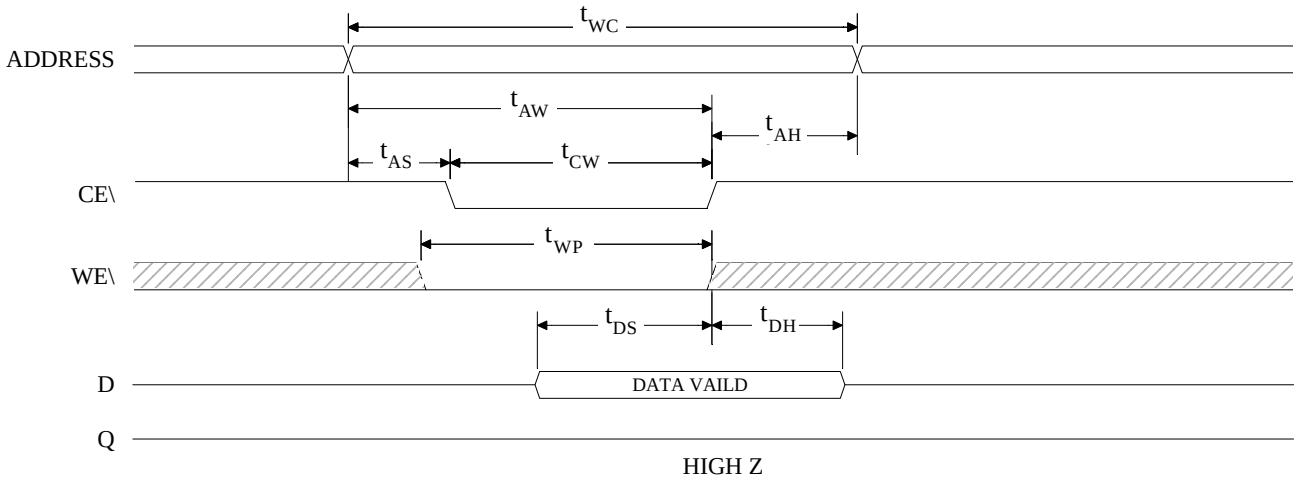
READ CYCLE NO. 1 [8, 9]



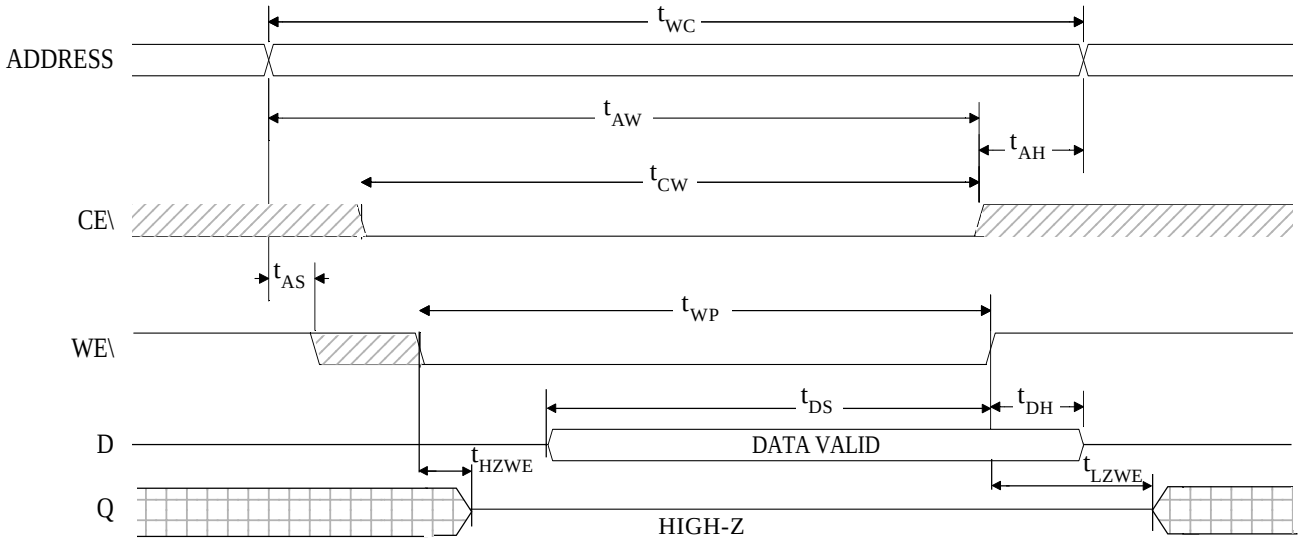
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enabled Controlled)



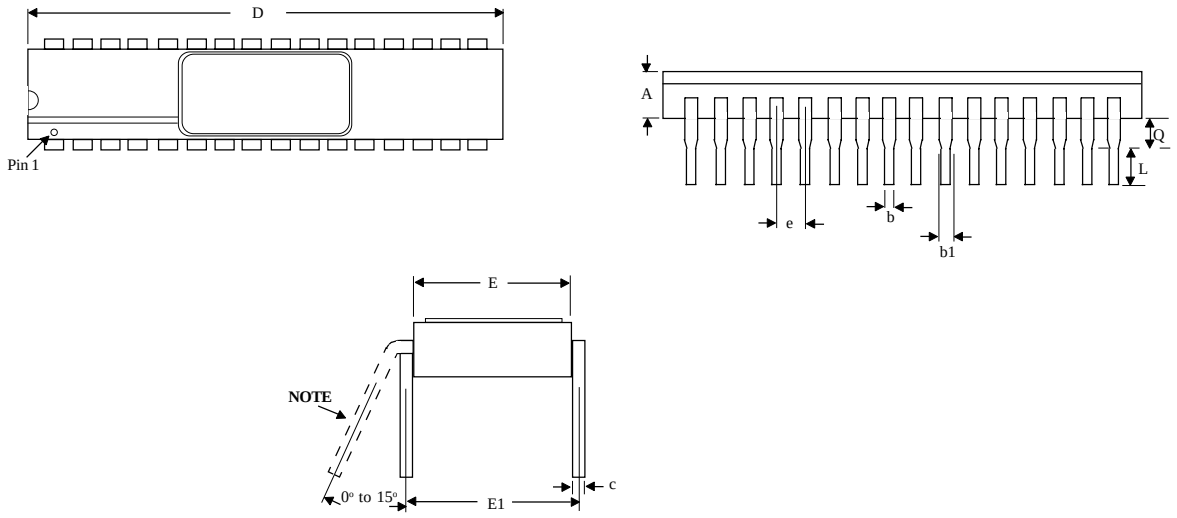
DON'T CARE

UNDEFINED

NOTE: Output enable (OE\) is inactive (HIGH).

MECHANICAL DEFINITIONS*

ASI Case #109 (Package Designator C)
SMD #5962-92316, Case Outline T



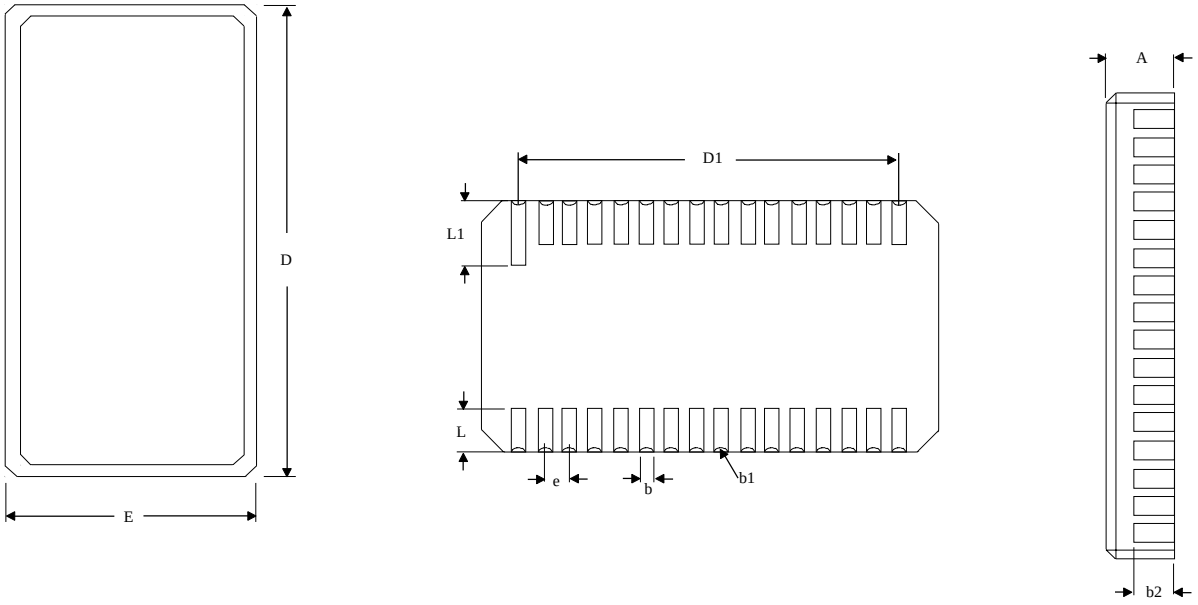
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.075	0.095
b	0.016	0.020
b1	0.040	0.060
c	0.008	0.012
D	1.386	1.414
E	0.385	0.405
E1	0.390	0.410
e	0.100 BSC	
L	0.125	0.175
Q	0.040	0.060

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #207 (Package Designator EC)
SMD# 5962-92316, Case Outline Y



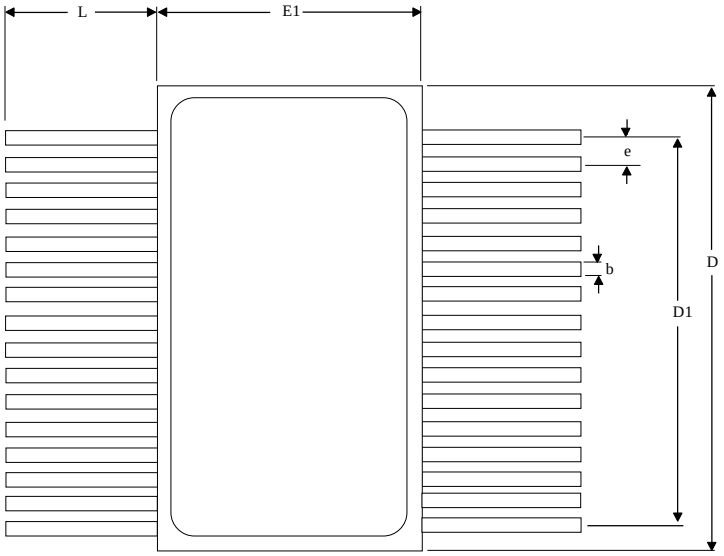
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.080	0.100
b	0.022	0.028
b1	0.004	0.014
b2	0.054	0.066
D	0.815	0.835
D1	0.740	0.760
E	0.392	0.408
e	0.050 BSC	
L	0.070	0.080
L1	0.090	0.110

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

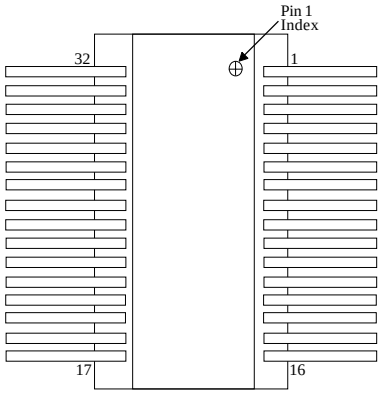
All measurements are in inches.

MECHANICAL DEFINITIONS*

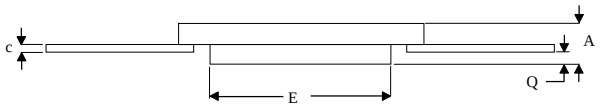
ASI Case #303 (Package Designator F)
SMD #5962-92316, Case Outline Z



Top View



Bottom View



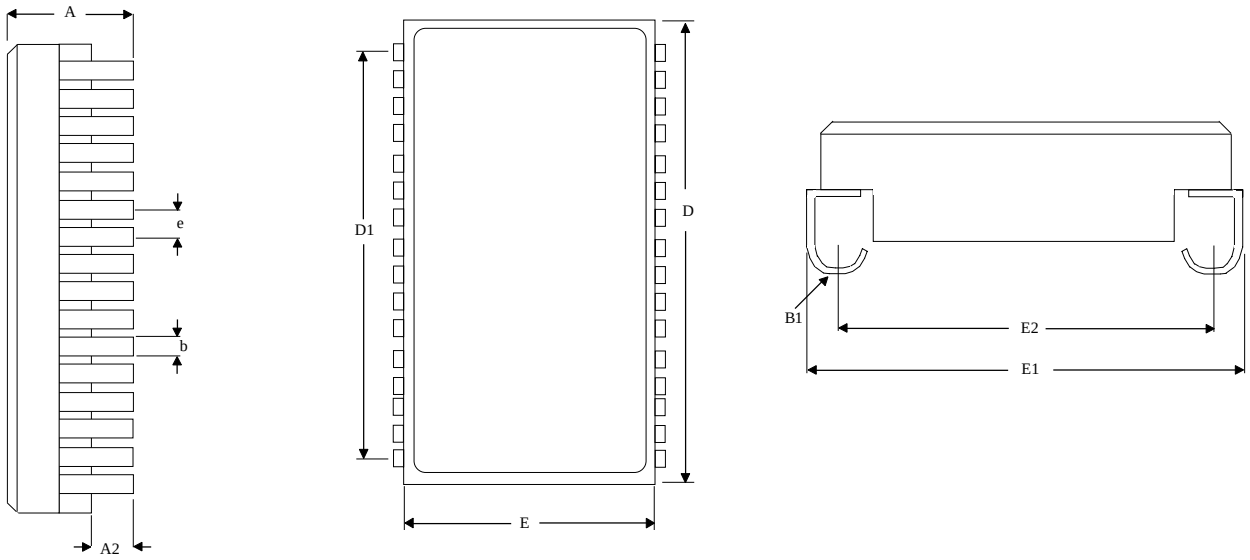
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.097	0.117
b	0.015	0.019
c	0.004	0.006
D	0.812	0.828
D1	0.745	0.755
E	0.324	0.336
E1	0.405	0.415
e	0.050 BSC	
L	0.290	0.310
Q	0.032	0.038

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #501 (Package Designator DCJ)
SMD #5962-92316, Case Outline U



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.135	0.153
A2	0.026	0.036
B1	0.030	0.040
b	0.015	0.019
D	0.812	0.828
D1	0.745	0.760
E	0.405	0.415
E1	0.435	0.445
E2	0.360	0.380
e	0.050 BSC	

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: MT5C1001C-20L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1001	C	-20	L	/*
MT5C1001	C	-25	L	/*
MT5C1001	C	-35	L	/*
MT5C1001	C	-40	L	/*
MT5C1001	C	-55	L	/*
MT5C1001	C	-70	L	/*

EXAMPLE: MT5C1001EC-45/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1001	EC	-20	L	/*
MT5C1001	EC	-25	L	/*
MT5C1001	EC	-35	L	/*
MT5C1001	EC	-40	L	/*
MT5C1001	EC	-55	L	/*
MT5C1001	EC	-70	L	/*

EXAMPLE: MT5C1001F-25L/883C

Device Number	Package Type	Speed ns	Options**	Process
MT5C1001	F	-20	L	/*
MT5C1001	F	-25	L	/*
MT5C1001	F	-35	L	/*
MT5C1001	F	-40	L	/*
MT5C1001	F	-55	L	/*
MT5C1001	F	-70	L	/*

EXAMPLE: MT5C1001DCJ-70/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C1001	DCJ	-20	L	/*
MT5C1001	DCJ	-25	L	/*
MT5C1001	DCJ	-35	L	/*
MT5C1001	DCJ	-40	L	/*
MT5C1001	DCJ	-55	L	/*
MT5C1001	DCJ	-70	L	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

**** OPTIONS**

L = 2V Data Retention/Low Power

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator C

ASI Part #	SMD Part #
MT5C1001C-20L/883C	5962-9231608MTA
MT5C1001C-20/883C	5962-9231604MTA
MT5C1001C-25L/883C	5962-9231607MTA
MT5C1001C-25/883C	5962-9231603MTA
MT5C1001C-35L/883C	5962-9231606MTA
MT5C1001C-35/883C	5962-9231602MTA
MT5C1001C-45L/883C	5962-9231605MTA
MT5C1001C-45/883C	5962-9231601MTA

ASI Package Designator EC

ASI Part #	SMD Part #
MT5C1001EC-20L/883C	5962-9231608MYA
MT5C1001EC-20/883C	5962-9231604MYA
MT5C1001EC-25L/883C	5962-9231607MYA
MT5C1001EC-25/883C	5962-9231603MYA
MT5C1001EC-35L/883C	5962-9231606MYA
MT5C1001EC-35/883C	5962-9231602MYA
MT5C1001EC-45L/883C	5962-9231605MYA
MT5C1001EC-45/883C	5962-9231601MYA

ASI Package Designator F

ASI Part #	SMD Part #
MT5C1001F-20L/883C	5962-9231608MZA
MT5C1001F-20/883C	5962-9231604MZA
MT5C1001F-25L/883C	5962-9231607MZA
MT5C1001F-25/883C	5962-9231603MZA
MT5C1001F-35L/883C	5962-9231606MZA
MT5C1001F-35/883C	5962-9231602MZA
MT5C1001F-45L/883C	5962-9231605MZA
MT5C1001F-45/883C	5962-9231601MZA

ASI Package Designator DCJ

ASI Part #	SMD Part #
MT5C1001DCJ-20L/883C	5962-9231608MUA
MT5C1001DCJ-20/883C	5962-9231604MUA
MT5C1001DCJ-25L/883C	5962-9231607MUA
MT5C1001DCJ-25/883C	5962-9231603MUA
MT5C1001DCJ-35L/883C	5962-9231606MUA
MT5C1001DCJ-35/883C	5962-9231602MUA
MT5C1001DCJ-45L/883C	5962-9231605MUA
MT5C1001DCJ-45/883C	5962-9231601MUA

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*