CMOS **MT90732**

E2/E3 Framer (E2/E3F)

Advance Information

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Features

- Framer for CCITT Recommendations
  - G.742 (8448 kbit/s)
  - G.745 (8448 kbit/s)
  - G.751 (34368 kbit/s)
  - G.753 (34368 kbit/s)
- Line side interface
  - Dual rail or NRZ
- HDB3 codec for dual rail I/O
- Terminal side interface
  - Nibble-parallel
  - Bit-serial
- Transmit reference generator for bit-serial I/O
- Microprocessor or control leads
- I/O port for service bits

Applications

- Line terminals
- Wideband data or video transport
- Test equipment
- Multiplexer systems

Ordering Information

MT90732AP 68 Pin PLCC

-40°C to +85°C

Description

The MT90732 E2/E3 Framer (E2/E3F) is a CMOS VLSI device that provides the functions needed to frame a wideband payload to one of four CCITT Recommendations. G.742, G.745, G.751, or G.753. The E2/E3 Framer interfaces to line circuitry with either dual rail or NRZ signals. On the terminal side, the interface can be either nibble-parallel or bit-serial.

The MT90732 can be operated with or without a microprocessor. When interfaced with a microprocessor, the E2/E3 Framer provides an 8-byte memory map for control, performance counters and alarm status. The MT90732 provides a transmit and receive interface port for accessing the overhead bits from each of the four recommendations. The overhead bits can also be accessed by the microprocessor via the memory map.

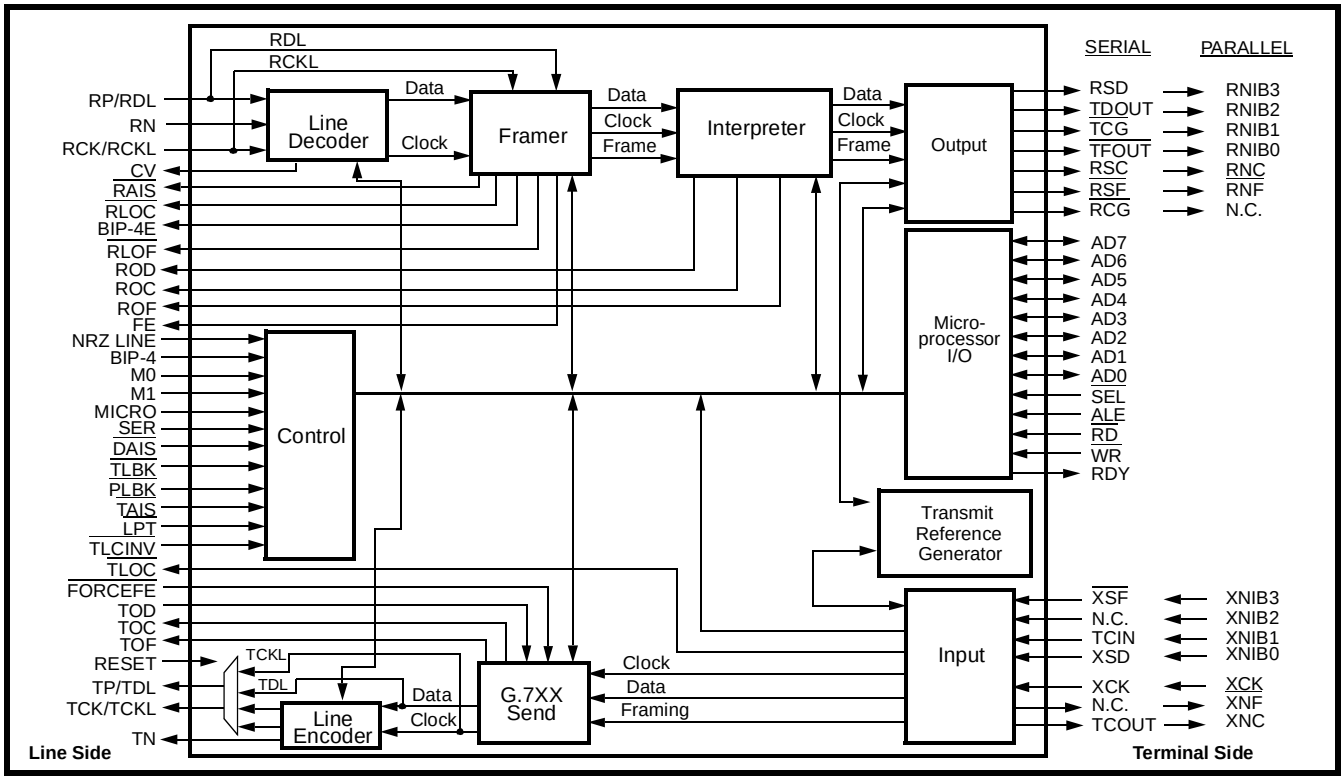

Figure 1 - Functional Block Diagram

U.S. Patent Number 5040170

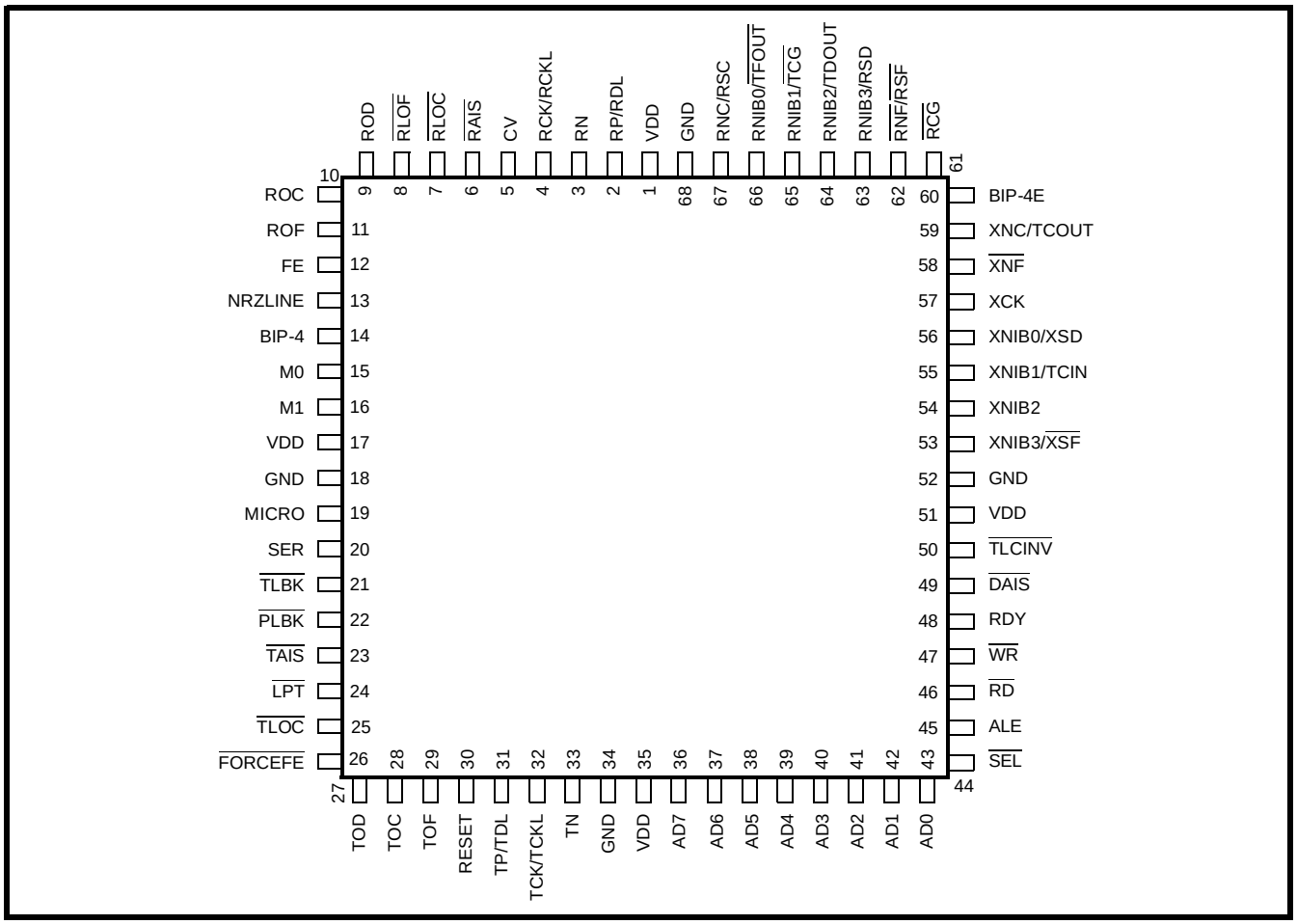

Figure 2 - Pin Connections

Pin Description

Power Supply and Ground

Pin #	Name	I/O/P	Description
1,17,35,51	VDD	P	**VDD.** 5-volt supply voltage, +/- 5%
18,34,52,68	GND	P	**Ground.**

Note: I = Input; O = Output; P = Power

Line Side Receive

Pin #	Name	I/O/P	Description
2	RP/RDL	I	**Receive Positive Rail/Receive NRZ Data.** Receive positive rail/NRZ data generated from line interface circuit.
3	RN	I	**Receive Negative Rail Data.** Receive negative rail data generated from line interface circuit.
4	RCK/RCKL	I	**Receive Clock Rail/Receive Clock NRZ.** The receive clock is used for clocking in the rail/NRZ data signals.

Note: I = Input; O = Output; P = Power

Line Side Transmit

Pin #	Name	I/O/P	Description
31	TP/TDL	O	**Transmit Positive Rail/Transmit NRZ Data.** Transmit positive rail/NRZ data sent out of E2/E3 Framer.
32	TCK/TCKL	O	**Transmit Clock Rail/Transmit Clock NRZ.** The transmit clock is used for clocking out the dual rail/NRZ data signals. The TCK/TCKL clock signal is derived from the XCK clock.
33	TN	O	**Transmit Negative Rail Data.** Transmit negative rail data sent out of E2/E3 Framer.

Note: I = Input; O = Output; P = Power

Terminal Interface

Pin #	Name	I/O/P	Description
61	$\overline{\text{RCG}}$	O	**Receive Clock Gapped.** An active low signal indicates the receive framing and service bit locations in the serial mode only.
62	$\overline{\text{RNF}}$/$\overline{\text{RSF}}$	O	**Receive Framing Pulse.** Framing pulse is synchronous with the last nibble for the nibble-parallel interface, and with the first bit in the frame for the bit-serial interface.
63	RNIB3/RSD	O	**Receive Nibble Bit 3/Receive Serial Data.** Bit 3 is the most significant bit in the nibble and corresponds to the first bit received in the nibble. The framing pattern, service bits, and BIP-4 nibble are not provided as parallel data. In the serial mode receive data signal consists of all bits, including the framing pattern and service bits.
64	RNIB2/TDOUT	O	**Receive Nibble Bit 2/Transmit Reference Generator Data Output.** In the nibble-parallel mode, it is Bit 2 of the received nibble.The reference generator is enabled in the serial mode. The output data signal (TDOUT) consists of all ones in place of the framing bits and zeros elsewhere in the frame.
65	RNIB1/$\overline{\text{TCG}}$	O	**Receive Nibble Bit 1/Transmit Reference Generator Clock Gap Signal.** In the nibble-parallel mode, it is Bit 1 of the received nibble. The active low $\overline{\text{TCG}}$ signal indicates the location of the framing pattern and the service bits in the frame.
66	RNIB0/$\overline{\text{TFOUT}}$	O	**Receive Nibble Bit 0/Transmit Reference Generator Framing Pulse.** Bit 0 is the least significant bit in the nibble and is the last bit received. The active low $\overline{\text{TFOUT}}$ signal is synchronous with the first bit in the frame.
67	RNC/RSC	O	**Receive Nibble Clock/Receive Serial Clock.** The nibble and serial clocks are derived from the line side dual rail/NRZ clock signal (RCK/RCKL). RNC is gapped during framing pattern, service bit and BIP-4 bit times.
53	XNIB3/$\overline{\text{XSF}}$	I	**Transmit Nibble Bit 3/Transmit Serial Framing Pulse.** In the nibble-parallel mode, bit 3 is the most significant bit in the nibble and corresponds to the first bit transmitted in the nibble. When the terminal interface is serial, the negative framing pulse is synchronous with the first bit in the frame.
54	XNIB2	I	**Transmit Nibble Bit 2.** Bit 2 in the 4-bit nibble.
55	XNIB1/TCIN	I	**Transmit Nibble Bit 1/Transmit Reference Generator Clock In.** Bit 1 in the transmit nibble. For a serial interface, the TCIN is used to derive the clock out (TCOUT), data signal (TDOUT), framing pulse ($\overline{\text{TFOUT}}$), and gapped clock signal ($\overline{\text{TCG}}$).The reference generator signals are provided for multiplexing the external payload data into the serial frame.

Terminal Interface

Pin #	Name	I/O/P	Description
56	XNIB0/XSD	I	**Transmit Nibble Bit 0/Transmit Serial Data.** In the nibble-parallel mode, bit 0 is the least significant bit in the nibble. For a serial interface, the input must consist of all the bits in the frame.
57	XCK	I	**Transmit Clock.** For the terminal side nibble-parallel interface, the XCK is used for all transmit timing functions, including deriving the nibble output clock (XNC) and framing pulse ($\overline{\text{XNF}}$).For the serial interface, this clock may be derived from the transmit reference generator clock output (TCOUT).
58	$\overline{\text{XNF}}$	O	**Transmit Nibble Framing Pulse.** The $\overline{\text{XNF}}$ and clock signal (XNC) are provided for multiplexing nibble data into the E2/E3 Framer from external circuitry. The negative framing pulse identifies the first bit in the frame.
59	XNC/TCOUT	O	**Transmit Nibble Clock/Transmit Reference Generator Clock Out.** The XNC is derived from the transmit clock (XCK) and is used as a time base for clocking data out of the external multiplexer and into the E2/E3 Framer. XNC is gapped during the framing pattern, service bit and BIP-4 bit times. TCOUT is derived from the input clock (TCIN), and has the same duty cycle.

Note: I = Input; O = Output; P = Power

Service Bit Interface

Pin #	Name	I/O/P	Description
9	ROD	O	**Receive Service Data Bits.** These service bits are clocked out of E2/E3 Framer on positive transitions of clock signal (ROC).
10	ROC	O	**Receive Service Bits Clock.** A gapped clock that clocks out the service bits. The clock is active only for clocking out the receive service data bits(ROD).
11	ROF	O	**Receive Service Bits Framing Pulse.** A positive framing pulse that is synchronous with the first bit in the frame.
27	TOD	I	**Transmit Service Data Bits.** The service bits are clocked into E2/E3 Framer on positive transitions of clock signal (TOC).
28	TOC	O	**Transmit Service Bits Clock.** A gapped clock that clocks in the service bits. The clock is active only for clocking in the transmit service data bits (TOD).
29	TOF	O	**Transmit Service Bits Framing Pulse.** A positive framing pulse that is synchronous with the first bit in the frame.

Note: I = Input; O = Output; P = Power

Microprocessor Interface

Pin #	Name	I/O/P	Description
36-43	AD(7-0)	I/O	**Address/Data Bus.** These leads constitute the time-multiplexed address and data bus for accessing the registers which reside in the E2/E3F.
44	$\overline{\text{SEL}}$	I	**Select.** A low enables the microprocessor to access the E2/E3F memory map for control, status, and alarm information.
45	ALE	I	**Address Latch Enable.** An active high signal generated by the microprocessor. Used by the microprocessor to hold an address stable during a read/write bus cycle.
46	$\overline{\text{RD}}$	I	**Read.** An active low signal generated by the microprocessor for reading the registers which reside in the memory map.

Microprocessor Interface

Pin #	Name	I/O/P	Description
47	$\overline{WR}$	I	**Write.** An active low signal generated by the microprocessor for writing to the registers which reside in the memory map.
48	RDY	O	**Ready.** An active high signal indicating an E2/E3F acknowledgment to the microprocessor that the addressed memory map location can complete the data transfer.

Note: I = Input; O = Output; P = Power

Control Interface

Pin #	Name	I/O/P	Description
13	NRZLINE	I	**Non-Return to Zero Line Selection.** A high enables an NRZ line input (RP and TP), and causes the HDB3 decoder/encoder to be bypassed. When low enables the dual rail interface (RP/RN and TP/TN) and the HDB3 decoder/encoder.
14	BIP-4	I	**Bit Interleaved Parity - 4.** A high enables the BIP-4 function. In the transmit direction, the BIP-4 is calculated for data nibbles only, and is sent as the last nibble in the frame format. In the receive direction, the BIP-4 is calculated for the data bits only and compared against the received value which is present in the last four bits of the frame. An output indication (BIP-4E) occurs when one or more columns do not match.
16 15	M1 M0	I	**Mode Control.** The two controls select the operating rate of the E2/E3F according to the table given below.
19	MICRO	I	**Microprocessor Mode.** A high enables the microprocessor interface. When the microprocessor is enabled, the following hardware control leads are disabled. BIP-4, Mode (M0 and M1), Serial I/O (SER), and transmit AIS ($\overline{TAIS}$). Bits are provided in the memory map for controlling these functions.
20	SER	I	**Serial Interface.** A high selects the bit-serial interface for the terminal side interface. A low selects the nibble-parallel interface.
21	$\overline{TLBK}$	I	**Terminal Loopback.** A low enables a transmit to receive loopback at the line side.
22	$\overline{PLBK}$	I	**Payload Loopback.** A low enables a receive to transmit loopback at the terminal side in the serial mode of operation only.
23	$\overline{TAIS}$	I	**Transmit Alarm Indication Signal.** A low causes an all ones signal (AIS) to be sent in place of a G.7XX frame format.
24	$\overline{LPT}$	I	**Loop Timing.** A low enables the loop timing feature. Loop timing disables the transmit clock and enables the receive clock to be used as the transmit clock.
26	$\overline{FORCEFE}$	I	**Force Framing Error.** The errored bit is sent into the framing pattern upon the high-to-low transition of this pin.

M1	M0	Recommendation	Rate (kbit/s)
0	0	G.745	8448
0	1	G.742	8448
1	0	G.753	34368
1	1	G.751	34368

Control Interface

Pin #	Name	I/O/P	Description
30	RESET	I	**Reset.** A positive pulse applied to this pin resets the internal counters, logic circuits, and the performance counters and control bits in the memory map to zero. The reset pulse is applied after the power becomes stable.
49	$\overline{\text{DAIS}}$	I	**Disable AIS.** A low disables the automatic insertion of AIS into the terminal side receive nibble/serial bit stream.
50	$\overline{\text{TLCINV}}$	I	**Transmit Line Clock Invert.** A low inverts the output clock TCK/TCKL when operating in the dual rail mode.
5	CV	O	**Coding Violation.** A positive pulse, one clock cycle wide, is generated when an **illega**l coding violation is detected.
6	$\overline{\text{RAIS}}$	O	**Receive Alarm Indication Signal.** An active low alarm occurs within one millisecond after the E2/E3F detects an all ones condition, including in the presence of a 10^{-3} error rate. An incoming signal with a framing pattern and all ones in the data field is not mistaken as an AIS.
7	$\overline{\text{RLOC}}$	O	**Receive Loss of Clock.** An active low alarm occurs when there are no transitions in the received clock (RCK/RCKL). Recovery occurs on the first clock transition.
8	$\overline{\text{RLOF}}$	O	**Receive Loss of Frame.** An active low alarm occurs when a valid frame cannot be detected accordingly to G.7XX recommendations.
12	FE	O	**Framing Error.** An active high alarm occurs when one or more framing bits are in error.
25	$\overline{\text{TLOC}}$	O	**Transmit Loss of Clock.** An active low alarm occurs when there are no transitions in the transmit clock (TCK). Recovery occurs on the first clock transition.
60	BIP-4E	O	**BIP-4E.** A positive pulse occurs when the comparison between the received BIP-4 value and the calculated value does not match in a column.

Note: I = Input, O = Output, P = Power

Functional Description

The block diagram for the E2/E3F is shown in Figure 1. The E2/E3F receives NRZ data signal (RDL) and clock signal (RCKL), or a positive (RP) and negative (RN) rail signal and clock signal (RCK), from a line interface circuit. The selection of the line interface, dual rail or NRZ, is controlled by the external lead labeled NRZ LINE. Indications of HDB3 coding violation errors are provided on an external signal lead (CV) as pulses. Coding violation errors are also counted in an 8-bit saturating counter accessed by the microprocessor through the memory map.

The selection of the framing format (G.742, G.745, G.751 or G.753) is done by external control leads (M1 and M0), or by the microprocessor. The Framer Block performs frame alignment and alarm detection including Loss of Frame ($\overline{\text{RLOF}}$), Loss of Clock ($\overline{\text{RLOC}}$), AIS detection ($\overline{\text{RAIS}}$) and BIP-4 detection (BIP-4E). A framing error (FE) output is also provided to indicate when any of the framing bits in the G. 7XX frame are in error. The disable AIS ($\overline{\text{DAIS}}$) control lead permits the E2/E3F to provide receive data on the terminal side regardless of frame alignment. The external alarm indications (latched and unlatched states) are provided in the memory map, and unlatched alarm indications are provided at signal leads.

The E2/E3F terminal side output block provides either a bit-serial or a nibble-parallel interface. The interface is selected by an external control lead (SER) or by the microprocessor. The bit-serial interface consists of the following signals: a data output signal (RSD), a clock output signal (RSC), a receive clock gapped output signal ($\overline{\text{RCG}}$), and a framing pulse ($\overline{\text{RSF}}$). The receive clock gapped signal ($\overline{\text{RCG}}$) identifies framing and service bit times. The nibble-parallel interface consists of data output signal having a nibble format (RNIB3 through RNIB0), a clock output signal (RNC), and a framing pulse ($\overline{\text{RNF}}$). In the nibble mode, the framing pattern, service bits and BIP-4 nibble are not provided at the interface. The receive nibble clock (RNC) is gapped during framing pattern, service bit and BIP-4 times.

The transmitter operates independently of the receiver, unless the loop timing feature($\overline{LPT}$) is selected, when the receive clock becomes the transmitted clock. In the transmit direction, the terminal side bit-serial interface consists of: data input signal (XSD), a clock input signal (XCK), and a framing pulse ($\overline{XSF}$). The nibble-parallel interface consists of the following signals: a data input signal having a nibble format (XNIB3 - XNIB0), a clock input signal (XCK), a framing output pulse ($\overline{XNF}$), and a nibble output clock signal (XNC). The transmit nibble clock (XNC) is stretched to accommodate the framing pattern, service bit and BIP-4 times.

MT90372 provides interface to service bits as defined in G.7XX recommendations.The receive service bit interface consists of: data output (ROD), clock output (ROC), and framing pulse (ROF) output. The clock signal (ROC) is gapped and is provided for clocking out the service bits. The service bit states are also written into E2/E3F memory locations, which can be read by the microprocessor. The transmitted service bits are inserted into the frame format from either an external interface or from memory map locations. The transmit service bit interface consists of data input signal (TOD), a clock output (TOC), and a framing pulse (TOF) output.

To fix transmit time-base for the terminal payload multiplexer circuitry, while operating in the bit-serial mode, the E2/E3F provides a transmit frame reference generator. The transmit frame reference generator accepts an external 8.448 or 34.368 MHz clock signal (TCIN) and produces a clock out signal (TCOUT), a framing pulse ($\overline{TFOUT}$), a clock gap signal ($\overline{TCG}$), and a data signal (TDOUT). The data signal consists of G.7XX framing bits and zeros elsewhere.

The selection of the transmit line interface, dual rail or NRZ, is controlled by the NRZLINE control lead, which also controls the receive interface selection. When the internal HDB3 Encoder Block is bypassed, the transmit line interface consists of a data signal (TDL) and a clock signal (TCKL). When the HDB3 encoder is enabled, the transmit line interface consists of positive (TP) and negative (TN) rail signals and a clock signal (TCK).

A high placed on the microprocessor control lead (MICRO) selects the microprocessor interface. All the external control leads, except the loop timing ($\overline{LPT}$), receive AIS disable ($\overline{DAIS}$), and the line interface control leads (NRZLINE) are disabled when the microprocessor interface is selected.

The microprocessor interface consists of eight bidirectional data and address leads (AD7 - AD0), along with other microprocessor control leads, including a ready (RDY) signal.

Typical Application

The E2/E3 Framer is used for wideband data transport as shown in Figure 2. In the receive direction, the E2/E3 Framer receives NRZ or dual rail data from LIU, removes overhead bits and puts out only the payload of the incoming signal to the terminal. Overhead bits can be accessed through microprocessor or by service bit interface. In the transmit direction, the E2/E3 Framer receives data generated from Data Source, adds framing pattern and service bits and sends it out to LIU. The E2/E3 Framer handles wideband data at either 8448 or 34 368 Kb/s, and can optionally perform BIP-4 making data transport more reliable.

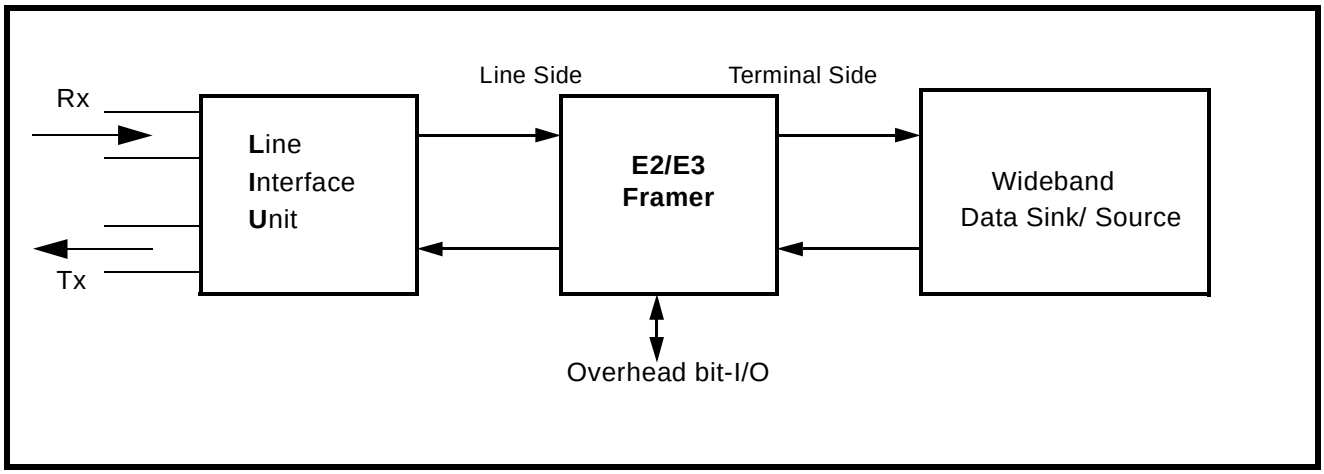

Figure 2. Wideband Data Transport using E2/E3 Framer

Notes.