

## 8051 Embedded CRT Monitor Controller MASK Version

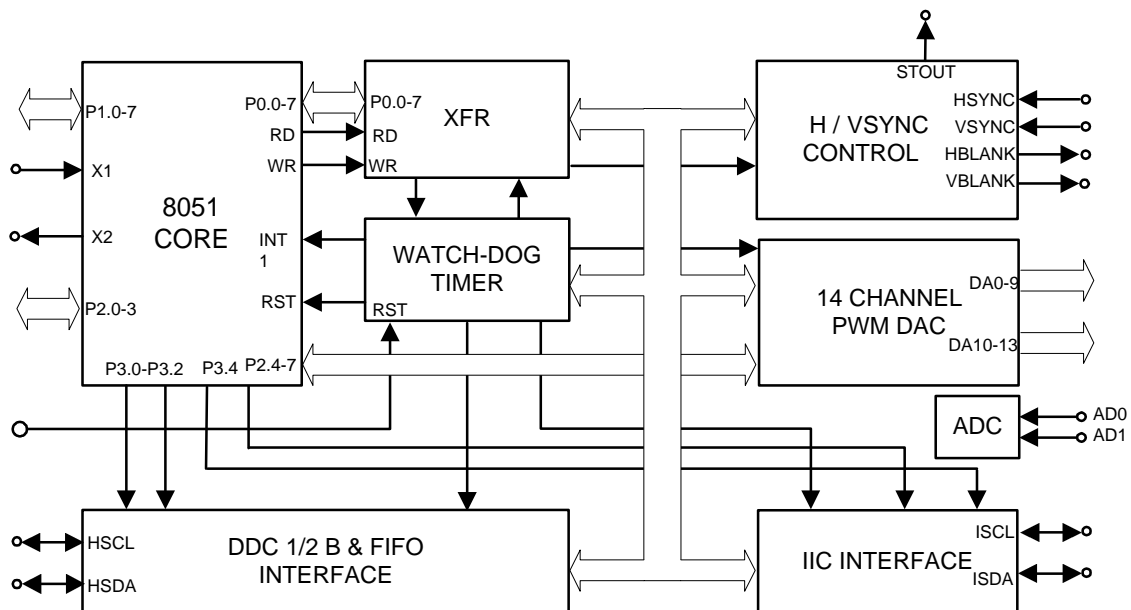
### FEATURES

- 8051 core.
- 384-bytes internal RAM.
- 16K-bytes program Mask ROM.
- 14-channels 10V open-drain PWM DAC, 10 dedicated channels and 4 channels shared with I/O pin.
- 28 bi-direction I/O pin, 12 dedicated pin, 12 shared with DAC, 4 shared with DDC/IIC interface.
- 5-output pin shared with H/V sync output and self test output pins.
- SYNC processor for composite separation, polarity and frequency check, and polarity adjustment.
- Built-in monitor self-test pattern generator.
- Built-in low power reset circuit.
- One slave mode IIC interface and one master mode IIC interface.
- IIC interface for DDC1/DDC2B and EEPROM; only one EEPROM needed to store DDC1/DDC2B and display mode information.
- Dual 4-bit ADC or 4 channel 6-bit ADC.
- Watchdog timer with programmable interval.
- 40-pin PDIP and 44-pin PLCC package.

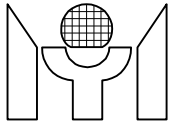
### GENERAL DESCRIPTION

The MTV112A micro-controller is an 8051 CPU core embedded device specially tailored to CRT monitor applications. It includes an 8051 CPU core, 384-byte SRAM, 14 built-in PWM DACs, DDC1/DDC2B interface, 24Cxx series EEPROM interface, A/D converter and a 16K-bytes internal program Mask ROM.

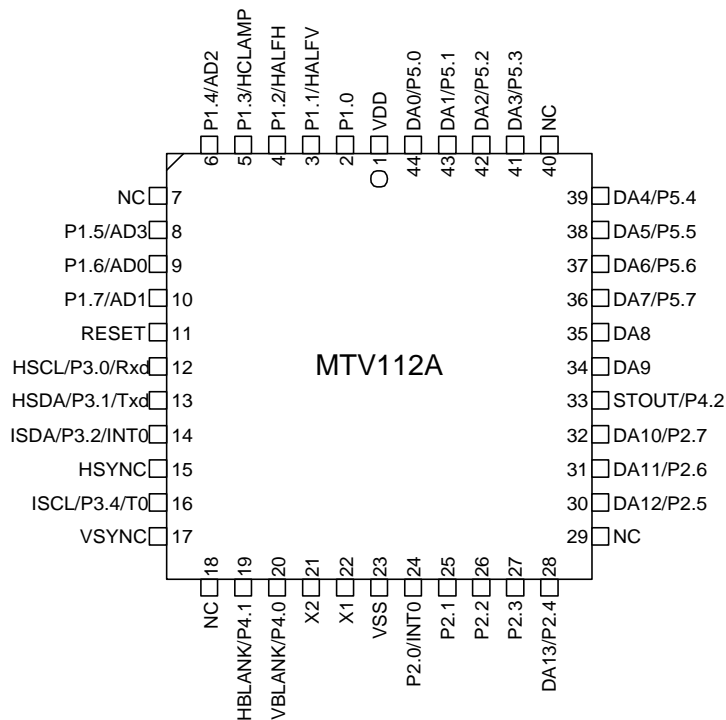
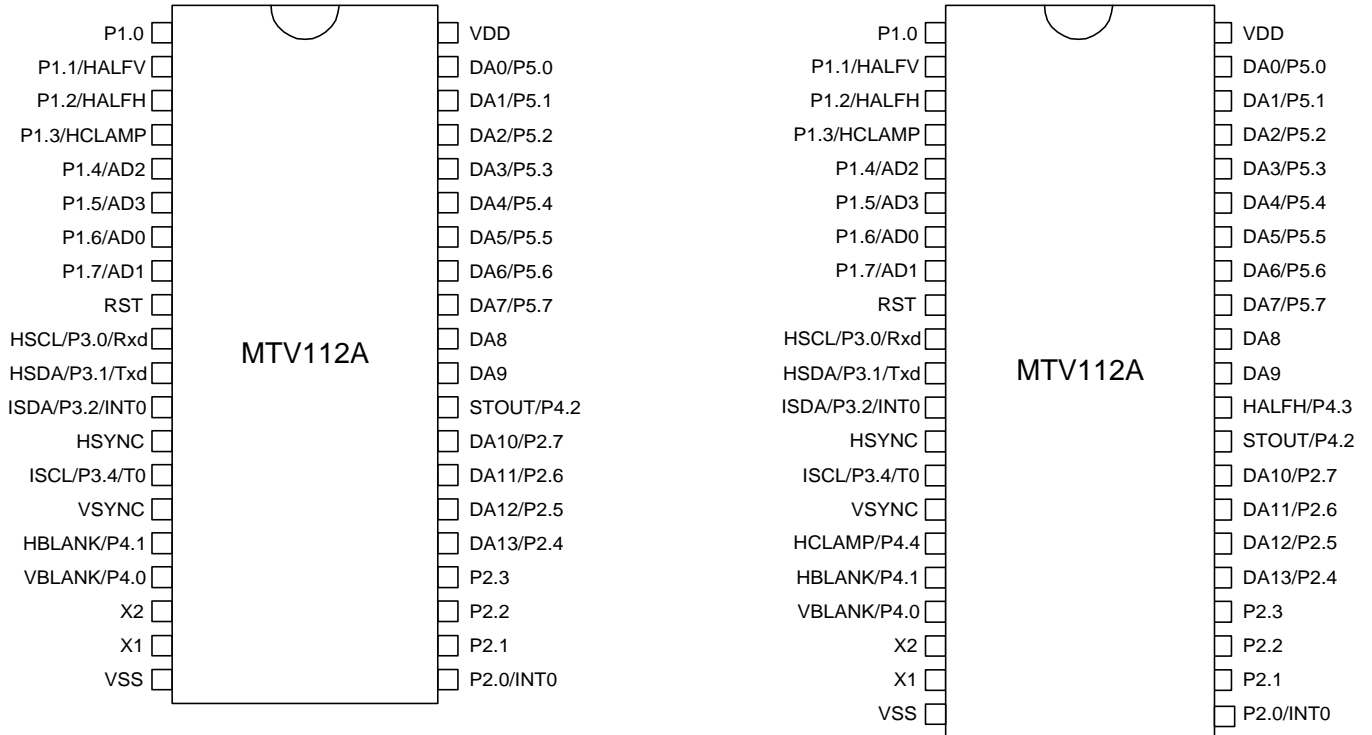
### BLOCK DIAGRAM

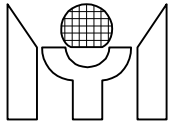


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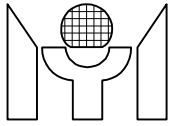
### 1.0 PIN CONNECTION





**2.0 PIN DESCRIPTIONS**

Name	Type	Pin#			Description
		40	42	44	
P1.0	I/O	1	1	2	General purpose I/O
P1.1/HALFV	I/O	2	2	3	General purpose I/O / Vsync half frequency output.
P1.2/HALFH	I/O	3	3	4	General purpose I/O / Hsync half frequency output.
P1.3/HCLAMP	I/O	4	4	5	General purpose I/O / Hsync clamp pulse output.
P1.4/AD2	I/O	5	5	6	General purpose I/O / ADC input.
P1.5/AD3	I/O	6	6	8	General purpose I/O / ADC input.
P1.6/AD0	I/O	7	7	9	General purpose I/O / ADC input
P1.7/AD1	I/O	8	8	10	General purpose I/O / ADC input
RST	I	9	9	11	Active high reset
HSCL/P3.0/Rxd	I/O	10	10	12	IIC clock / General purpose I/O / Rxd
HSDA/P3.1/Txd	I/O	11	11	13	IIC data / General purpose I/O / Txd
ISDA/P3.2/INT0	I/O	12	12	14	IIC data / General purpose I/O / INT0
HSYNC	I	13	13	15	Horizontal SYNC or Composite SYNC
ISCL/P3.4/T0	I/O	14	14	16	IIC clock / General purpose I/O / T0
VSYNC	I	15	15	17	Vertical SYNC
HCLAMP/P4.4	O	-	16	-	Hsync clamp pulse output / General purpose output
HBLANK/P4.1	O	16	17	19	Horizontal blank / General purpose output
VBLANK/P4.0	O	17	18	20	Vertical blank / General purpose output
X2	O	18	19	21	Oscillator output
X1	I	19	20	22	Oscillator input
VSS	-	20	21	23	Ground
P2.0/INT0	I/O	21	22	24	General purpose I/O / INT0
P2.1	I/O	22	23	25	General purpose I/O
P2.2	I/O	23	24	26	General purpose I/O
P2.3	I/O	24	25	27	General purpose I/O
DA13/P2.4	I/O	25	26	28	PWM DAC output / General purpose I/O (open-drain)
DA12/P2.5	I/O	26	27	30	PWM DAC output / General purpose I/O (open-drain)
DA11/P2.6	I/O	27	28	31	PWM DAC output / General purpose I/O (open-drain)
DA10/P2.7	I/O	28	29	32	PWM DAC output / General purpose I/O (open-drain)
STOUT/P4.2	O	29	30	33	Self-test video output / General purpose output
HALFH/P4.3	O	-	31	-	Hsync half frequency output / General purpose output
DA9	O	30	32	34	PWM DAC output / General purpose I/O (open-drain)
DA8	O	31	33	35	PWM DAC output / General purpose I/O (open-drain)
DA7/P5.7	O	32	34	36	PWM DAC output / General purpose I/O (open-drain)
DA6/P5.6	O	33	35	37	PWM DAC output / General purpose I/O (open-drain)
DA5/P5.5	O	34	36	38	PWM DAC output / General purpose I/O (open-drain)
DA4/P5.4	O	35	37	39	PWM DAC output / General purpose I/O (open-drain)
DA3/P5.3	O	36	38	41	PWM DAC output / General purpose I/O (open-drain)
DA2/P5.2	O	37	39	42	PWM DAC output / General purpose I/O (open-drain)
DA1/P5.1	O	38	40	43	PWM DAC output / General purpose I/O (open-drain)
DA0/P5.0	O	39	41	44	PWM DAC output / General purpose I/O (open-drain)
VDD	-	40	42	1	Positive power supply



### 3.0 FUNCTIONAL DESCRIPTION

#### 1. 8051 CPU Core

MTV112A includes all 8051 functions with the following exceptions:

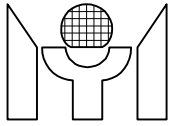
- 1.1 PSEN, ALE, RD and WR pins are disabled. The external RAM access is restricted to XFRs within MTV112A.
- 1.2 Port 0, port 3.3, and ports 3.5 ~ 3.7 are not general-purpose I/O ports. They are dedicated to monitor control or DAC pins.
- 1.3 INT1 and T1 input pins are not provided.
- 1.4 Ports 2.4 ~ 2.7 are shared with DAC pins; ports 3.0 ~ 3.2, and port3.4 are shared with monitor control pins.

In addition, there are 2 timers, 5 interrupt sources and a serial interface compatible with the standard 8051. The Txd/Rxd (P3.0/P3.1) pins are shared with DDC interface. INT0/T0 pins are shared with IIC interface. An extra option can be used to switch the INT0 source from P3.2 to P2.0. This feature maintains an external interrupt source when IIC interface is enabled.

**Note: All registers listed in this document reside in the external RAM area (XFR). For the internal RAM memory map please refer to the 8051 spec.**

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PADMOD	30h (w)	SINT0	IICF	DDCE	IICE	DA13E	DA12E	DA11E	DA10E
PADMOD	31h (w)	P57E	P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	37h (w)	-	-	-	-	-	-	-	MORE

- SINT0 = 1 → INT0 source is pin #21.
- = 0 → INT0 source is pin #12.
- IICF = 1 → Selects 400kHz master IIC speed.
- = 0 → Selects 100kHz master IIC speed.
- DDCE = 1 → Pin #10 is HSCL; pin #11 is HSDA.
- = 0 → Pin #10 is P3.0/Rxd; pin #11 is P3.1/Txd.
- IICE = 1 → Pin #12 is ISDA; pin #14 is ISCL.
- = 0 → Pin #12 is P3.2/(INT0\*); pin #14 is P3.4/T0.
- DA13E = 1 → Pin #25 is DA13.
- = 0 → Pin #25 is P2.4.
- DA12E = 1 → Pin #26 is DA12.
- = 0 → Pin #26 is P2.5.
- DA11E = 1 → Pin #27 is DA11.
- = 0 → Pin #27 is P2.6.
- DA10E = 1 → Pin #28 is DA10.
- = 0 → Pin #28 is P2.7.
- P57E = 1 → Pin #32 is P5.7.
- = 0 → Pin #32 is DA7.
- P56E = 1 → Pin #33 is P5.6.
- = 0 → Pin #33 is DA6.
- P55E = 1 → Pin #34 is P5.5.
- = 0 → Pin #34 is DA5.
- P54E = 1 → Pin #35 is P5.4.
- = 0 → Pin #35 is DA4.
- P53E = 1 → Pin #36 is P5.3.
- = 0 → Pin #36 is DA3.
- P52E = 1 → Pin #37 is P5.2.
- = 0 → Pin #37 is DA2.



- P51E = 1 → Pin #38 is P5.1.
- = 0 → Pin #38 is DA1.
- P50E = 1 → Pin #39 is P5.0.
- = 0 → Pin #39 is DA0.
- MORE = 1 → Bits P57E,P56E,P55E,P54E,P53E,P52E,P51E,P50E,DACK,EHALFV,  
          EHALFH,ENCLP,ADCMOD can be programmed,and master IIC speed is  
          controlled by (MCLK1,MCLK0) bits.
- = 0 → above bits internal keep "0" by MTV112A, and master IIC speed is controlled by  
          IICF bit.

\* SINT0 should be 0 in this case.

**2. Memory Allocation**

2.1 Internal Special Function Registers (SFR)

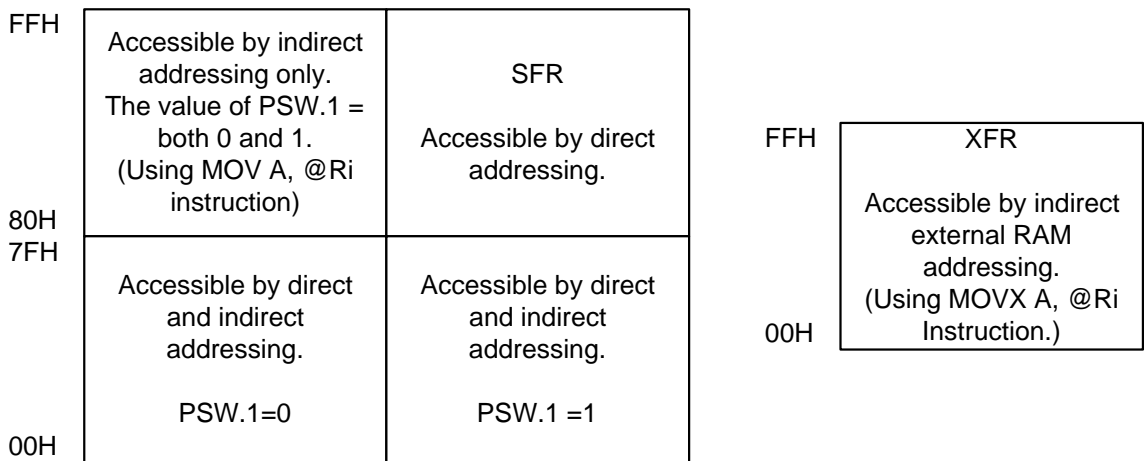
SFR is a group of registers that is the same as standard 8051.

2.2 Internal RAM

There is a 384 bytes RAM in MTV112A. The first portion of the RAM area contains 256 bytes, accessible by setting PSW.1=0; the second portion of the RAM area contains 128 bytes, accessible by setting PSW.1=1.

2.3 External Special Function Registers (XFR)

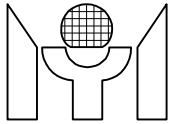
XFR is a group of registers allocated in the 8051 external RAM area. Most of the registers are used for monitor control or PWM DAC. The program can initialize Ri value and use "MOVX" instruction to access these registers.



**3. PWM DAC**

Each D/A converter's output pulse width is controlled by an 8-bit register in XFR. The frequency of PWM clk is X'tal or 2 \* X'tal, selected by DACK. And the frequency of these DAC outputs is (PWM clk frequency)/253 or (PWM clk frequency)/256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to the DAC register generates stable high output. If DIV253=0, the output will pulse low at least once even if the DAC register's content is FFH. Writing 00H to the DAC register generates stable low output.

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
<b>DA0</b>	20h (r/w)	DA0b7	DA0b6	DA0b5	DA0b4	DA0b3	DA0b2	DA0b1	DA0b0
<b>DA1</b>	21h (r/w)	DA1b7	DA1b6	DA1b5	DA1b4	DA1b3	DA1b2	DA1b1	DA1b0
<b>DA2</b>	22h (r/w)	DA2b7	DA2b6	DA2b5	DA2b4	DA2b3	DA2b2	DA2b1	DA2b0
<b>DA3</b>	23h (r/w)	DA3b7	DA3b6	DA3b5	DA3b4	DA3b3	DA3b2	DA3b1	DA3b0



<b>DA4</b>	24h (r/w)	DA4b7	DA4b6	DA4b5	DA4b4	DA4b3	DA4b2	DA4b1	DA4b0
<b>DA5</b>	25h (r/w)	DA5b7	DA5b6	DA5b5	DA5b4	DA5b3	DA5b2	DA5b1	DA5b0
<b>DA6</b>	26h (r/w)	DA6b7	DA6b6	DA6b5	DA6b4	DA6b3	DA6b2	DA6b1	DA6b0
<b>DA7</b>	27h (r/w)	DA7b7	DA7b6	DA7b5	DA7b4	DA7b3	DA7b2	DA7b1	DA7b0
<b>DA8</b>	28h (r/w)	DA8b7	DA8b6	DA8b5	DA8b4	DA8b3	DA8b2	DA8b1	DA8b0
<b>DA9</b>	29h (r/w)	DA9b7	DA9b6	DA9b5	DA9b4	DA9b3	DA9b2	DA9b1	DA9b0
<b>DA10</b>	2Ah (r/w)	DA10b7	DA10b6	DA10b5	DA10b4	DA10b3	DA10b2	DA10b1	DA10b0
<b>DA11</b>	2Bh (r/w)	DA11b7	DA11b6	DA11b5	DA11b4	DA11b3	DA11b2	DA11b1	DA11b0
<b>DA12</b>	2Ch (r/w)	DA12b7	DA12b6	DA12b5	DA12b4	DA12b3	DA12b2	DA12b1	DA12b0
<b>DA13</b>	2Dh (r/w)	DA13b7	DA13b6	DA13b5	DA13b4	DA13b3	DA13b2	DA13b1	DA13b0
<b>WDT</b>	80h	WEN	WCLR	CLRDDC	DIV253	DACK	WDT2	WDT1	WDT0

**DA0** (r/w) : The output pulse width control for DA0.

**DA1** (r/w) : The output pulse width control for DA1.

**DA2** (r/w) : The output pulse width control for DA2.

**DA3** (r/w) : The output pulse width control for DA3.

**DA4** (r/w) : The output pulse width control for DA4.

**DA5** (r/w) : The output pulse width control for DA5.

**DA6** (r/w) : The output pulse width control for DA6.

**DA7** (r/w) : The output pulse width control for DA7.

**DA8** (r/w) : The output pulse width control for DA8.

**DA9** (r/w) : The output pulse width control for DA9.

**DA10** (r/w) : The output pulse width control for DA10.

**DA11** (r/w) : The output pulse width control for DA11.

**DA12** (r/w) : The output pulse width control for DA12.

**DA13** (r/w) : The output pulse width control for DA13.

**WDT** (w) : Watchdog timer & special control bit.

DIV253 = 1 → The PWM DAC outputs frequency is (PWM clk frequency)/253.

= 0 → The PWM DAC output frequency is Xtal frequency/256.

DACK = 1 → The PWM clk frequency is 2 x (X'tal frequency).

= 0 → The PWM clk frequency is (X'tal frequency).

\*1. All D/A converters are centered with value 80h after power-on.

#### 4. H/V SYNC Processing

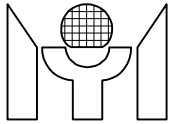
The H/V SYNC processing block performs the functions of composite signal separation, SYNC input presence check, frequency counting, and polarity detection and control, as well as the protection of VBLANK output while VSYNC speeds up to a high DDC communication clock rate. The present and frequency function block treat any pulse less than one OSC period as noise.

##### 4.1 Composite SYNC Separation

MTV112A continuously monitors the input HSYNC. If the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and the user can select the extracted "CVSYNC" for the source of polarity check, frequency count and VBLANK. The CVSYNC will have a 10-16 us delay compared to the original signal. The delay depends on the OSC frequency and composite mix method.

##### 4.2 H/V Frequency Counter

MTV112A can discriminate HSYNC/VSYNC frequency and saves the information in XFRs. The 15-bit Hcounter counts the time of the 64xHSYNC period, but only 11 upper bits are loaded into the HCNTH/HCNTL latch. The 11-bit output value is {2/H-Freq} / {1/OSC-Freq}, updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is not present. The 14-bit Vcounter counts the time between 2 VSYNC pulses, but only 9 upper bits are



loaded into the VCNT/VCNTL latch. The 9-bit output value is  $\{1/V\text{-Freq}\} / \{512/OSC\text{-Freq}\}$ , updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of the H/V counter overflow. The VFchg/HFchg interrupt is active when VCNT/HCNT value changes or overflows. Tables 4.2.1 and 4.2.2 shows the HCNT/VCNT value under the operations of 8MHz and 12MHz.

**4.2.1 H-Freq Table**

H-Freq(KHZ)		Output Value (11 bits)	
		8MHz OSC (hex / dec)	12MHz OSC (hex / dec)
1	30	215h / 533	320h / 800
2	31.5	1FBh / 507	2F9h / 761
3	33.5	1DDh / 477	2CCh / 716
4	35.5	1C2h / 450	2A4h / 676
5	36.8	1B2h / 434	28Ch / 652
6	38	1A5h / 421	277h / 631
7	40	190h / 400	258h / 600
8	48	14Dh / 333	1F4h / 500
9	50	140h / 320	1E0h / 480
10	57	118h / 280	1A5h / 421
11	60	10Ah / 266	190h / 400
12	64	0FAh / 250	177h / 375
13	100	0A0h / 160	0F0h / 240

- \*1. The H-Freq output (HF10 - HF0) is valid.
- \*2. The tolerance deviation is  $\pm 1$  LSB.

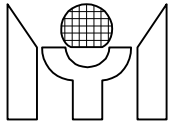
**4.2.2 V-Freq Table**

V-Freq(Hz)		Output Value (9 bits)	
		8MHz OSC (hex / dec)	12MHz OSC (hex / dec)
1	56.25	115h / 277	1A0h / 416
2	59.94	104h / 260	187h / 391
3	60	104h / 260	186h / 390
4	60.32	103h / 259	184h / 388
5	60.53	102h / 258	183h / 387
6	66.67	0EAh / 234	15Fh / 351
7	70.069	0DEh / 222	14Eh / 334
8	70.08	0DEh / 222	14Eh / 334
9	72	0D9h / 217	145h / 325
10	72.378	0D7h / 215	143h / 323
11	72.7	0D6h / 214	142h / 322
12	87	0B3h / 179	10Dh / 269

- \*1. The V-Freq output (VF8 - VF0) is valid.
- \*2. The tolerance deviation is  $\pm 1$  LSB.

**4.3 H/V Presence Check**

The Hpresent function checks the input HSYNC pulse. The Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse. The Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. A control bit "PREFS" selects the time base for these functions. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value changes. However, the CVpre flag interrupt may be disabled when S/W disables the composite function.



#### 4.4 H/V Polarity Detection

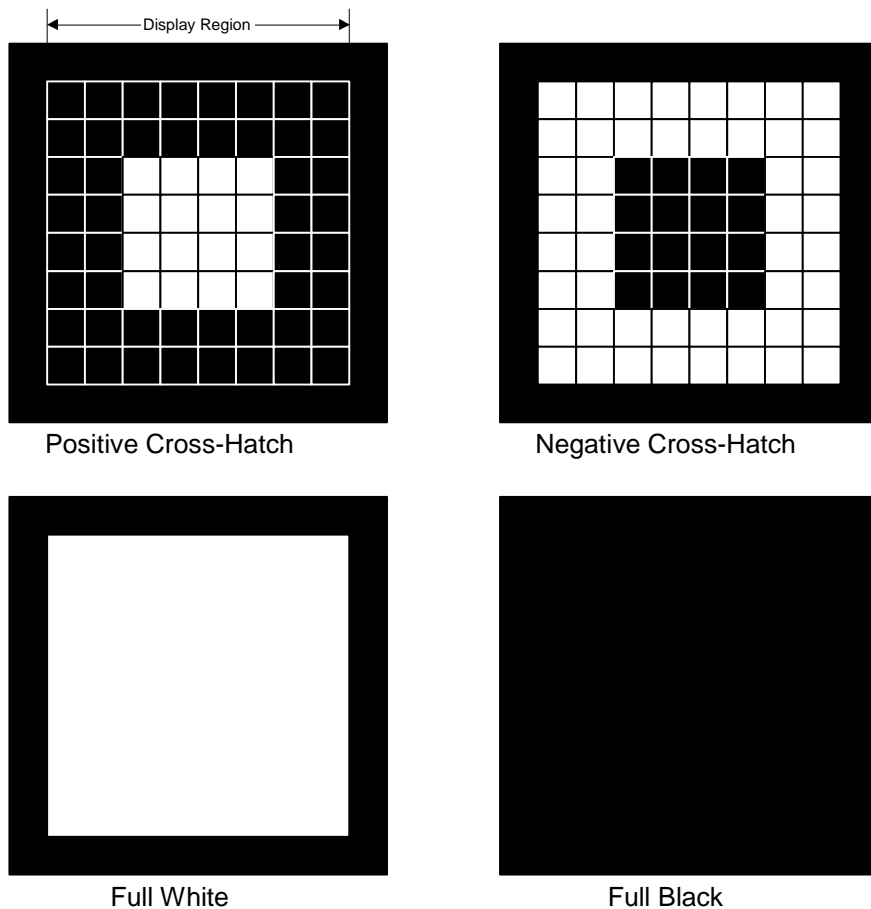
The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

#### 4.5 Output HBLANK/VBLANK Control and Polarity Adjustment

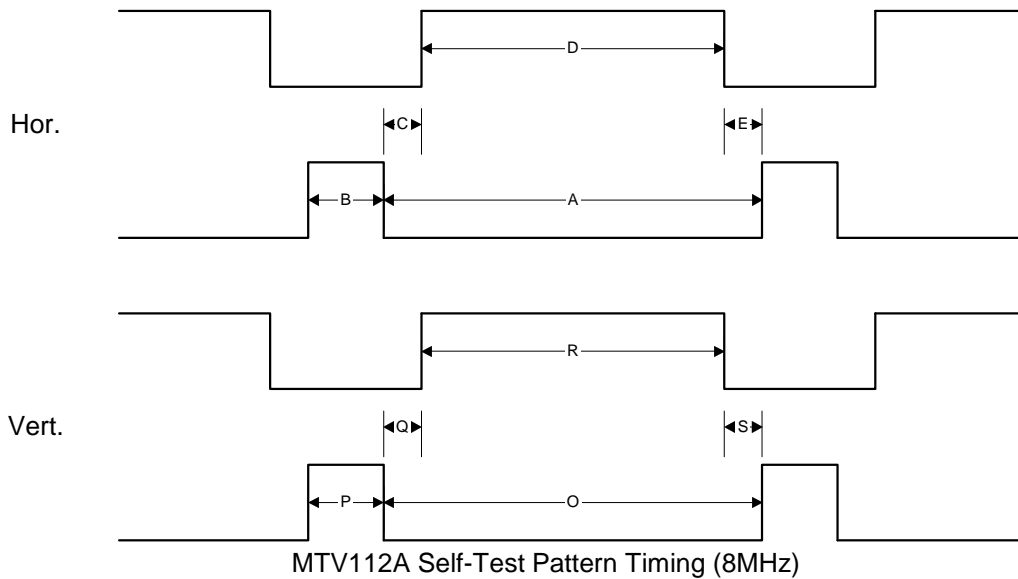
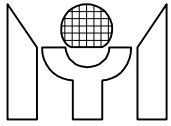
The HBLANK is the mux output of HSYNC and self-test horizontal pattern. The VBLANK is the mux output of VSYNC, CVSINC and the self-test vertical pattern. The mux selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 200Hz or 133Hz depends on 8MHz/12MHz OSC selection. The HBLANK/VBLANK shares the output pin with P4.1/ P4.0.

#### 4.6 Self-Test Pattern Generator

This generator can generate 4 display patterns for testing purposes: positive cross-hatch, negative cross-hatch, full white, and full black (shown in the following figure). It was originally designed to support the monitor manufacturer in performing a burn-in test, or to offer the end-user a reference to check the monitor. The generator's output STOUT shares the output pin with P4.2.







	63.5KHz, 60Hz		31.7KHz, 60Hz	
	Absolute time	H dots	Absolute time	H dots
Hor. Total Time	Us(A)=15.75	1280	Us(A)=31.5	640
Hor. Active Time	Us(D)=12.05	979.3	Us(D)=24.05	488.6
Hor. F. P.	Us(E)=0.2	16.25	Us(E)=0.45	9
SYNC Pulse Width	Us(B)=1.5	122	Us(B)=3	61
Hor. B. P.	Us(C)=2	162.54	Us(C)=4	81.27
	V lines		V lines	
Hor. Total Time	Us(O)=16.6635	1024	Us(O)=16.6635	480
Hor. Active Time	Us(R)=15.6555	962	Us(R)=15.6555	451
Hor. F. P.	Us(S)=0.063	3.87	Us(S)=0.063	1.82
SYNC Pulse Width	Us(P)=0.063	3.87	Us(P)=0.063	1.82
Hor. B. P.	Us(Q)=0.882	54.2	Us(Q)=0.882	25.4

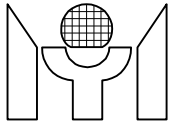
\* 8 x 8 blocks of cross-hatch pattern in display region.

#### 4.7 VSYNC Interrupt

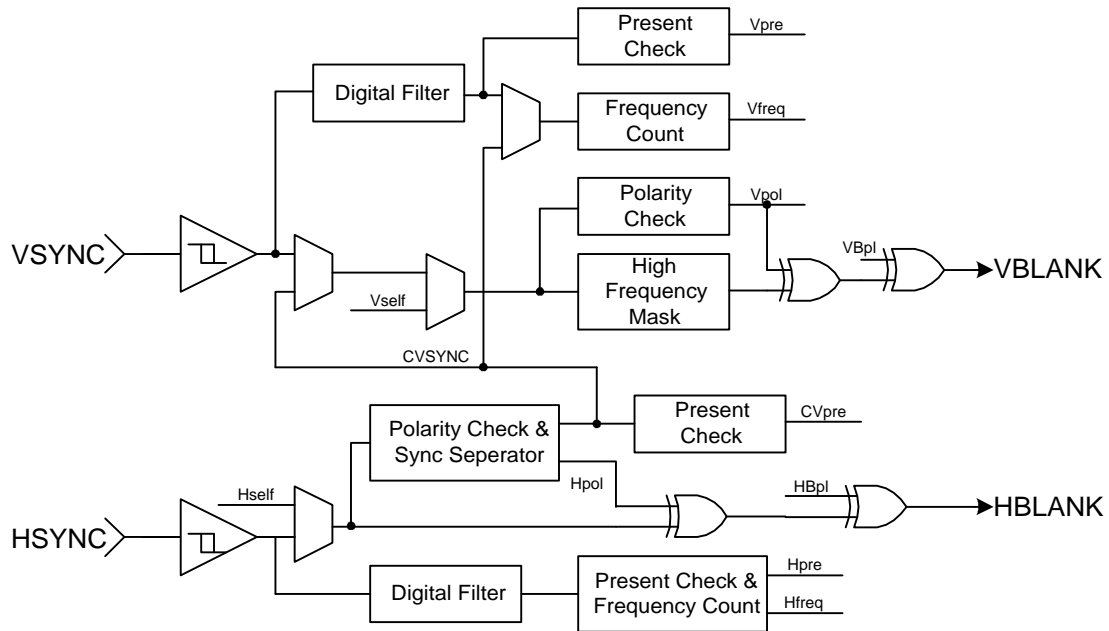
MTV112A checks the VSYNC input pulse and generates an interrupt at its leading edge. The VSYNC1 flag is set each time MTV112A detects a VSYNC pulse.

#### 4.8 H/V SYNC Processor Register

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PSTUS	40h (r)	CVpre	X	Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	41h (r)	Hovf	X	X	X	X	HF10	HF9	HF8
HCNTL	42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	43h (r)	Vovf	X	X	X	X	X	X	VF8
VCNTL	44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
PCTR0	40h (w)	C1	C0	HVsel	STOsel	PREFS	HALFV	HBpl	VBpl
PCTR2	42h (w)	X	X	X	Selft	STbsh	Rt1	Rt0	STF
PCTR3	43h (w)	ENCLP	CLPEG	CLPPO	CLPW2	CLPW1	CLPW0	EHALFV	EHALFH
P4OUT	44h (w)	X	X	X	P44	P43	P42	P41	P40



<b>P5OUT</b>	45h (r/w)	P57	P56	P55	P54	P53	P52	P51	P50
<b>PCTR6</b>	46h (w)	X	X	X	X	X	X	CLPsel	HALFHsel
<b>INTFLG</b>	50h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	FIFOI	MI
<b>INTEN</b>	60h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EFIFO	EMI
<b>INTFLG</b>	51h(r/w)	X	X	X	X	X	X	X	VSYNC
<b>INTEN</b>	61h(w)	X	X	X	X	X	X	X	EVSI



H/V SYNC Processor Block Diagram

**PSTUS** (r) : The status of polarity, presence and static level for HSYNC and VSYNC.

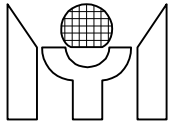
- CVpre = 1 → The extracted CVSYNC is present.
- = 0 → The extracted CVSYNC is not present.
- Hpol = 1 → HSYNC input is positive polarity.
- = 0 → HSYNC input is negative polarity.
- Vpol = 1 → VSYNC (CVSYNC) is positive polarity.
- = 0 → VSYNC (CVSYNC) is negative polarity.
- Hpre = 1 → HSYNC input is present.
- = 0 → HSYNC input is not present.
- Vpre = 1 → VSYNC input is present.
- = 0 → VSYNC input is not present.
- Hoff\* = 1 → HSYNC input's off-level is high.
- = 0 → HSYNC input's off-level is low.
- Voff\* = 1 → VSYNC input's off-level is high.
- = 0 → VSYNC input's off-level is low.

\*Hoff and Voff are valid when Hpre=0 or Vpre=0.

**HCNTH** (r) : H-Freq counter's high bits.

- Hovf = 1 → H-Freq counter overflows; this bit is cleared by H/W when condition removed.
- HF10 - HF8 : 3 high bits of H-Freq counter.

**HCNTL** (r) : H-Freq counter's low bits.



**VCNTH** (r) : V-Freq counter's high bits.  
Vovf = 1 → V-Freq counter overflows; this bit is cleared by H/W when condition removed.  
VF8 : High bit of V-Freq counter.

**VCNTL** (r) : V-Freq counter's low bits.

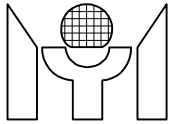
**PCTR0** (w) : SYNC processor control register 0.  
C1, C0 = 1,1 → Selects CVSYNC as the polarity, Freq and VBLANK source.  
= 1,0 → Selects VSYNC as the polarity, Freq and VBLANK source.  
= 0,0 → Disables composite function (MTV012 compatible mode).  
= 0,1 → H/W auto switches to CVSYNC when CVpre=1 and VSpre=0.  
HVsel = 1 → Pin #16 is P4.1, pin #17 is P4.0.  
= 0 → Pin #16 is HBLANK, pin #17 is VBLANK.  
STOsel = 1 → Pin #29 is P4.2.  
= 0 → Pin #29 is STOUT.  
PREFS = 0 → Selects 8MHz OSC as H/V presence check and self-test pattern time base.  
= 1 → Selects 12MHz OSC as H/V presence check and self-test pattern time base.  
HALFV = 1 → VBLANK is half frequency output of VSYNC.  
HBpl = 1 → Negative polarity HBLANK output.  
= 0 → Positive polarity HBLANK output.  
VBpl = 1 → Negative polarity VBLANK output.  
= 0 → Positive polarity VBLANK output.

**PCTR2** (w) : Self-test pattern generator control.  
Selft = 1 → Enables generator.  
= 0 → Disables generator.  
STbsh = 1 → 63.5KHz (horizontal) output selected.  
= 0 → 31.75KHz (horizontal) output selected.  
Rt1, Rt0 = 0,0 → Positive cross-hatch pattern output.  
= 0,1 → Negative cross-hatch pattern output.  
= 1,0 → Full white pattern output.  
= 1,1 → Full black pattern output.  
STF = 1 → Enables STOUT output.  
= 0 → Disables STOUT output.

**PCTR3** (w) : HSYNC clamp pulse control register.  
ENCLP = 1 → pin #4 is HCLAMP.  
= 0 → pin #4 is P1.3.  
CLPEG = 1 → Clamp pulse follows HSYNC leading edge.  
= 0 → Clamp pulse follows HSYNC trailing edge.  
CLPPO = 1 → Positive polarity clamp pulse output.  
= 0 → Negative polarity clamp pulse output.  
CLPW2 : CLPW0 : Pulse width of clamp pulse is  
[[CLPW2:CLPW0) + 1] X 0.25 μs for 8MHz X'tal selection, or  
[[CLPW2:CLPW0) + 1] X 0.167 μs for 12MHz X'tal selection.  
EHALFV = 1 → pin #2 is HALFV.  
= 0 → pin #2 is P1.1.  
EHALFH = 1 → pin #3 is HALFH.  
= 0 → pin #3 is P1.2.

**P4OUT** (w) : Port 4 data output value.

**P5OUT** (r/w) : Port 5 data input/output value.



**PCTR6 (w) :** Sync processor control register 6.  
CLPsel = 1 → pin HCLAMP/P4.4 is P4.4.  
= 0 → pin HCLAMP/P4.4 is HCLAMP.  
HALFHsel = 1 → pin HALFH/P4.3 is P4.3.  
= 0 → pin HALFH/P4.3 is HALFH.

**INTFLG (w) :** Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enabler bit is set, the 8051 core's INT1 source will be driven by a zero level. Software **MUST** clear this register while serving the interrupt routine.

HPRchg= 1 → No action.  
= 0 → Clears HSYNC presence change flag.  
VPRchg= 1 → No action.  
= 0 → Clears VSYNC presence change flag.  
HPLchg= 1 → No action.  
= 0 → Clears HSYNC polarity change flag.  
VPLchg= 1 → No action.  
= 0 → Clears VSYNC polarity change flag.  
HFchg = 1 → No action.  
= 0 → Clears HSYNC frequency change flag.  
VFchg = 1 → No action.  
= 0 → Clears VSYNC frequency change flag.  
VSYNCi= 1 → No action.  
= 0 → Clears VSYNC interrupt flag.

**INTFLG (r) :** Interrupt flag.

HPRchg= 1 → Indicates an HSYNC presence change.  
VPRchg= 1 → Indicates a VSYNC presence change.  
HPLchg= 1 → Indicates a HSYNC polarity change.  
VPLchg= 1 → Indicates a VSYNC polarity change.  
HFchg = 1 → Indicates an HSYNC frequency change or counter overflow.  
VFchg = 1 → Indicates a VSYNC frequency change or counter overflow.  
VSYNCi= 1 → Indicates a VSYNC interrupt.

**INTEN (w) :** Interrupt enabler.

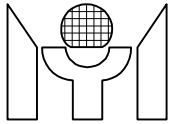
EHPR = 1 → Enables HSYNC presence change interrupt.  
EVPR = 1 → Enables VSYNC presence change interrupt.  
EHPL = 1 → Enables HSYNC polarity change interrupt.  
EVPL = 1 → Enables VSYNC polarity change interrupt.  
EHF = 1 → Enables HSYNC frequency change / counter overflow interrupt.  
EVF = 1 → Enables VSYNC frequency change / counter overflow interrupt.  
EVS I = 1 → Enables VSYNC interrupt.

## 5. DDC & IIC Interface

### 5.1 DDC1 Mode

MTV112A enters DDC1 mode after Reset. In this mode, VSYNC is used as a data clock. The HSCL pin should remain at high. The data output to the HSDA pin is taken from 8 bytes of FIFO in MTV112A. MTV112A fetches the data byte from FIFO, then sends it in a 9-bit packet format which includes a null bit (=1) as packet separator. The software program should load EDID data (original stored in EEPROM) into FIFO and take care of the FIFO depth. FIFO sets the FIFOI (FIFO low interrupt) flag when there are fewer than N (N=2,3,4 or 5 controlled by LS1, LS0) bytes to be output to the HSDA pin. To prevent FIFO from emptying, software needs to write EDID data to FIFO as soon as FIFOI is set. On the other hand, FIFO sets the FIFOH flag when its capacity is full. Software should not write additional data to FIFO in such instance. The FIFOI interrupt can be masked or enabled by an EFIFO control bit. A simple way to control FIFO is to set (LS1,

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LS0=1,0) and enable FIFOI interrupt, then software may load 4 bytes into FIFO each time a FIFOI interrupt arises. A special control bit "LDFIFO" can reduce the software effort when EDID data is stored in EEPROM. If LDFIFO=1, FIFO will be automatically loaded with MBUF data when software reads MBUF XFR.

### 5.2 DDC2B Mode

MTV112A switches to DDC2B mode when it detects a high to low transition on the HSCL pin. Once MTV112A enters DDC2B mode, the host can access the EEPROM using IIC bus protocol as if the HSDA and HSCL are directly bypassed to ISDA and ISCL pins. MTV112A will return to DDC1 mode if HSCL is kept high for a 128 VSYNC clock period. However, it will lock in DDC2B mode if a valid IIC access has been detected on HSCL/HSDA bus. The DDC2 flag reflects the current DDC status. S/W may clear it by setting CLRDDC. Control bits M128/M256 are used to block the EEPROM write operation from the host if the address is over 128/256.

### 5.3 Master Mode IIC Function Block

The master mode IIC block is connected to the ISDA and ISCL pins. Its speed can be selected to 100kHz or 400kHz by s/w set IICF control bit while MORE=0, or to 50KHz,100KHz,200KHz or 400KHz by s/w set (MCLK1,MCLK0) bits while MORE=1. The software program can access the external EEPROM through this interface. Since the EDID/VDIF data and display information share the common EEPROM, precaution must be taken to avoid bus conflict. In DDC1 mode, the IIC interface is controlled by MTV112A only. In DDC2B mode, the host may access the EEPROM directly. Software can test the HSCL condition by reading the BUSY flag, which is set in case HSCL=0. A summary of master IIC access is illustrated as follows:

#### *5.3.1. To Write EEPROM*

1. Write the EEPROM slave address to MBUF (bit 0 = 0).
  2. Set the S bit to Start.
  3. After MTV112A transmits this byte, an MI interrupt will be triggered.
  4. The program can write MBUF to transfer the next byte or set the P bit to Stop.
- \* Please see the attachments about "Master IIC Transmission Timing".

#### *5.3.2. To Read EEPROM*

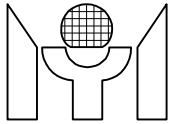
1. Write the slave address to MBUF (bit 0 = 1).
  2. Set the S bit to Start.
  3. After MTV112A transmits this byte, a MI interrupt will be triggered.
  4. Set or reset the ACK flag according to the IIC protocol.
  5. Read out the useless byte to MBUF to continue the data transfer.
  6. After MTV112A receives a new byte, the MI interrupt is triggered again.
  7. Reading MBUF also triggers the next receiving operation, but setting the P bit before reading can terminate the operation.
- \* Please see the attachments about "Master IIC Timing Receiving".

### 5.4 Slave Mode IIC Function Block

The slave mode IIC block can be connected to HSDA/HSCL or ISDA/ISCL pins, and selected by the SLVsel control bit. This block can receive/transmit data using the IIC protocol. S/W may set the SLVADR register to determine which slave address the block should respond to.

In receiving mode, the block first detects an IIC slave address match condition then issues a SLVMI interrupt. The data received from SDA is shifted into a shift register and written to the RCBUF latch. The first byte loaded is the word address (slave address is dropped). This block also generates an RCBI (Receive Buffer full Interrupt) each time the RCBUF is loaded. If S/W can't read out the RCBUF in time, the next byte will not be written to RCBUF and the slave block will return NACK to the master. This feature guarantees the data integrity of communication. A WADR flag can tell S/W if the data in RCBUF is a word address.

In transmission mode, the block first detects an IIC slave address match condition then issues a SLVMI. In the meantime, the data pre-stored in the TXBUF is loaded into the shift register, results in TXBUF emptying and generates a TXBI (Transmission Buffer Interrupt). S/W should write the TXBUF a new byte for the next transfer before the shift register empties. Failure to do this will cause data corruption. The TXBI occurs each time the shift register receives new data from TXBUF. The SLVMI is cleared by writing the SLVSTUS register. The RCBI is cleared by reading the RCBUF. The TXBI is cleared by writing the TXBUF.



If the control bit ENSCL is set, the block will hold SCL low until the RCBI/TXBI is cleared.

\*Please see the attachments about "Slave IIC Block Timing".

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
<b>MCTR</b>	00h (w)	LS1	LS0	LDIFIFO	M256	M128	ACK	P	S
<b>MSTUS</b>	00h (r)	X	SCLERR	DDC2	BERR	HFREQ	FIFOH	FIFOL	BUSY
<b>MCTR</b>	01h (w)	X	X	X	X	X	X	MCLK1	MCLK0
<b>MBUF</b>	10h (r/w)	MBUF7	MBUF6	MBUF5	MBUF4	MBUF3	MBUF2	MBUF1	MBUF0
<b>INTFLG</b>	50h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	FIFOI	MI
<b>INTEN</b>	60h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EFIFO	EMI
<b>FIFO</b>	70h (w)	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
<b>SLVCTR</b>	90h (w)	ENSLV	SLVsel	ERCBI	ESLVMI	ETXBI	ENSCL	X	X
<b>SLVSTUS</b>	91h (r)	WADR	SLVS	RCBI	SLVMI	TXBI	RWB	ACKIN	X
<b>SLVSTUS</b>	91h (w)	Write to clear SLVMI							
<b>RCBUF</b>	92h (r)	RCbuf7	RCbuf6	RCbuf5	RCbuf4	RCbuf3	RCbuf2	RCbuf1	RCbuf0
<b>TXBUF</b>	92h (w)	TXbuf7	TXbuf6	TXbuf5	TXbuf4	TXbuf3	TXbuf2	TXbuf1	TXbuf0
<b>SLVADR</b>	93h (w)	SLVadr7	SLVadr6	SLVadr5	SLVadr4	SLVadr3	SLVadr2	SLVadr1	X

**MCTR** (w) : Master IIC interface control register.

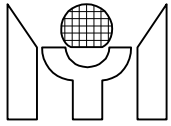
- LS1, LS0 = 11 → FIFOL is the status in which FIFO depth < 5.
- = 10 → FIFOL is the status in which FIFO depth < 4.
- = 01 → FIFOL is the status in which FIFO depth < 3.
- = 00 → FIFOL is the status in which FIFO depth < 2.
- LDIFIFO = 1 → FIFO will be written while S/W reads MBUF.
- M256 = 1 → Disables host writing EEPROM when address is over 256.
- M128 = 1 → Disables host writing EEPROM when address is over 128.
- ACK = 1 → In receiving mode, no acknowledgment is given by MTV112A.
- = 0 → In receiving mode, ACK is returned by MTV112A.
- S, P = ↑, 0 → Start condition when Master IIC is not transferring.
- = X, ↑ → Stop condition when Master IIC is not transferring.
- = 1, X → Will resume transfer after a read/write MBUF operation.
- = X, 0 → Forces HSCL low and occupies the IIC bus.
- MCLK1 : MCLK0 : Master IIC speed select,
- = 0 → 50KHz for 8MHz X'tal, 75KHz for 12MHz X'tal.
- = 1 → 100KHz for 8MHz X'tal, 150KHz for 12MHz X'tal.
- = 2 → 200KHz for 8MHz X'tal, 300KHz for 12MHz X'tal .
- = 3 → 400KHz for 8MHz X'tal, 600KHz for 12MHz X'tal.

\* MTV112A uses a 100KHz clock to sample the S/P bit; any pulse should sustain at least 20us.

\* A write/read MBUF operation can be recognized only after 10us of the MI flag's rising edge.

**MSTUS** (r) : Master IIC interface status register.

- SCLERR = 1 → The ISCL pin has been pulled low by other devices during the transfer, cleared when S=0.
- DDC2 = 1 → DDC2B is active.
- = 0 → MTV112A remains in DDC1 mode.
- BERR = 1 → IIC bus error, no ACK received from the slave, updated each time the slave sends ACK on the ISDA pin.
- HFREQ = 1 → MTV112A has detected a higher than 200Hz clock on the VSYNC pin.
- FIFOH = 1 → FIFO high indicated.
- FIFOL = 1 → FIFO low indicated.
- BUSY = 1 → Host drives the HSCL pin to low.



\* While writing FIFO, the FIFOH/FIFOL flag will reflect the FIFO condition after 30us.

**MBUF (w) :** Master IIC data shift register, after START and before STOP condition, write this register will resume MTV112A's transmission to the IIC bus.

**MBUF (r) :** Master IIC data shift register, after START and before STOP condition, read this register will resume MTV112A's receiving from the IIC bus.

**INTFLG (w) :** Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enabler bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

FIFOI = 1 → No action.  
= 0 → Clears FIFOI flag.  
MI = 1 → No action.  
= 0 → Clears Master IIC bus interrupt flag (MI).

**INTFLG (r) :** Interrupt flag.

FIFOI = 1 → Indicates the FIFO low condition; when EFIFO is set, MTV112A will be interrupted by INT1.  
MI = 1 → Indicates when a byte is sent/received to/from the IIC bus; when EME is active, MTV112A will be interrupted by INT1.

**INTEN (w) :** Interrupt enabler.

EFIFO = 1 → Enables FIFO interrupt.  
EMI = 1 → Enables Master IIC bus interrupt.

**FIFO (w) :** Writes FIFO contents.

**SLVCTR (w) :** Slave IIC block control.

ENSLV = 1 → Enables slave IIC block.  
= 0 → Disables slave IIC block.  
SLVsel = 1 → Slave IIC connects to ISDA/ISCL.  
= 0 → Slave IIC connects to HSDA/HSCL.  
ERCBI = 1 → Enables slave receiving buffer interrupt.  
ESLVMI = 1 → Enables slave address match interrupt.  
ETXBI = 1 → Enables slave transmission buffer interrupt.  
ENSCL = 1 → Enables slave block to hold SCL pin low.

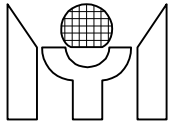
**SLVSTUS (r) :** Slave IIC block status.

WADR = 1 → The data in SLVBUF is a word address.  
SLVS = 1 → The slave block has detected a START; cleared when STOP detected.  
RCBI = 1 → RCBUF has loaded a new data byte; reset by S/W reading RCBUF.  
SLVMI = 1 → The slave block has detected the slave address match condition; cleared by S/W writing SLVSTUS.  
TXBI = 1 → TXBUF is empty; reset by S/W writing TXBUF.  
RWB = 1 → Current transfer is slave transmitting.  
= 0 → Current transfer is slave receiving.  
ACKIN = 1 → Master responds to NACK.

**SLVSTUS (w) :** Clears SLVMI flag.

**RCBUF (r) :** Slave IIC receives data buffer.

**TXBUF (w) :** Slave IIC transmits data buffer.



**SLVADR (w)** : Slave IIC address to which the slave block should respond.

### 6. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of the power supply is below 4.0V for a specific time, the LVR will generate a chip resetting signal. After the power supply is above 4.0V, LVR maintains the reset state for 144 Xtal cycles to guarantee the chip exit reset condition has a stable Xtal oscillation. The specific time of power supply in a low level is 3us and is adjustable by an external capacitor connected to the RST pin.

The watchdog timer automatically generates a device reset when it overflows. The interval of overflow is 0.25 sec x N, in which N is a number from 1 to 8, and can be programmed via register WDT (2:0). The timer function is disabled after power-on reset. The user can activate this function by setting WEN and clear the timer by setting WCLR.

### 7. A/D Converter

The MTV112 is equipped with two 4-bit or four 6-bit A/D converters. Each one can be enabled/disabled by S/W control. The refresh rate for the ADC is OSC freq./6144(4-bit) or OSC freq./12288(6-bit). The ADC compare the input pin voltage with the internal  $VDD \cdot N/16$ (4-bit) or  $VDD \cdot N/64$ (6-bit) voltage (where  $N = 0 - 15$  or  $N = 0 - 63$ ). The ADC output value is N when pin voltage is greater than  $VDD \cdot N/16$  or  $VDD \cdot N/64$  and smaller than  $VDD \cdot (N+1)/16$  or  $VDD \cdot (N+1)/64$ .

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
<b>ADC</b>	A0h (w)	ENADC	X	X	X	X	X	EADC1	EADC0
<b>ADC</b>	A0h (r)	AD1b3	AD1b2	AD1b1	AD1b0	AD0b3	AD0b2	AD0b1	AD0b0
<b>ADC</b>	A0h (r)	X	X	ADb5	ADb4	ADb3	ADb2	ADb1	ADb0
<b>WDT</b>	80h (w)	WEN	WCLR	CLRDDC	DIV253	DACK	WDT2	WDT1	WDT0

**WDT (w)** : Watchdog timer control register.

WEN	= 1	→ Enables watchdog timer.
WCLR	= 1	→ Clears watchdog timer.
CLRDDC	= 1	→ Clears DDC2 flag.
WDT2: WDT0	= 0	→ Overflow interval = 8 x 0.25 sec.
	= 1	→ Overflow interval = 1 x 0.25 sec.
	= 2	→ Overflow interval = 2 x 0.25 sec.
	= 3	→ Overflow interval = 3 x 0.25 sec.
	= 4	→ Overflow interval = 4 x 0.25 sec.
	= 5	→ Overflow interval = 5 x 0.25 sec.
	= 6	→ Overflow interval = 6 x 0.25 sec.
	= 7	→ Overflow interval = 7 x 0.25 sec.

**ADC (w)** : ADC control.

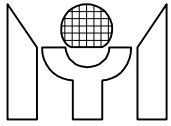
ENADC	= 1	→ Enables ADC.
ADCMOD	= 1	→ 4 channels 6 bits ADC are selected.
	= 0	→ Dual 4 bits ADC are selected.(ADC1 and ADC0)
EADC3	= 1	→ Enables ADC3 pin input.
EADC2	= 1	→ Enables ADC2 pin input.
EADC1	= 1	→ Enables ADC1 pin input.
EADC0	= 1	→ Enables ADC0 pin input.

**Note:** Only one ADC input can be enabled at the same time.

**ADC (r)** : ADC conversion result.

AD1b3: AD1b0	4-bit ADC1 convert result.
AD0b3: AD0b0	4-bit ADC0 convert result.





ADb5: ADb0 6-bit ADC convert result.

#### 4.0 Test Mode Condition

In normal applications, users should avoid the MTV012 entering its test/program mode, outlined as follow:

Test Mode A: RESET=1 & DA9=0 & DA8=1 & DA7=1 & DA6=0

Test Mode B: RESET falling edge & DA9=1 & DA8=0 & DA7=1 & DA6=0

### 5.0 ELECTRICAL PARAMETERS

#### 5.1 Absolute Maximum Ratings

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +6.0	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	°C
Maximum Storage Temperature	Tstg	-25 to +125	°C

#### 5.2 Allowable Operating Conditions

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	4.0	6.0	V
Input "H" Voltage	Vih1	0.4 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	-0.3	0.15 x VDD	V
Operating Freq.	Fopg	-	15	MHz

#### 5.3 DC Characteristics

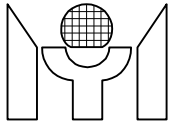
at: Ta=0 to 70 °C, VDD=4.0V ~ 6.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage, except open-drain pins: pin #s 16, 17, 29	Voh1	Ioh=-50uA	4			V
Output "H" Voltage, pin #s 16, 17, 29	Voh2	Ioh=-1mA	4			V
Output "L" Voltage	Vol	Iol=8mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=5V	50		150	Kohm
Pin Capacitance	Cio				15	pF

#### 5.4 AC Characteristics

at: Ta=0 to 70 °C, VDD=4.0V ~ 6.0V, VSS=0V

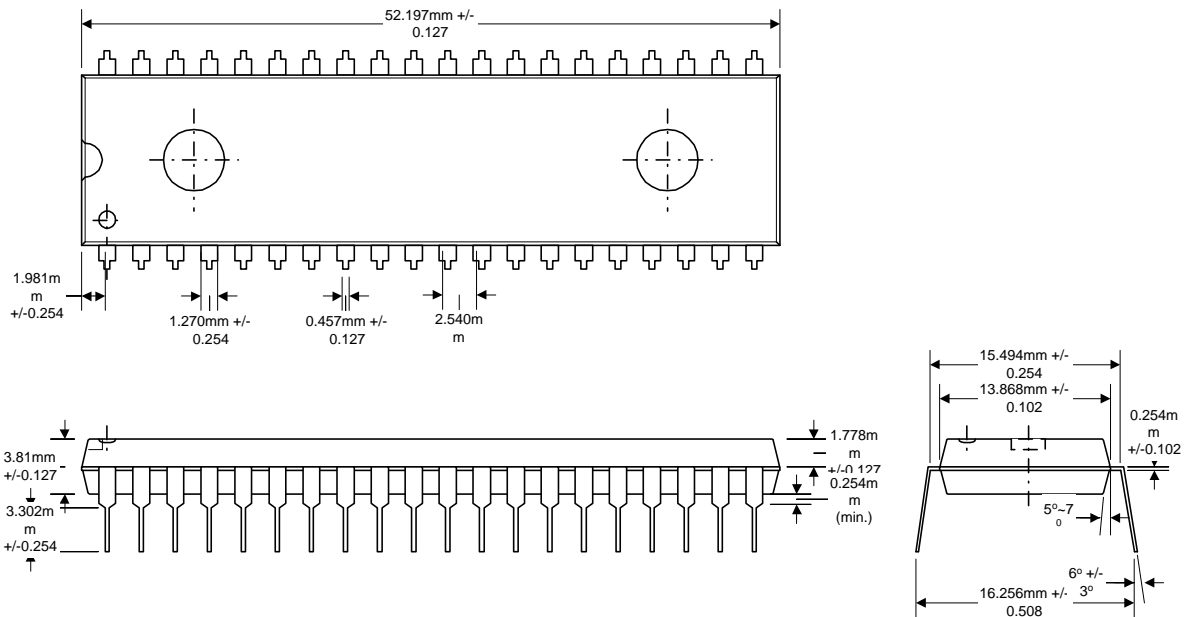
Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			8		MHz
PWM DAC Frequency	fDA	fXtal=8MHz	31.25		31.62	KHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		47.43	KHz
HS Input Pulse Width	tHIPW	fXtal=8MHz	0.3		12	uS



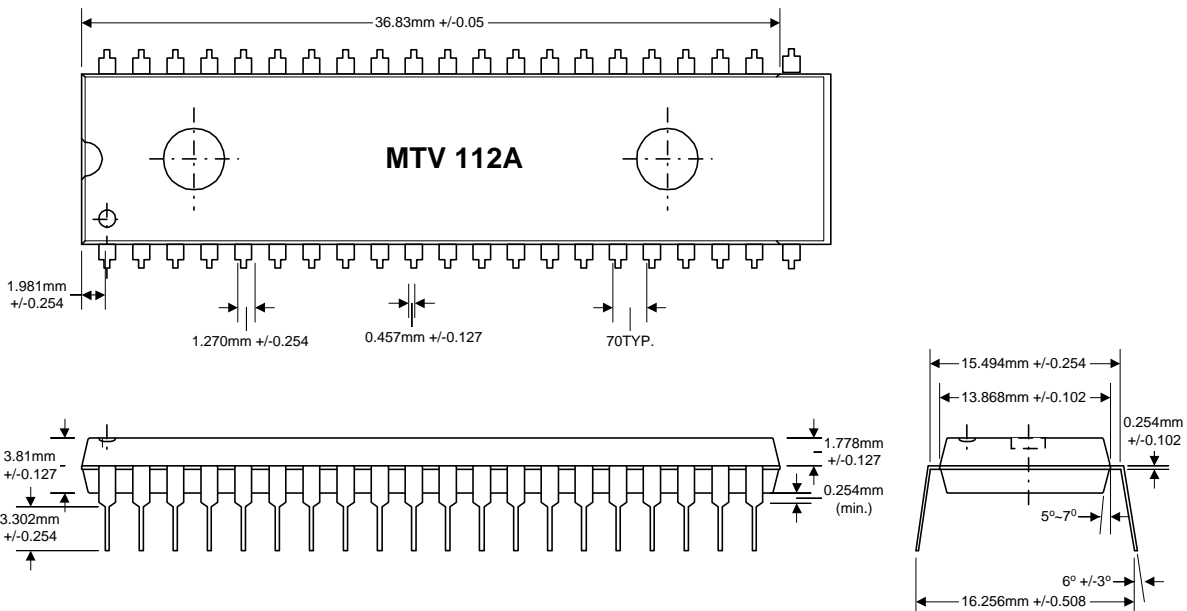
VS Input Pulse Width	tVIPW	fXtal=8MHz	3			US
HS Input Pulse Width	tHIPW	fXtal=12MHz	0.2		8	US
VS Input Pulse Width	tVIPW	fXtal=12MHz	2			US
HSYNC to HBLANK Output Jitter	tHHBJ				5	NS
H+V to VBLANK Output Delay	tVVBD	fXtal=8MHz		16		uS
H+V to VBLANK Output Delay	tVVBD	fXtal=12MHz		10		uS
VS Pulse Width in H+V Signal	tVCPW	fXtal=8MHz	32			uS
VS Pulse Width in H+V Signal	tVCPW	fXtal=12MHz	20			uS

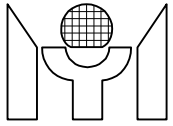
## 6.0 PACKAGE DIMENSION

### 6.1 40 pin PDIP 600 mil

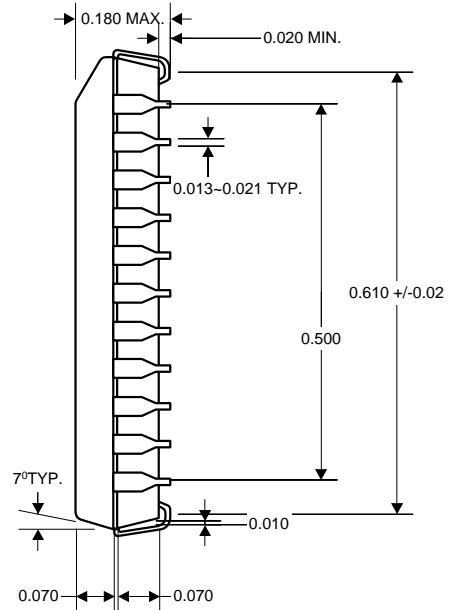
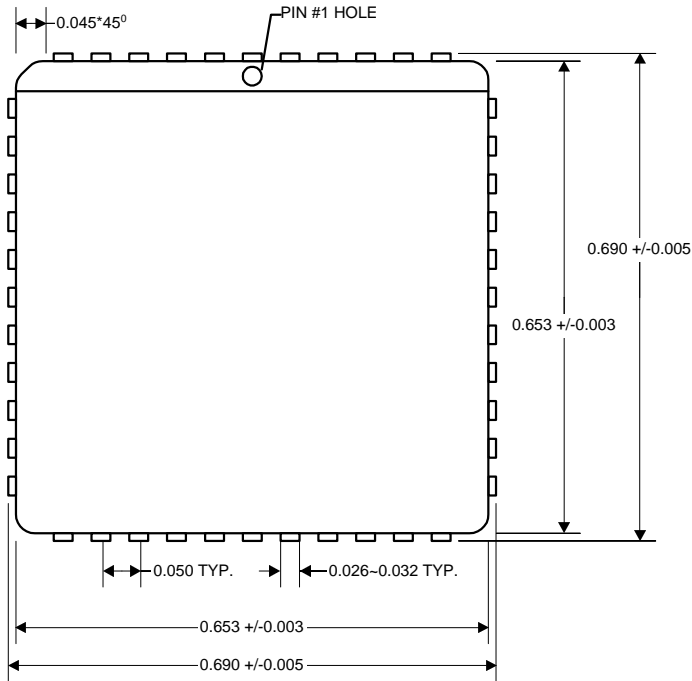


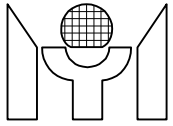
### 6.2 42 pin SDIP 600 mil





6.3 44 pin PLCC Unit: inch





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## 7.0 Ordering Information

Standard configurations:

Prefix	Part Type	Package Type	Other Information
MTV	112A	N: PDIP V: PLCC	

Part Numbers:

