On-Screen Display for LCD Monitor

FEATURES

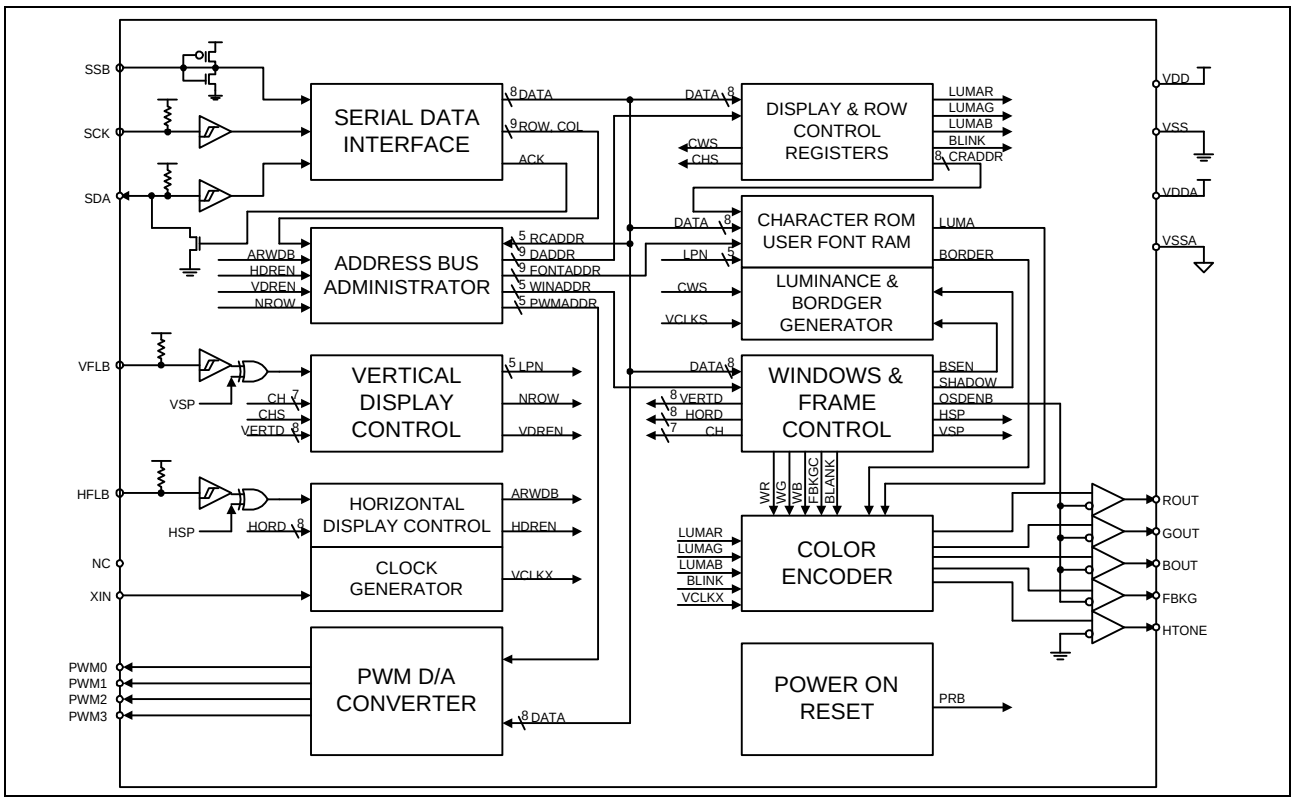
- Horizontal SYNC input up to 150 KHz.
- Acceptable wide-range pixel clock up to 150 MHz.
- Full screen self-test pattern generator.
- Full-screen display consists of 15 (rows) by 30 (columns) characters.
- Two font size 12x16 or 12x18 dot matrix per character.
- True totally 512 mask ROM fonts including 496 standard fonts and 16 multi-color fonts.
- 8 color selection maximum per display character.
- Double character height and/or width control.
- Programmable positioning for display screen center.
- Character bordering, shadowing and blinking effect.
- Programmable character height (18 to 71 lines) control.
- Row to row spacing control to avoid expansion distortion.
- 4 programmable windows with multi-level operation.
- Shadowing on windows with programmable shadow width/height/color.
- Software clears bit for full-screen erasing.
- Intensity and fast blanking output.
- Fade-in/fade-out or blending-in/blending-out effects.
- 4-channel/8-bit PWM D/A converter output.
- Compatible with SPI bus or I^2C interface with slave address 7AH (slave address is mask option).
- 16-pin or 20-pin PDIP/SOP package.

GENERAL DESCRIPTION

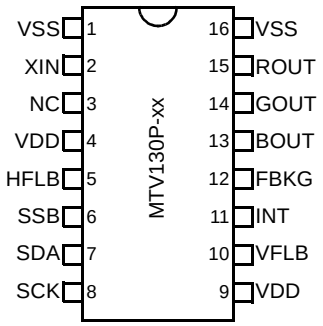
MTV130 is designed for LCD monitor applications to display built-in characters or fonts onto an LCD monitor screens. The display operation occurs by transferring data and control information from the micro-controller to RAM through a serial data interface. It can execute full-screen display automatically, as well as specific functions such as character background, bordering, shadowing, blinking, double height and width, font by font color control, frame positioning, frame size control by character height and row-to-row spacing, horizontal display resolution, full-screen erasing, fade-in/fade-out effect, windowing effect, shadowing on window and full-screen self-test pattern generator.

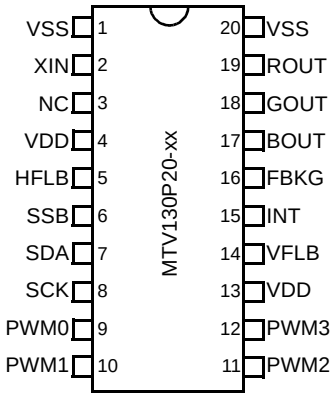
MTV130 provides true 512 fonts including 496 standard fonts and 16 multi-color fonts and 2 font sizes, 12x16 or 12x18 for more efficacious applications. So each one of the 512 fonts can be displayed at the same time. The full OSD menu is formed by 15 rows x 30 columns, which can be positioned anywhere on the monitor screen by changing vertical or horizontal delay.

BLOCK DIAGRAM



1.0 PIN CONNECTION





2.0 PIN DESCRIPTIONS

Name	I/O	Pin No.		Descriptions
		P16	P20	
VSS	-	1	1	**Ground.** This ground pin is used to internal circuitry.
XIN	I	2	2	**Pixel clock input.** This is a clock input pin. MTV130 is driven by an external pixel clock source for all the logics inside. The frequency of XIN must be the integral time of pin HFLB.
NC	I	3	3	**No connection.**
VDD	-	4	4	**Power supply.** Positive 5 V DC supply for internal circuitry. And a 0.1uF decoupling capacitor should be connected across to VDD and VSS.
HFLB	I	5	5	**Horizontal input.** This pin is used to input the horizontal synchronizing signal. It is a leading edge triggered and has an internal pull-up resistor.
SSB	I	6	6	**Serial interface enable.** It is used to enable the serial data and is also used to select the operation of I^2C or SPI bus. If this pin is left floating, I^2C bus is enabled, otherwise the SPI bus is enabled.
SDA	I	7	7	**Serial data input.** The external data transfer through this pin to internal display registers and control registers. It has an internal pull-up resistor.
SCK	I	8	8	**Serial clock input.** The clock-input pin is used to synchronize the data transfer. It has an internal pull-up resistor.
PWM0	O	-	9	**Open-Drain PWM D/A converter 0.** The output pulse width is programmable by the register of Row 15, Column 23.
PWM1	O	-	10	**Open-Drain PWM D/A converter 1.** The output pulse width is programmable by the register of Row 15, Column 24.
PWM2	O	-	11	**Open-Drain PWM D/A converter 2.** The output pulse width is programmable by the register of Row 15, Column 25.
PWM3	O	-	12	**Open-Drain PWM D/A converter 3.** The output pulse width is programmable by the register of Row 15, Column 26.

Name	I/O	Pin No.		Descriptions
		P16	P20	
VDD	-	9	13	**Power supply.** Positive 5 V DC supply for internal circuitry and a 0.1uF decoupling capacitor should be connected across to VDD and VSS.
VFLB	I	10	14	**Vertical input.** This pin is used to input the vertical synchronizing signal. It is leading triggered and has an internal pull-up resistor.
INT	O	11	15	**Intensity color output.** 16-color selection is achievable by combining this intensity pin with R/G/B output pins.
FBKG	O	12	16	**Fast Blanking output.** It is used to cut off external R, G, B signals of VGA while this chip is displaying characters or windows.
BOUT	O	13	17	**Blue color output.** It is a blue color video signal output.
GOUT	O	14	18	**Green color output.** It is a green color video signal output.
ROUT	O	15	19	**Red color output.** It is a red color video signal output.
VSS	-	16	20	**Ground.** This ground pin is used to internal circuitry.

3.0 FUNCTIONAL DESCRIPTIONS

3.1 SERIAL DATA INTERFACE

The serial data interface receives data transmitted from an external controller. And there are 2 types of bus can be accessed through the serial data interface, one is SPI bus and other is I^2C bus.

3.1.1 SPI bus

While SSB pin is pulled to "high" or "low" level, the SPI bus operation is selected. And a valid transmission should be starting from pulling SSB to "low" level, enabling MTV130 to receiving mode, and retain "low" level until the last cycle for a complete data packet transfer. The protocol is shown in Figure 1.

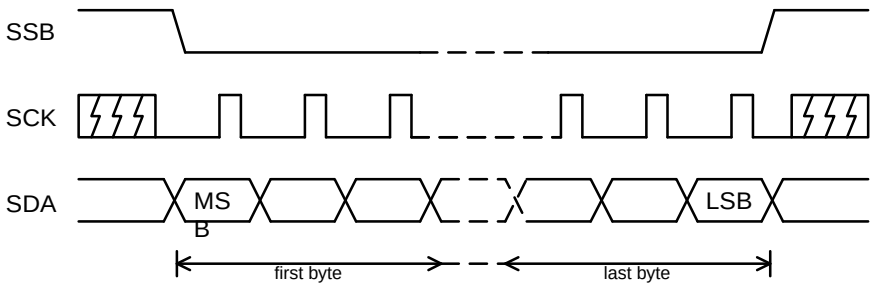


FIGURE 1. Data Transmission Protocol (SPI)

There are three transmission formats shown as below:
Format (a) R - C - D → R - C - D → R - C - D .....
Format (b) R - C - D → C - D → C - D → C - D .....
Format (c) R - C - D → D → D → D → D → D .....
Where R=Row address, C=Column address, D=Display data

3.1.2 I^2C bus

I^2C bus operation is only selected when SSB pin is left floating. And a valid transmission should be starting from writing the slave address 7AH to MTV130. The protocol is shown in Figure 2.

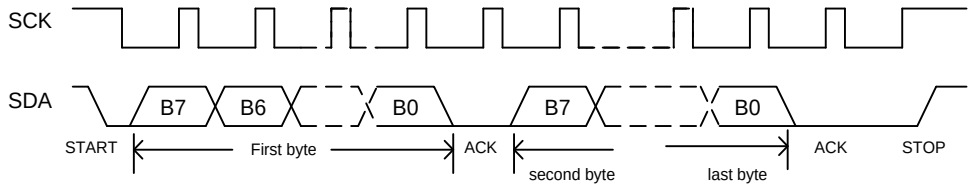


FIGURE 2. Data Transmission Protocol (I^2C)

There are three transmission formats shown as below:
Format (a) S - R - C - D → R - C - D → R - C - D .....
Format (b) S - R - C - D → C - D → C - D → C - D .....
Format (c) S - R - C - D → D → D → D → D → D .....
Where S=Slave address, R=Row address, C=Column address, D=Display data

Each arbitrary length of data packet consists of 3 portions viz, Row address (R), Column address (C), and Display data (D). Format (a) is suitable for updating small amount of data which will be allocated with different row address and column address. Format (b) is recommended for updating data that has same row address but different column address. Massive data updating or full screen data change should use format (c) to increase transmission efficiency. The row and column address will be incremented automatically when the format (c) is applied. Furthermore, the undefined locations in display or fonts RAM should be filled with dummy data.

TABLE 1. The configuration of transmission formats.

	Address	b7	b6	b5	b4	b3	b2	b1	b0	Format
Address Bytes of Display Reg.	Row	1	0	0	x	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	**D8**	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	**D8**	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c
Attribute Bytes of Display Reg.	Row	1	0	1	R4	R3	R2	R1	R0	a,b,c
	$Column_{ab}$	0	0	x	C4	C3	C2	C1	C0	a,b
	$Column_c$	0	1	x	C4	C3	C2	C1	C0	c
	Data	D7	D6	D5	D4	D3	D2	D1	D0	a,b,c

There are 2 types of data should be accessed through the serial data interface, one is **ADDRESS** bytes of display registers, and other is **ATTRIBUTE** bytes of display registers, the protocol are same for all except the bit5 of row address and the bit5 of column address. The MSB(b7) is used to distinguish row and column addresses when transferring data from external controller. The bit6 of column address is used to differentiate the column address for format (a), (b) and format (c) respectively. Bit5 of row address for display register is used to distinguish ADDRESS byte when it is set to "0" and ATTRIBUTE byte when it is set to "1". And **at address bytes, bit5 of column address is the MSB (bit8) and data bytes are the 8 LSB (bit7~bit0) of display fonts address** to save half MCU memory for true 512 fonts. So each one of the 512 fonts can be displayed at the same time. See Table 1. And for format (c), since D8 is filled while program column address of address bytes, the continued data will be the same bank of upper 256 fonts or lower 256 fonts until program column address of address bytes again.
The data transmission is permitted to change from format (a) to format (b) and (c), or from format (b) to format (a) and (c), but not from format (c) back to format (a) and (b). The alternation between transmission formats is configured as the state diagram shown in Figure 3.

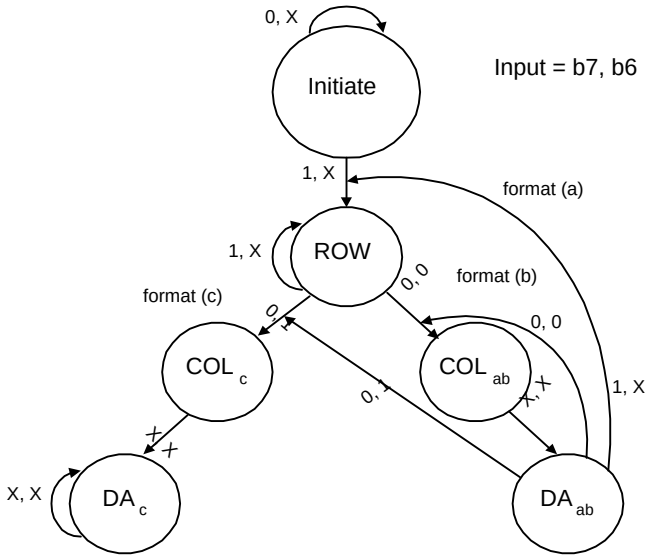


FIGURE 3. Transmission State Diagram

3.2 Address bus administrator

The administrator manages bus address arbitration of internal registers or user fonts RAM during external data write in. The external data write through serial data interface to registers must be synchronized by internal display timing. In addition, the administrator also provides automatic increment to address bus when external write using format (c).

3.3 Vertical display control

The vertical display control can generates different vertical display sizes for most display standards in current monitors. The vertical display size is calculated with the information of double character height bit(CHS), vertical display height control register(CH6-CH0).The algorithm of repeating character line display are shown as Table 2 and Table 3. The programmable vertical size range is 270 lines to maximum 2130 lines.

The vertical display center for full screen display could be figured out according to the information of vertical starting position register (VERTD) and VFLB input. The vertical delay starting from the leading edge of VFLB, is calculated with the following equation:

Vertical delay time = (VERTD * 4 + 1) * H Where H = one horizontal line display time

TABLE 2. Repeat line weight of character

CH6 - CH0	Repeat Line Weight
CH6,CH5=11	+18*3
CH6,CH5=10	+18*2
CH6,CH5=0x	+18
CH4=1	+16
CH3=1	+8
CH2=1	+4
CH1=1	+2
CH0=1	+1

TABLE 3. Repeat line number of character

Repeat Line Weight	Repeat Line #																	
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
+1	-	-	-	-	-	-	-	-	v	-	-	-	-	-	-	-	-	-
+2	-	-	-	-	v	-	-	-	-	-	-	-	v	-	-	-	-	-
+4	-	-	v	-	-	-	v	-	-	-	v	-	-	-	v	-	-	-
+8	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	v	-	-
+16	-	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+17	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	-
+18	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v	v

Note:" v " means the nth line in the character would be repeated once, while " - " means the nth line in the character would not be repeated.

3.4 Horizontal display control

The horizontal display control is used to generate control timing for horizontal display based on double character width bit (CWS), horizontal positioning register (HORD) and HFLB input. A horizontal display line includes 360 dots for 30 display characters and the remaining dots for blank region. The horizontal delay starting from HFLB leading edge is calculated with the following equation,

Horizontal delay time = (HORD * 6 + 49) * P
Where P = 1 XIN pixel display time

3.5 Display & Row control registers

The internal RAM contains display and row control registers. The display registers have 450 locations which are allocated between (row 0, column 0) to (row 14, column 29), as shown in Figure 4 and Figure 5. Each display register has its corresponding character address on ADDRESS byte, its corresponding background color, 1 blink bit and its corresponding color bits on ATTRIBUTE bytes. The row control register is allocated at column 30 for row 0 to row 14 of attribute bytes, it is used to set character size to each respective row. If double width character is chosen, only even column characters could be displayed on screen and the odd column characters will be hidden.

ROW #	COLUMN #		
	0 1 ... 28 29	30	31
0 1 13 14	CHARACTER ADDRESS BYTES of DISPLAY REGISTERS	ROW ATTRIBUTE CRTL REG	RESERVED

FIGURE 4. Address Bytes of Display Registers Memory Map

ROW #	COLUMN #	
	0 1 ... 28 29	30 ... 31
0 1 13 14	CHARACTER ATTRIBUTE BYTES of DISPLAY REGISTERS	RESERVED

ROW 15	COLUMN#			
	0 ... 11	12 ... 22	23 ... 27	28 ... 31
	WINDOW1 ~ WINDOW4	FRAME CRTL REG	PWM D/A CRTL REG	RESERVED

ROW 16	COLUMN#	
	0 ... 1	2 ... 31
	WINDOW SHADOW COLOR	RESERVED

FIGURE 5. Attribute Bytes of Display Registers Memory Map

ADDRESS BYTES:
Address registers,

b8	b7	b6	b5	b4	b3	b2	b1	b0
				CRADDR				
MSB								LSB

CRADDR - Define ROM character address from address 0 to 511.

Row Control Registers, (Row 0 - 14)

COLN 30	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	CHS	CWS

CHS - Define double height character to the respective row.

CWS - Define double width character to the respective row.

ATTRIBUTE BYTES:

b7	b6	b5	b4	b3	b2	b1	b0
-	BGR	BGG	BGB	BLINK	R	G	B

BGR, BGG, BGB - These three bits define the color of the background for its relative address character. If all three bits are clear, no background will be shown(transparent). Therefore, total 7 background color can be selected.

BLINK - Enable blinking effect while this bit is set to " 1 ". And the blinking is alternate per 32 vertical frames.

R, G, B - These three bits are used to specify its relative address character color.

3.6 Character ROM

MTV130 character ROM contains 512 built-in characters and symbols including 496 standard fonts and 16 multi-color fonts. The 496 standard fonts are located from address 0 to 495. And the 16 multi-color fonts are located from address 496 to 511. Each character and symbol consists of 12x18 dots matrix. The detail pattern structures for each character and symbols are shown in “CHARACTERS AND SYMBOLS PATTERN” on page 18.

3.7 Multi-Color Font

The color fonts comprises three different R, G, B fonts. When the code of color font is accessed, the separate R/G/B dot pattern is output to corresponding R/G/B output. See Figure 6 for the sample displayed color font. Note: No black color can defined in color font, black window underline the color font can make the dots become black in color. The detail pattern structures for each character and symbols are shown in “CHARACTERS AND SYMBOLS PATTERN” on page 18.

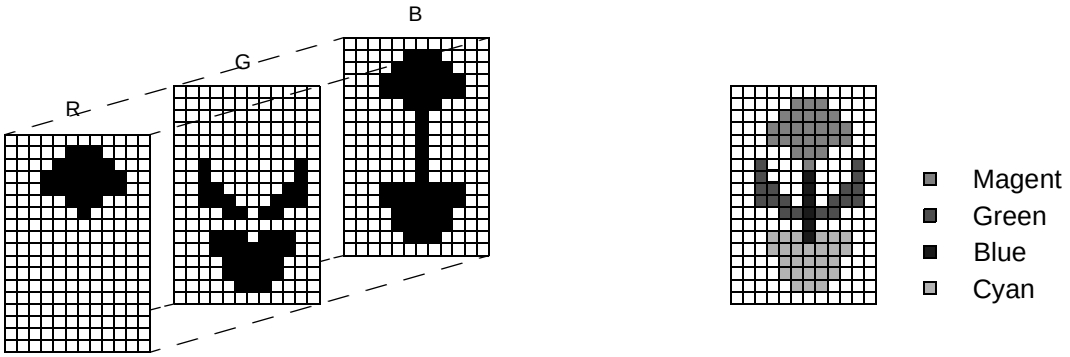


FIGURE 6. Example of Multi-Color Font

TABLE 4. The Multi-Color Font Color Selection

	R	G	B
Background Color	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magent	1	0	1
Yellow	1	1	0
White	1	1	1

3.8 Luminance & border generator

There are 3 shift registers included in the design which can shift out of luminance and border dots to color encoder. The bordering and shadowing feature is configured in this block. For bordering effect, the character will be enveloped with blackedge on four sides. For shadowing effect, the character is enveloped with blackedge for right and bottom sides only.

3.9 Window and frame control

The display frame position is completely controlled by the contents of VERTD and HORD. The window size and position control are specified in column 0 to 11 on row 15 of memory map, as shown in Figure 5. Window 1 has the highest priority, and window 4 is the least, when two windows are overlapping. More detailed information is described as follows:

1. Window control registers,

ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 0,3,6,OR 9	ROW START ADDR MSB LSB				ROW END ADDR MSB LSB			

	b7	b6	b5	b4	b3	b2	b1	b0
Column 1,4,7,OR 10	COL START ADDR MSB LSB					WEN	-	WSHD

	b7	b6	b5	b4	b3	b2	b1	b0
Column 2,5,8,OR 11	COL END ADDR MSB LSB					R	G	B

START(END) ADDR - These addresses are used to specify the window size. It should be noted that when the start address is greater than the end address, the window will be disabled.

WEN - Enable the relative background window display.

WSHD - Enable shadowing on the window.

R, G, B - Specify the color of the relative background window.

2. Frame control registers,

ROW 15

	b7	b6	b5	b4	b3	b2	b1	b0
Column 12	VERTD MSB LSB							

VERTD - Specify the starting position for vertical display. The total steps are 256, and the increment of each step is 4 Horizontal display lines. The initial value is 4 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 13	HORD MSB LSB							

HORD - Define the starting position for horizontal display. The total steps are 256, and the increment of each step is 6 dots. The initial value is 15 after power up.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 14	-	CH6	CH5	CH4	CH3	CH2	CH1	CH0

CH6-CH0 - Define the character vertical height, the height is programmable from 18 to 71 lines. The character vertical height is at least 18 lines if the contents of CH6-CH0 is less than 18. For example, when the contents is " 2 ", the character vertical height is regarded as equal to 20 lines. And if the con-

tents of CH4-CH0 is greater than or equal to 18, it will be regarded as equal to 17. See Table 2 and Table 3 for detail description of this operation.

Column 15	b7	b6	b5	b4	b3	b2	b1	b0
	Reserved							

This byte is reserved for internal testing.

Column 16	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	RSPACE				
				MSB				LSB

RSPACE - Define the row to row spacing in unit of horizontal line. That is, extra RSPACE horizontal lines will be appended below each display row, and the maximum space is 31 lines. The initial value is 0 after power up.

Column 17	b7	b6	b5	b4	b3	b2	b1	b0
	OSDEN	BSEN	SHADOW	FBEN	BLEND	WENCLR	RAMCLR	FBKGC

OSDEN - Activate the OSD operation when this bit is set to "1". The initial value is 0 after power up.

BSEN - Enable the bordering and shadowing effect.

SHADOW - Bordering and shadowing effect select bit. Activate the shadowing effect if this bit is set, otherwise the bordering is chosen.

FBEN - Enable the fade-in/fade-out and blending-in/blending-out effect when OSD is turned on from off state or vice verca.

BLEND - Fade-in/fade-out and blending-in/blending-out effect select bit. Activate the blendinf-in/blending-out function if this bit is set, otherwise the fade-in/fade-out function is chosen. These function roughly takes about 0.5 second to fully display the whole menu or to disappear completely.

WENCLR - Clear all WEN bits of window control registers when this bit is set to "1". The initial value is 0 after power up.

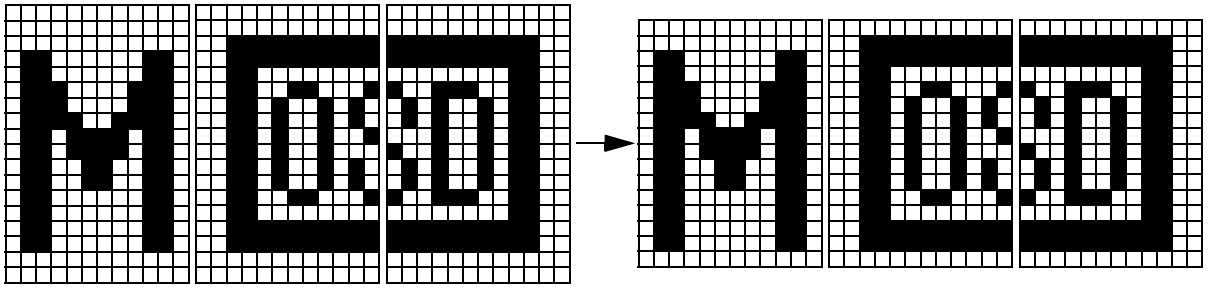
RAMCLR - Clear all ADDRESS bytes, BGR, BGG, BGB and BLINK bits of display registers when this bit is set to "1". The initial value is 0 after power up.

FBKGC - Define the output configuration for FBKG pin. When it is set to "0", the FBKG outputs high during the displaying of characters or windows, otherwise, it outputs high only during the displaying of character.

Column 18	B7	b6	b5	b4	b3	b2	b1	b0
	TRIC	FSS	-	DWE	HSP	VSP	PWM1	PWM0

TRIC - Define the driving state of output pins ROUT, GOUT, BOUT and FBKG when OSD is disabled. That is, while OSD is disabled, these four pins will drive low if this bit is set to 1, otherwise these four pins are in high impedance state. The initial value is 0 after power up.

FSS - Font size selection.
= 1 $\Rightarrow$ 12x18 font size selected.
= 0 $\Rightarrow$ 12x16 font size selected.



Fonts designed to be 12x18 display **Output display if FSS=0; first and last lines omitted**

FIGURE 7. 12x18 and 12x16 Fonts

DWE - Enable double width. When the bit is set to “1”, the display of OSD menu can change to half resolution for double character width, and then the number of pixels of each line should be even. The initial value is 0 after power up.

HSP - = 1 ⇒ Accept positive polarity Hsync input.
= 0 ⇒ Accept negative polarity Hsync input.

VSP - = 1 ⇒ Accept positive polarity Vsync input.
= 0 ⇒ Accept negative polarity Vsync input.

PWM1, PWM0 - Select the PWMCK output frequency.
= (0, 0) ⇒ XIN frequency /8
= (0, 1) ⇒ XIN frequency /4
= (1, 0) ⇒ XIN frequency /2
= (1, 1) ⇒ XIN frequency /1
The initial value is (0, 0) after power up.

Notes : When XIN is not present, don’t write data in any address. If data is written in any other address, a malfunction may occur.

TABLE 5. PWMCK Frequency and PWMDA sampling rate

(PWM1, PWM0)	PWMCK Freq	PWMDA sampling rate
(0, 0)	XIN frequency /8	XIN frequency /(8 * 256)
(0, 1)	XIN frequency /4	XIN frequency /(4 * 256)
(1, 0)	XIN frequency /2	XIN frequency /(2 * 256)
(1 ,1)	XIN frequency /1	XIN frequency /(1 * 256)

Column 19	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	CSR	CSG	CSB

CSR, CSG, CSB - Define the color of bordering or shadowing on characters. The initial value is (0, 0, 0) after power up.

Column 20	B7	b6	b5	b4	b3	b2	b1	b0
	FSW	-	-	-	-	FSR	FSG	FSB

FSW - Enable full screen self-test pattern and force the FBKG pin output to high to disable video RGB while this bit is set to "1". The self-test pattern’s color is determined by (FSR, FSG, FSB) bits.

FSR, FSG, FSB - Define the color of full screen self-test pattern.

Column 21	B7	b6	b5	b4	b3	b2	b1	b0
	WW41	WW40	WW31	WW30	WW21	WW20	WW11	WW10

WW41, WW40 - Determines the shadow width of the window 4 when WSHD bit of th window 4 is enabled. Please refer to the Table 6 for more details.

TABLE 6. Shadow Width Setting

(WW41, WW40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Width (unit in Pixel)	2	4	6	8

WW31, WW30 - Determines the shadow width of the window 3 when WSHD bit of th window 3 is enabled.

WW21, WW20 - Determines the shadow width of the window 2 when WSHD bit of th window 2 is enabled.

WW11, WW10 - Determines the shadow width of the window 1 when WSHD bit of th window 1 is enabled.

Column 22	B7	b6	b5	b4	b3	b2	b1	b0
	WH41	WH40	WH31	WH30	WH21	WH20	WH11	WH10

WH41, WH40 - Determines the shadow height of the window 4 when WSHD bit of th window 4 is enabled. Please refer to the Table 7 for more details.

TABLE 7. Shadow Height Setting

(WH41, WH40)	(0, 0)	(0, 1)	(1, 0)	(1, 1)
Shadow Height (unit in Line)	2	4	6	8

WH31, WH30 - Determines the shadow height of the window 3 when WSHD bit of th window 3 is enabled.
WH21, WH20 - Determines the shadow height of the window 2 when WSHD bit of th window 2 is enabled.
WH11, WH10 - Determines the shadow height of the window 1 when WSHD bit of th window 1 is enabled.

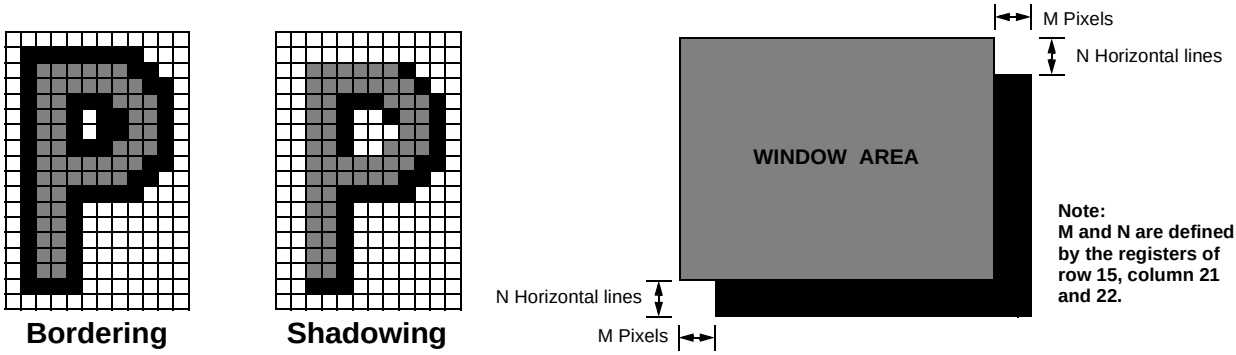


FIGURE 8. Character Bordering and Shadowing and Shadowing on Window

3.10 Color encoder

The encoder generates the video output to ROUT, GOUT and BOUT by integrating window color, border blackedge, luminance output and color selection output (R, G, B) to form the desired video outputs.

3.11 PWM D/A converter

There are 4 open-drain PWM D/A outputs (PWM0 to PWM3). These PWM D/A converter outputs pulse width are programmable by writing data to Column 23 to 26 registers of Row 15 with 8-bit resolution to control the pulse width duration from 0/256 to 255/256. And the sampling rate is selected by (PWM1, PWM0) shown as table 5. In applications, all open-drain output pins should be pulled-up by external resistors to supply voltage (5V to 9V) for desired output range.

	b7	b6	b5	b4	b3	b2	b1	b0
Column 23 | Column 26	PWMDA0 | PWMDA3							
	MSB							LSB

PWMDA0 - PWMDA3 - Define the output pulse width of pin PWM0 to PWM3.

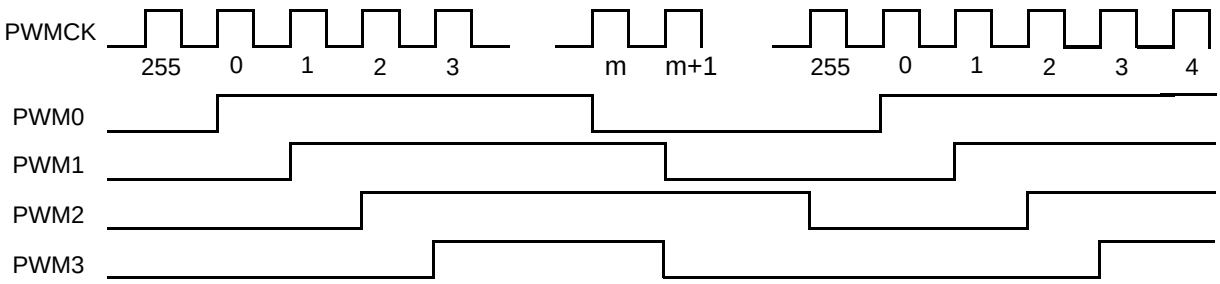


FIGURE 9. 5 Channel PWM Output Rising Edges Are Separated by One PWMCK

Column 27 ~ column 31 : Reserved.

Notes : The register located at column 31 of row 15 are reserved for the testing. Don't program this byte anytime in normal operation.

ROW 16

	B7	b6	b5	b4	b3	b2	b1	b0
Column 0	-	R1	G1	B1	-	R2	G2	B2

R1, G1, B1 - Define the shadow color of window 1. The initial value is (0, 0, 0) after power up.

R2, G2, B2 - Define the shadow color of window 2. The initial value is (0, 0, 0) after power up.

	B7	b6	b5	b4	b3	b2	b1	b0
Column 1	-	R3	G3	B3	-	R4	G4	B4

R3, G3, B3 - Define the shadow color of window 3. The initial value is (0, 0, 0) after power up.

R4, G4, B4 - Define the shadow color of window 4. The initial value is (0, 0, 0) after power up.

Column 2	B7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	D2	D1	D0

D2-D0 - These 3 bits define the setup time of HFLB to XIN and the propagation delay R, G, B, FBKG and INT outputs. Please refer to Figure 12 and Table 8. The initial value is (0, 0, 0) after power up.

TABLE 8. Output and HFLB timing to Pixel Clock

Symbol	(D2, D1, D0)	Min.	Typ.	Max.	Unit
t_{SETUP}	0	10	-	-	ns
	1	11	-	-	ns
	2	12	-	-	ns
	3	13	-	-	ns
	4	14	-	-	ns
	5	15	-	-	ns
	6	16	-	-	ns
	7	17	-	-	ns
t_{HOLD}	-	500	-	-	ns
t_{pd}	0	8	-	10	ns
	1	9	-	11	ns
	2	10	-	12	ns
	3	11	-	13	ns
	4	12	-	14	ns
	5	13	-	15	ns
	6	14	-	16	ns
	7	15	-	17	ns

Column 3 ~ column 31 : Reserved.

4.0 ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage(VDD,VDDA)	-0.3 to +7 V
Voltage with respect to Ground	-0.3 to VDD+0.3 V
Storage Temperature	-65 to +150 ^{o}C
Ambient Operating Temperature	0 to +70 ^{o}C

5.0 OPERATING CONDITIONS

DC Supply Voltage(VDD,VDDA)	+4.75 to +5.25 V
Operating Temperature	0 to +70 ^{o}C

6.0 ELECTRICAL CHARACTERISTICS (Under Operating Conditions)

Symbol	Parameter	Conditions (Notes)	Min.	Max.	Units
V_{IH}	Input High Voltage (pin hflb, vflb, sda, sck, ssb)	-	0.7 * VDD	VDD+0.3	V

Symbol	Parameter	Conditions (Notes)	Min.	Max.	Units
V_{IL}	Input Low Voltage (pin hflb, vflb, sda, sck)	-	VSS-0.3	0.3 * VDD	V
	Input Low Voltage (pin ssb)	-	VSS-0.3	0.2 * VDD	V
V_{OH}	Output High Voltage	$I_{OH} \geq$ -5 mA	VDD-0.8	-	V
V_{OL}	Output Low Voltage	$I_{OL} \leq$ 5 mA	-	0.5	V
V_{ODH}	Open Drain Output High Voltage	- (For all OD pins, and pulled up by external 5 to 9V power supply)	5	9	V
V_{ODL}	Open Drain Output Low Voltage	5 mA $\geq I_{DOL}$ (For all OD pins)	-	0.5	V
I_{CC}	Operating Current	Pixel rate=150MHz I_{load} = 0uA	-	25	mA
I_{SB}	Standby Current	Vin = VDD, I_{load} = 0uA	-	12	mA

7.0 SWITCHING CHARACTERISTIC (Under Operating Conditions)

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{HFLB}	HFLB input frequency	15	-	150	KHz
f_{VFLB}	VFLB input frequency	-	-	200	Hz
T_r	Output rise time	-	3	-	ns
T_f	Output fall time	-	3	-	ns
t_{BCSU}	SSB to SCK set up time	200	-	-	ns
t_{BCH}	SSB to SCK hold time	100	-	-	ns
t_{DCSU}	SDA to SCK set up time	200	-	-	ns
t_{DCH}	SDA to SCK hold time	100	-	-	ns
t_{SCKH}	SCK high time	500	-	-	ns
t_{SCKL}	SCK low time	500	-	-	ns
$t_{SU:STA}$	START condition setup time	500	-	-	ns
$t_{HD:STA}$	START condition hold time	500	-	-	ns
$t_{SU:STO}$	STOP condition setup time	500	-	-	ns
$t_{HD:STO}$	STOP condition hold time	500	-	-	ns
t_{SETUP}	minimum HFLB delay to rising edge of pixel clock	TBD	-	TBD	ns
t_{HOLD}	minimum pulse width of HFLB	25	-	-	ns
t_{pd}	propagation delay of output to pixel clock	TBD	-	TBD	ns
PIXin	pixel clock input	6	-	150	MHz

8.0 TIMING DIAGRAMS

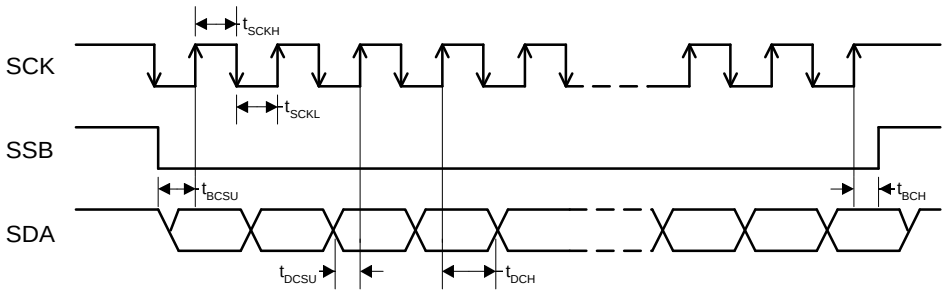


FIGURE 10. Data interface timing(SPI)

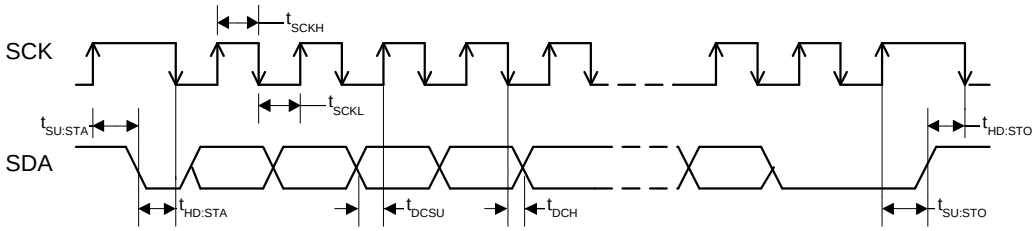


FIGURE 11. Data interface timing(I²C)

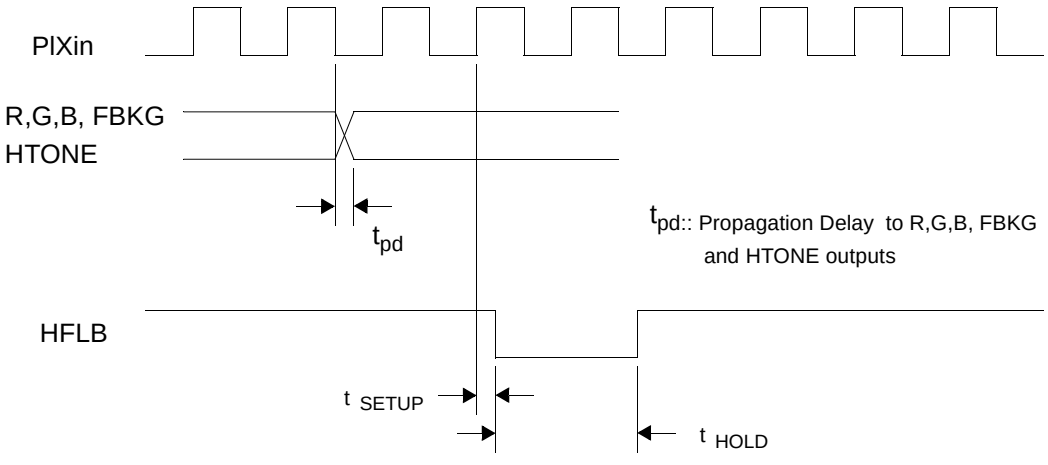
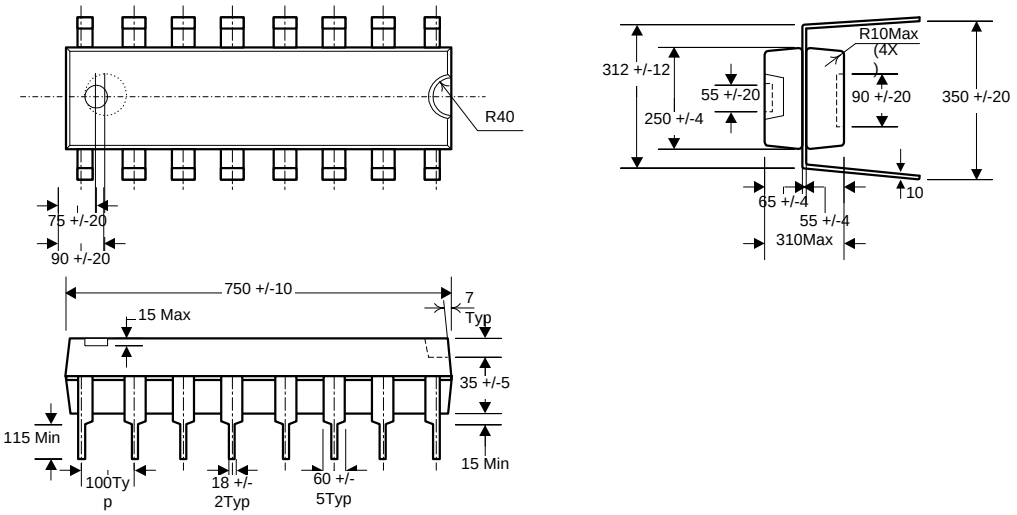


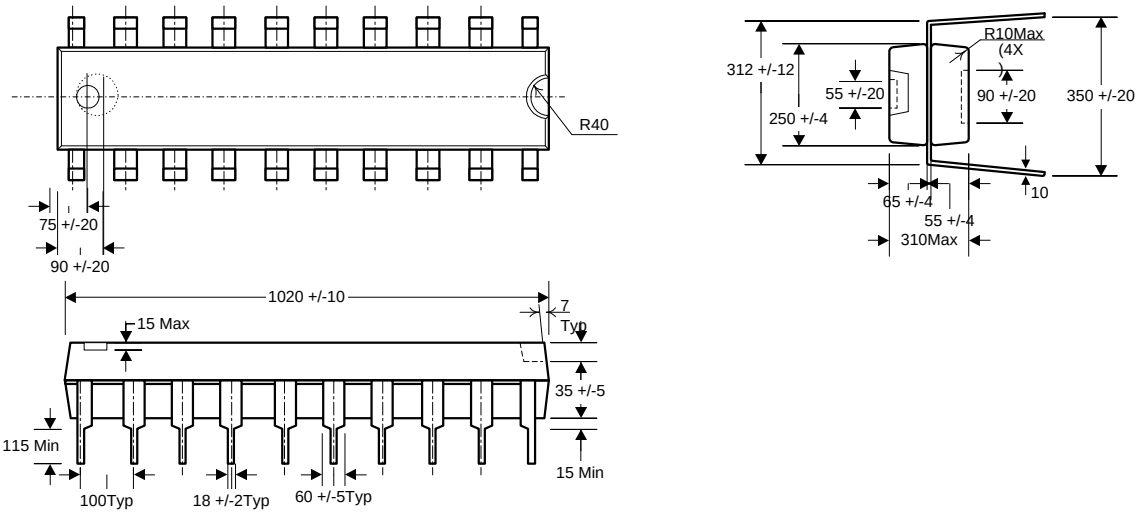
FIGURE 12. Output and HFLB Timing to Pixel Clock

9.0 PACKAGE DIMENSION

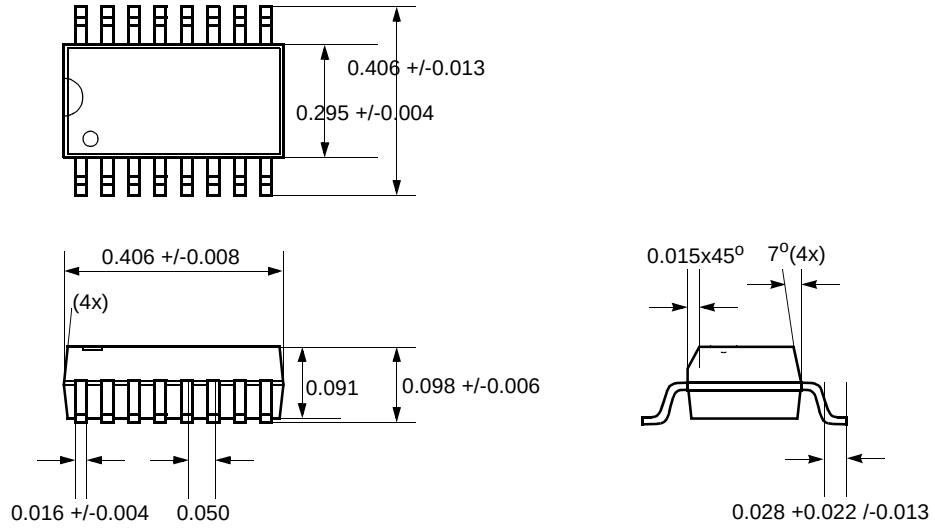
9.1 16 Pin PDIP 300mil



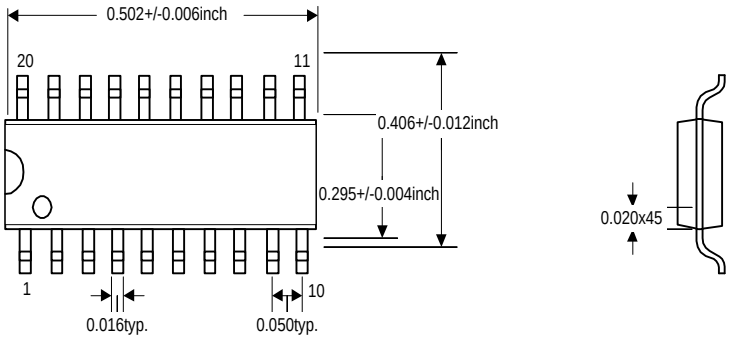
9.2 20 Pin PDIP 300mil



9.3 16 Pin SOP 300mil



9.4 20 Pin SOP 300 mil



10.0 CHARACTERS AND SYMBOLS PATTERN

Please see the attachment.

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