MX27L1000

1M-BIT [128Kx8] LOW VOLTAGE OPERATION CMOS EPROM

FEATURES

- 128K x 8 organization
- Wide power supply range, 2.7V DC to 3.6VDC
- +12.5V programming voltage
- Fast access time:90/120/150/200/250 ns
- Totally static operation
- Completely TTL compatible
- Operating current: 20mA @3.6V, 5MHz
- Standby current: 10uA
- Package type:
  - 32 pin plastic DIP
  - 32 pin SOP
  - 32 pin TSOP
  - 32 pin PLCC

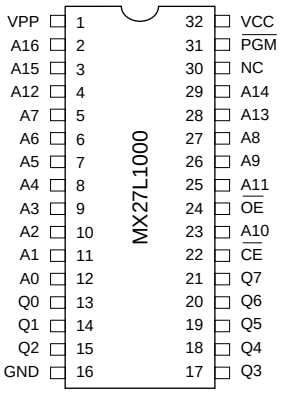
GENERAL DESCRIPTION

The MX27L1000 is a 1M-bit, One Time Programmable Read Only Memory. It isorganized as 128K words by 8 bits per word, opeates from a single 2.7 to 3.6 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requirin a single pulse. For programming outside from the system, existing EPROM programmers may be used. The MX27L1000 supports a intelligent fast programming algorithm which can result in programming time of less than thirty seconds.

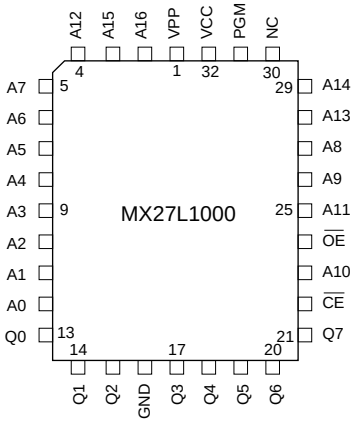
This EPROM is packaged in industry standard 32 pin dual-in-line packages,32 lead SOP , 32 lead PLCC, and 32 lead TSOP packages.

PIN CONFIGURATIONS

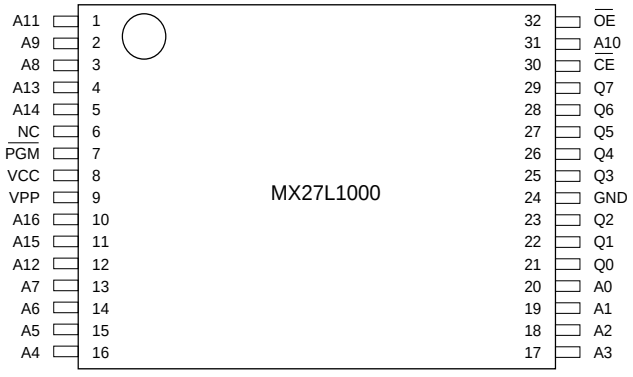
32 PDIP/SOP



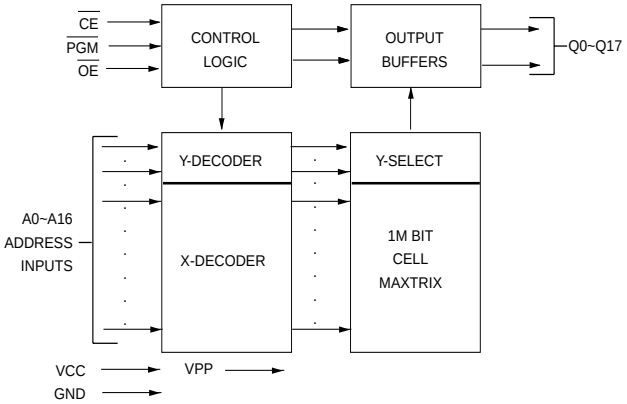
32 PLCC



32 TSOP



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A16	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{PGM}$	Programmable Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin
GND	Ground Pin

FUNCTIONAL DESCRIPTION

THE PROGRAMMING OF THE MX27L1000

When the MX27L1000 is delivered, or it is erased, the chip has all 1M bits in the "ONE" or HIGH state. "ZERO" are loaded into the MX27L1000 through the procedure of programming.

For programming, the data to be programmed is applied with 8 bits in parallel to the data pins.

VCC must be applied simultaneously or before VPP, and removed simultaneously or after VPP. When programming an MXIC EPROM, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

FAST PROGRAMMING

The device is set up in the fast programming mode when the programming voltage VPP = 12.75V is applied, with VCC = 6.25 V and $\overline{PGM}$ = VIL(or $\overline{OE}$ = VIH) (Algorithm is shown in Figure 1). The programming is achieved by applying a single TTL low level 100us pulse to the $\overline{PGM}$ input after addresses and data line are stable. If the data is not verified, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the device. When the programming mode is completed, the data in all address is verified at VCC = VPP = 5V ± 10%.

PROGRAM INHIBIT MODE

Programming of multiple MX27L1000s in parallel with different data is also easily accomplished by using the Program Inhibit Mode. Except for $\overline{CE}$ and $\overline{OE}$, all like inputs of the parallel MX27L1000 may be common. A TTL low-level program pulse applied to an MX27L1000 $\overline{CE}$ input with VPP = 12.5 ± 0.5 V and $\overline{PGM}$ LOW will program that MX27L1000. A high-level $\overline{CE}$ input inhibits the other MX27L1000s from being programmed.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. The verification should be performed with $\overline{OE}$ and $\overline{CE}$ at VIL, $\overline{PGM}$ at VIH, and VPP at its programming voltage.

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25℃ ± 5℃ ambient temperature range that is required when programming the MX27L1000.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX27L1000, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (Q7) defined as the parity bit.

READ MODE

The MX27L1000 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tQE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX27L1000 has a CMOS standby mode which reduces the maximum VCC current to 10 uA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX27L1000 also has a TTL-standby mode which reduces the maximum VCC current to 0.25mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

TWO-LINE OUTPUT CONTROL FUNCTION

To accommodate multiple memory connections, a two-line control function is provided to allow for:

1. Low memory power dissipation,
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device-selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

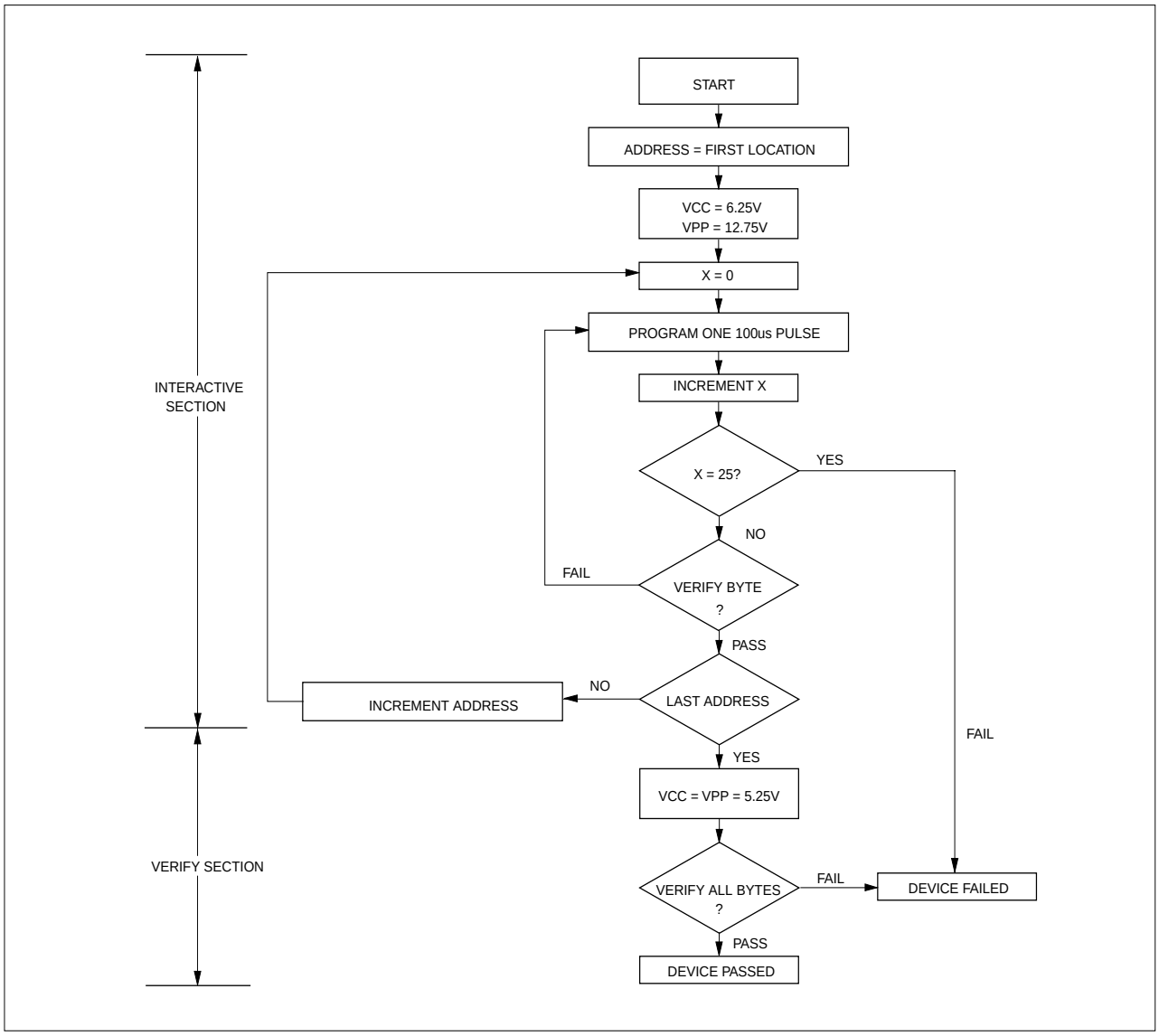
During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between Vcc and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between Vcc and GND for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

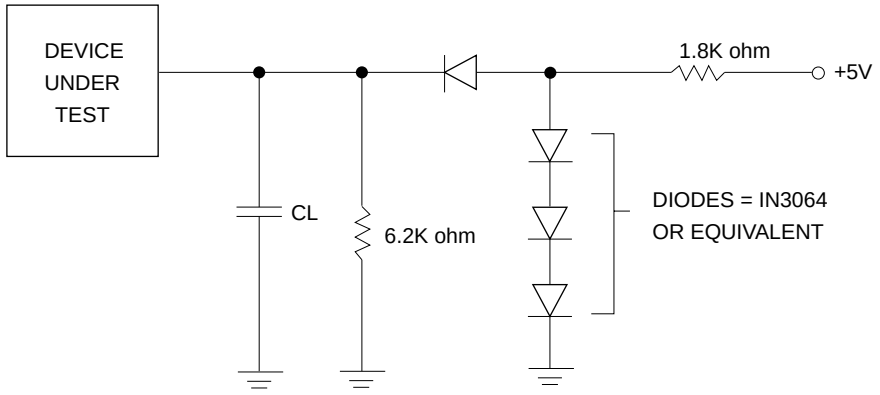
	PINS						
MODE	**$\overline{CE}$**	**$\overline{OE}$**	**$\overline{PGM}$**	**A0**	**A9**	**VPP**	**OUTPUTS**
Read	VIL	VIL	X	X	X	VCC	DOUT
Output Disable	VIL	VIH	X	X	X	VCC	High Z
Standby (TTL)	VIH	X	X	X	X	VCC	High Z
Standby (CMOS)	VCC ± 0.3V	X	X	X	X	VCC	High Z
Program	VIL	VIH	VIL	X	X	VPP	DIN
Program Verify	VIL	VIL	VIH	X	X	VPP	DOUT
Program Inhibit	VIH	X	X	X	X	VPP	High Z
Manufacturer Code(3)	VIL	VIL	X	VIL	VH	VCC	C2H
Device Code(3)	VIL	VIL	X	VIH	VH	VCC	0EH

NOTES:
1. VH = 12.0 V ± 0.5 V
2. X = Either VIH or VIL
3. A1 - A8 = A10 - A16 = VIL(For auto select)
4. See DC Programming Characteristics for VPP voltage during programming.

FIGURE 1. FAST PROGRAMMING FLOW CHART

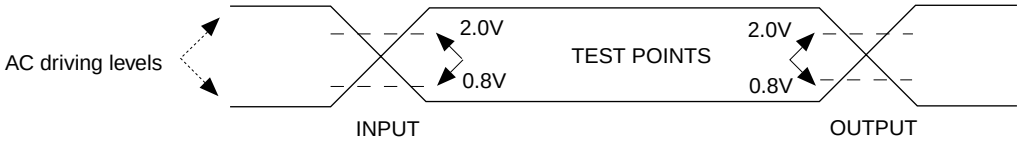


SWITCHING TEST CIRCUITS



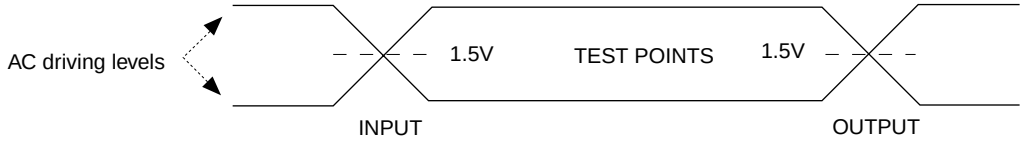
CL = 100 pF including jig capacitance
CL = 30 pF including jig capacitance for 90/120ns

SWITCHING TEST WAVEFORMS



AC TESTING: AC driving levels are 2.4V/0.4V for both commercial grade and industrial grade.
Input pulse rise and fall times are ≤ 10ns.

SWITCHING TEST WAVEFORMS (For Speed 90/120ns)



AC TESTING: AC driving levels are 3.0V/0V for both commercial grade and industrial grade.
Input pulse rise and fall times are ≤ 10ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC+0.5V
VCC to Ground Potential	-0.5V to 7.0V
V9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC/AC Operating Conditions for Read Operation

		MX27L1000				
		-90	-12	-15	-20	-25
Operating Temperature	Commercial	0℃ to 70℃	0℃ to 70℃	0℃ to 70℃	0℃ to 70℃	0℃ to 70℃
	Industrial	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃
Vcc Power Supply		2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V	2.7V to 3.6V

DC CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	VCC - 0.3		V	IOH = -100uA VCC=3.0V
VOL	Output Low Voltage		0.3	V	IOL = 2.1mA, VCC = 3.0V
VIH	Input High Voltage	2.0	Vcc + 0.5	V	
VIL	Input Low Voltage	-0.3	0.6	V	2.7V < VCC < 3.6V
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 3.6V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 3.6V
ICC3	VCC Power-Down Current		10	uA	$\overline{CE}$ = VCC ± 0.3V
ICC2	VCC Standby Current		0.25	mA	$\overline{CE}$ = VIH
ICC1	VCC Active Current		20	mA	$\overline{CE}$ = VIH, f=5MHz, Iout = OmA, Vcc=3.6V
IPP	Supply Current Read		10	uA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = VCC

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

AC CHARACTERISTICS

		27L1000-90		27L1000-12		27L1000-15		27L1000-20		27L1000-25			
Symbol	**PARAMETER**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**MIN.**	**MAX.**	**UNIT**	**CONDITIONS**
tACC	Address to Output Delay		90		120		150		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = VIL
tCE	Chip Enable to Output Delay		90		120		150		200		250	ns	$\overline{OE}$ = VIL
tOE	Output Enable to Output Delay		40		50		70		100		120	ns	$\overline{CE}$ = VIL
tDF	$\overline{OE}$ High to Output Float, or $\overline{CE}$ High to Output Float	0	30	0	40	0	50	0	60	0	70	ns	
tOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ which ever occurred first	0		0		0		0		0		ns	

DC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

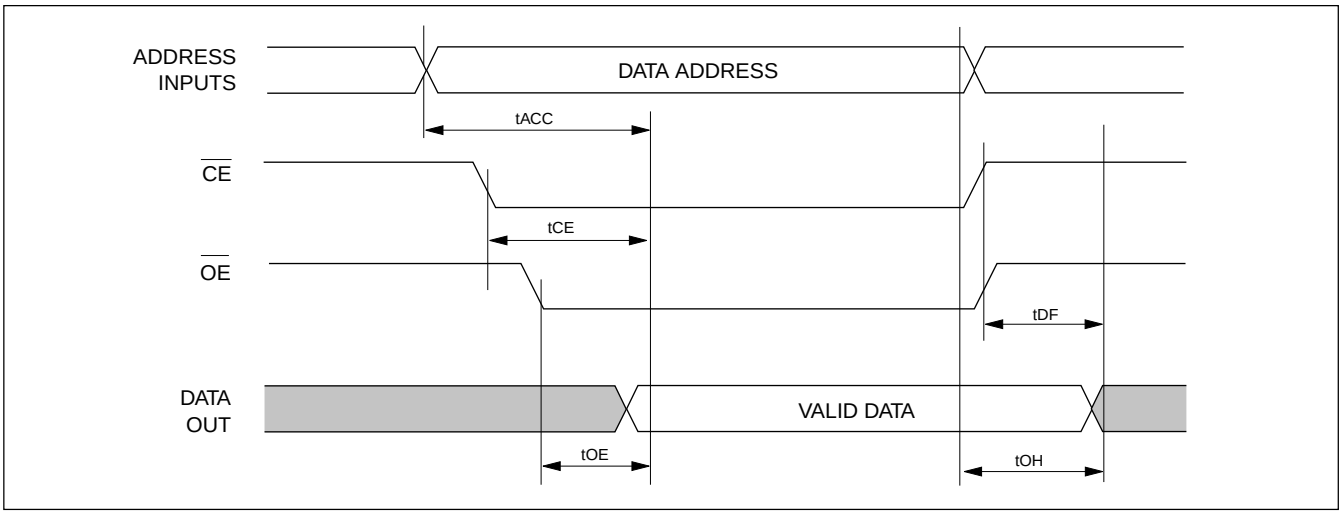
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VOH	Output High Voltage	2.4		V	IOH = -0.10mA
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VIL	Input Low Voltage	-0.3	0.8	V	
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 3.6V
VH	A9 Auto Select Voltage	11.5	12.5	V	
ICC3	VCC Supply Current (Program & Verify)		50	mA	
IPP2	VPP Supply Current(Program)		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$ = VIH
VCC1	Fast Programming Supply Voltage	6.00	6.50	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

AC PROGRAMMING CHARACTERISTICS TA = 25°C ± 5°C

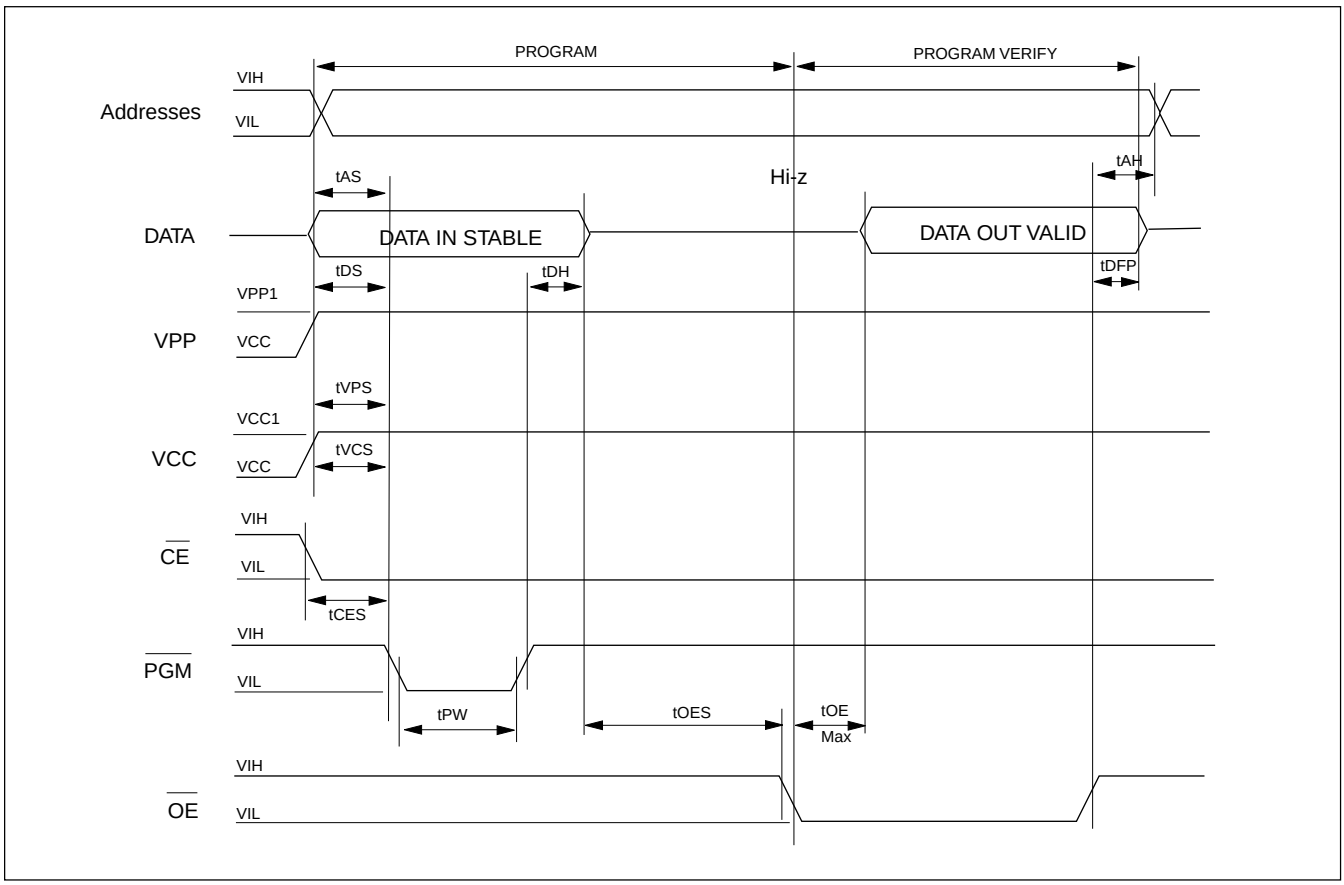
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tAS	Address Setup Time	2.0		us
tOES	OE Setup Time	2.0		us
tDS	Data Setup Time	2.0		us
tAH	Address Hold Time	0		us
tDH	Data Hold Time	2.0		us
tDFP	Out put Enable to Output Float Delay	0	130	ns
tVPS	VPP Setup Time	2.0		us
tPW	PGM Program Pulse Width	95	105	us
tVCS	VCC Setup Time	2.0		us
tCES	CE Setup Time	2.0		us
tOE	Data valid from OE		150	ns

WAVEFORMS

READ CYCLE



FAST PROGRAMMING ALGORIHTM WAVEFORMS

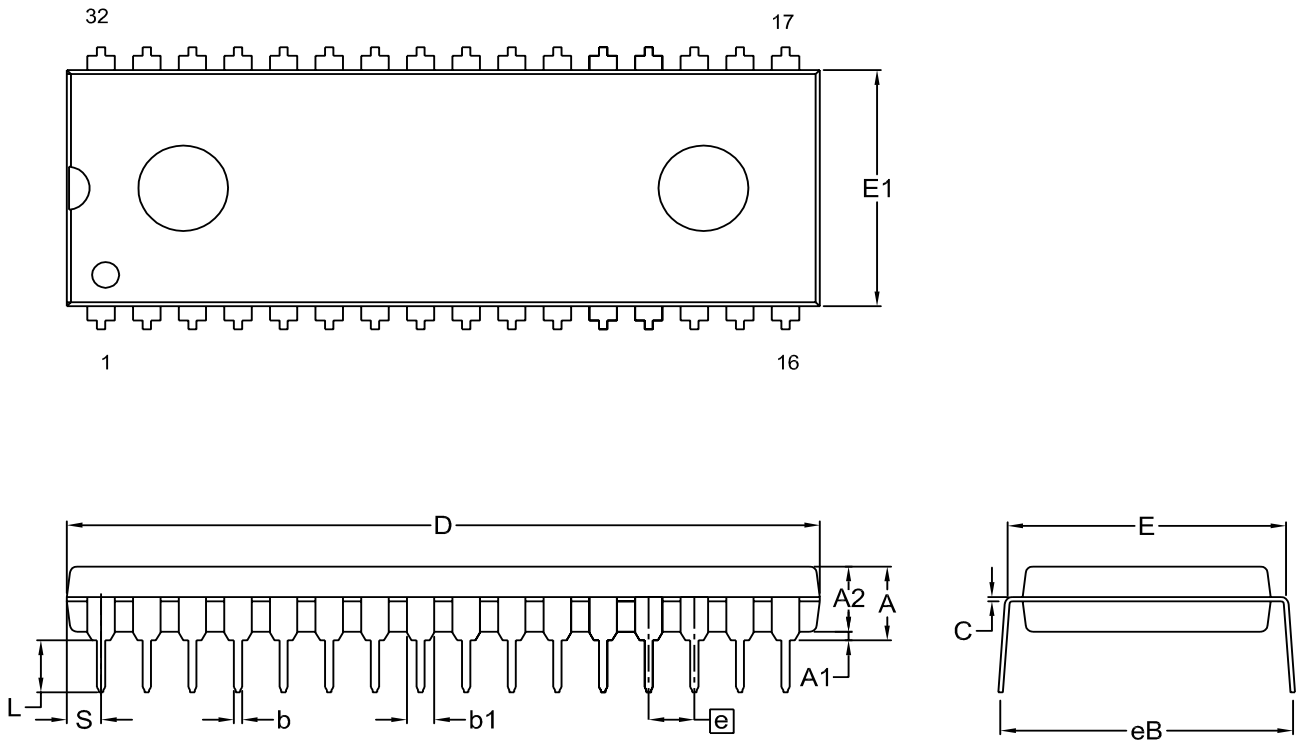


ORDER INFORMATION

PART NO.	ACCESS TIME(ns)	OPERATING CURRENT MAX.(mA)	STANDBY CURRENT MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX27L1000PC-25	250	30	10	0℃ to 70℃	32 Pin DIP
MX27L1000QC-25	250	20	10	0℃ to 70℃	32 Pin PLCC
MX27L1000MC-25	250	30	10	0℃ to 70℃	32 Pin SOP
MX27L1000TC-25	250	30	10	0℃ to 70℃	32 Pin TSOP
MX27L1000PC-20	200	30	10	0℃ to 70℃	32 Pin DIP
MX27L1000QC-20	200	20	10	0℃ to 70℃	32 Pin PLCC
MX27L1000MC-20	200	30	10	0℃ to 70℃	32 Pin SOP
MX27L1000TC-20	200	30	10	0℃ to 70℃	32 Pin TSOP
MX27L1000PC-15	150	30	10	0℃ to 70℃	32 Pin DIP
MX27L1000QC-15	150	20	10	0℃ to 70℃	32 Pin PLCC
MX27L1000MC-15	150	30	10	0℃ to 70℃	32 Pin SOP
MX27L1000TC-15	150	30	10	0℃ to 70℃	32 Pin TSOP
MX27L1000PC-12	120	30	10	0℃ to 70℃	32 Pin DIP
MX27L1000QC-12	120	20	10	0℃ to 70℃	32 Pin PLCC
MX27L1000MC-12	120	30	10	0℃ to 70℃	32 Pin SOP
MX27L1000TC-12	120	30	10	0℃ to 70℃	32 Pin TSOP
MX27L1000PC-90	90	30	10	0℃ to 70℃	32 Pin DIP
MX27L1000QC-90	90	20	10	0℃ to 70℃	32 Pin PLCC
MX27L1000MC-90	90	30	10	0℃ to 70℃	32 Pin SOP
MX27L1000TC-90	90	30	10	0℃ to 70℃	32 Pin TSOP
MX27L1000PI-25	250	30	10	-40℃ to 85℃	32 Pin DIP
MX27L1000QI-25	250	20	10	-40℃ to 85℃	32 Pin PLCC
MX27L1000MI-25	250	30	10	-40℃ to 85℃	32 Pin SOP
MX27L1000TI-25	250	30	10	-40℃ to 85℃	32 Pin TSOP
MX27L1000PI-20	200	30	10	-40℃ to 85℃	32 Pin DIP
MX27L1000QI-20	200	20	10	-40℃ to 85℃	32 Pin PLCC
MX27L1000MI-20	200	30	10	-40℃ to 85℃	32 Pin SOP
MX27L1000TI-20	200	30	10	-40℃ to 85℃	32 Pin TSOP
MX27L1000PI-15	150	30	10	-40℃ to 85℃	32 Pin DIP
MX27L1000QI-15	150	20	10	-40℃ to 85℃	32 Pin PLCC
MX27L1000MI-15	150	30	10	-40℃ to 85℃	32 Pin SOP
MX27L1000TI-15	150	30	10	-40℃ to 85℃	32 Pin TSOP
MX27L1000PI-12	120	30	10	-40℃ to 85℃	32 Pin DIP
MX27L1000QI-12	120	20	10	-40℃ to 85℃	32 Pin PLCC
MX27L1000MI-12	120	30	10	-40℃ to 85℃	32 Pin SOP
MX27L1000TI-12	120	30	10	-40℃ to 85℃	32 Pin TSOP
MX27L1000PI-90	90	30	10	-40℃ to 85℃	32 Pin DIP
MX27L1000QI-90	90	20	10	-40℃ to 85℃	32 Pin PLCC
MX27L1000MI-90	90	30	10	-40℃ to 85℃	32 Pin SOP
MX27L1000TI-90	90	30	10	-40℃ to 85℃	32 Pin TSOP

PACKAGE INFORMATION

Title: Package Outline for PDIP 32L(600MIL)

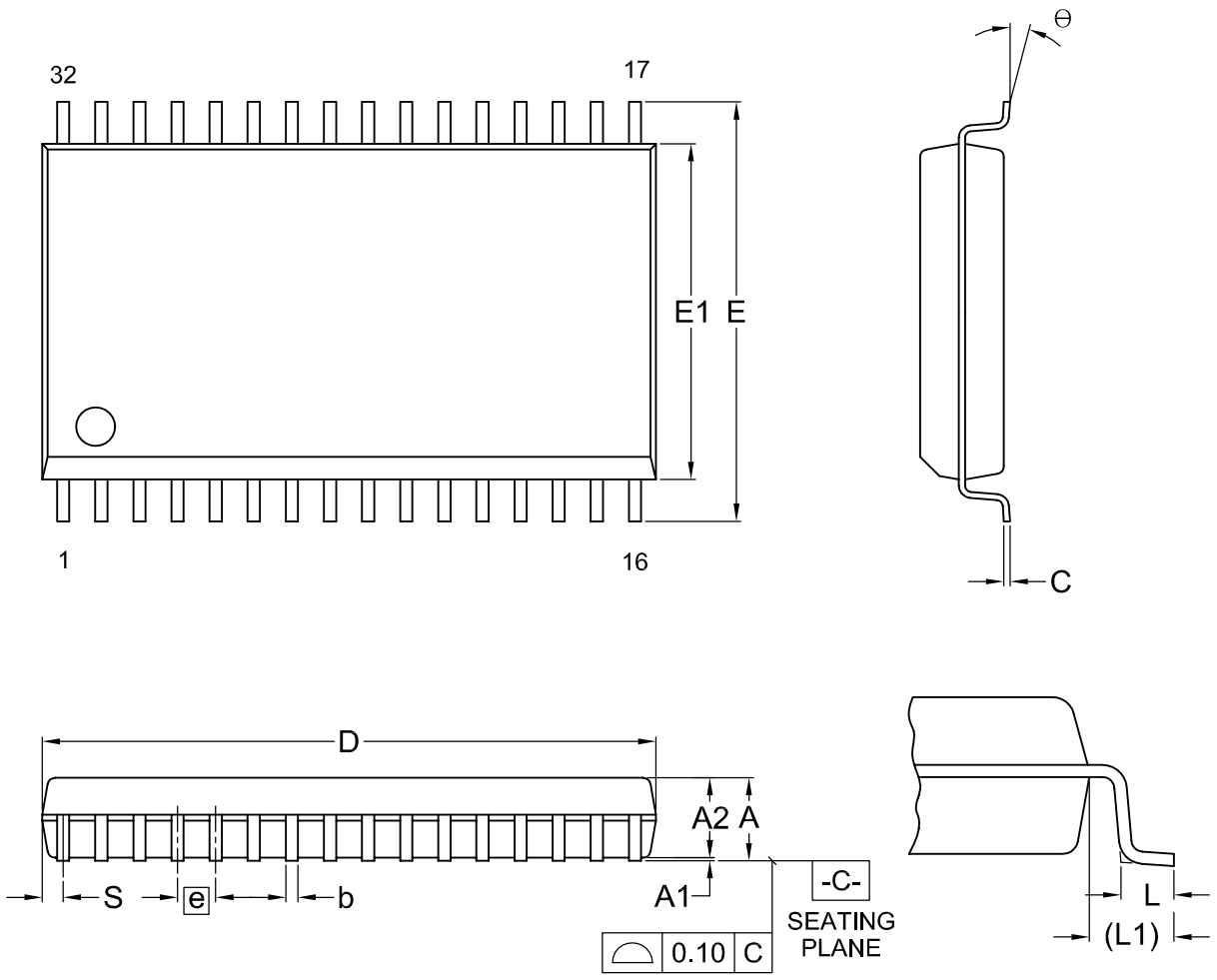


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.38	3.73	0.38	1.14	0.20	41.78	15.11	13.84		15.75	2.92	1.65
	Nom.	---	---	3.94	0.46	1.27	0.25	41.91	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	42.04	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.015	0.147	0.015	0.045	0.008	1.645	0.595	0.545		0.620	0.115	0.065
	Nom.	---	---	0.155	0.018	0.050	0.010	1.650	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	1.655	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.2	6				11-19-'02

Title: **Package Outline for SOP 32L (450MIL)**

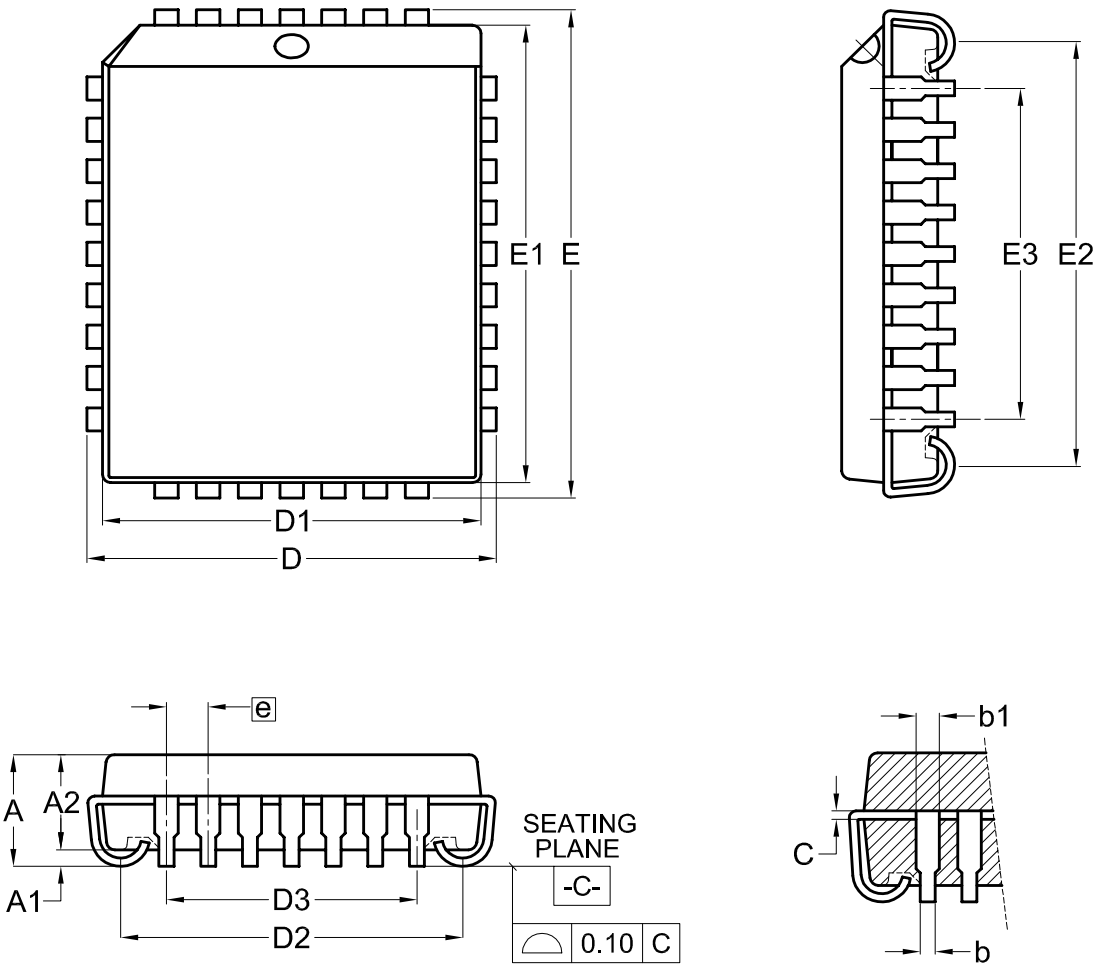


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	20.32	13.92	11.18		0.56	1.20	0.58	0
	Nom.	---	0.15	2.69	0.41	0.20	20.45	14.12	11.30	1.27	0.76	1.40	0.70	5
	Max.	3.00	0.20	2.80	0.51	0.25	20.57	14.32	11.43		0.96	1.60	0.83	8
Inch	Min.	---	0.004	0.102	0.014	0.006	0.800	0.548	0.440		0.022	0.047	0.023	0
	Nom.	---	0.006	0.106	0.016	0.008	0.805	0.556	0.445	0.050	0.030	0.055	0.028	5
	Max.	0.118	0.008	0.110	0.020	0.010	0.810	0.564	0.450		0.038	0.063	0.033	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404	4	MO-099			09-24-'02

Title: **Package Outline for 32L PLCC**

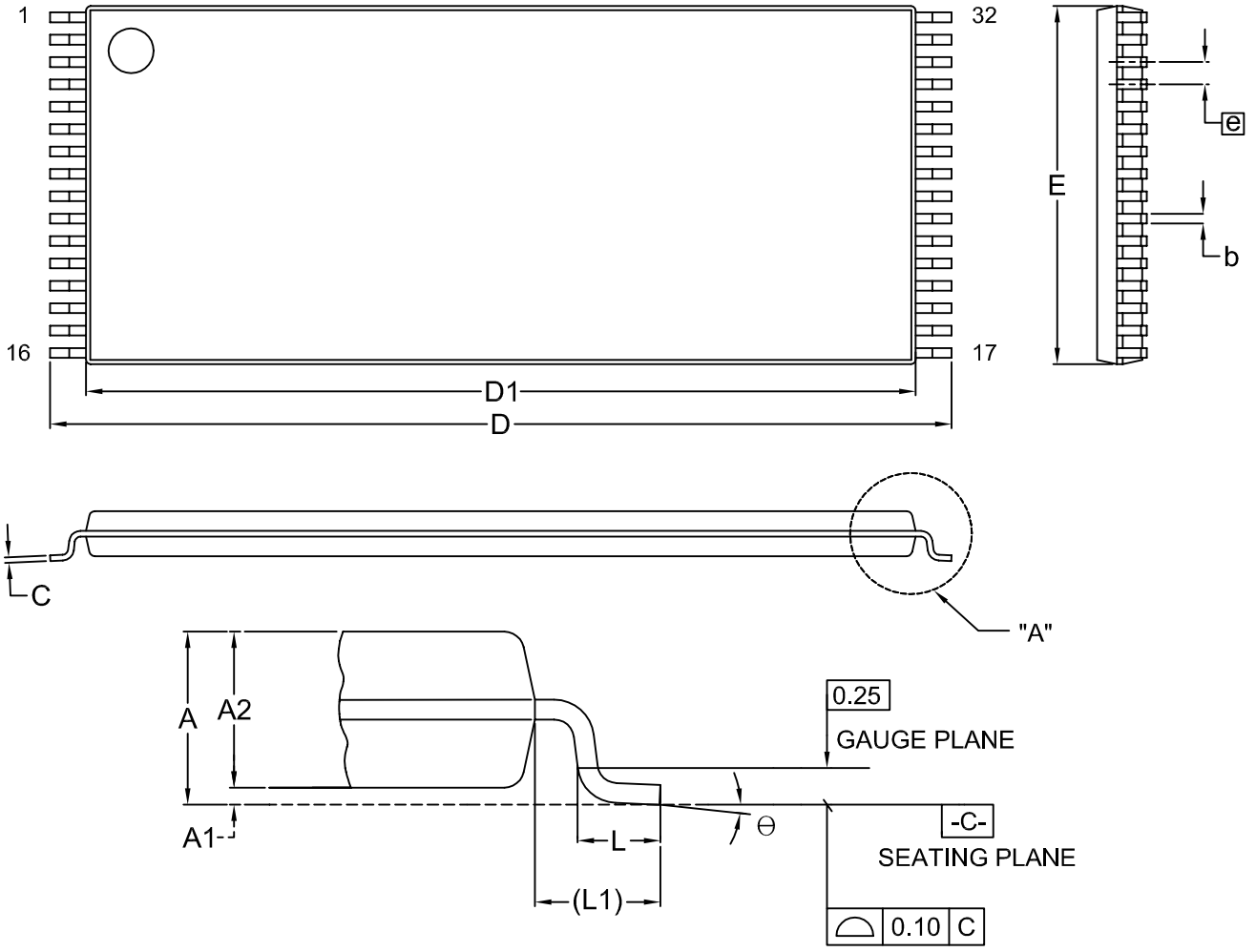


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	—	0.38	2.69	0.38	0.61	0.20	12.32	11.36	10.11		14.86	13.98	12.65		
	Nom.	—	0.58	2.79	0.46	0.71	0.25	12.45	11.43	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.81	2.89	0.54	0.81	0.30	12.58	11.50	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.447	0.398		0.585	0.550	0.498		
	Nom.	---	0.023	0.110	0.018	0.028	0.010	0.490	0.450	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.032	0.114	0.021	0.032	0.012	0.495	0.453	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	6	MS-016			08-15-'03

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	8	MO-142			09-24-'02

REVISION HISTORY

Revision No.	Description	Page	Date
2.4	Page 3:Mode Select Table : VPP pin-"VCC" instead of " X".		9/24/1996
	Revise SWITCHING TEST WAVEFORM, VOL=0.6V to VOL=0.8V.		
3.0	Eliminate Interactive Programming Mode.		6/18/1997
3.1	IPP 100uA --> 10uA		8/07/1997
3.2	Change TSOP Orientation		4/09/1998
3.3	Add speed 90/120ns	P1,9,10	OCT/13/1999
	Change VIH/VIL, VOH/VOL for 90/120ns	P5	
	Change CL to 30pF for 90/120ns	P5	
3.4	Cancel 32pin ceramic DIP Package	P1,2,9,11	FEB/25/2000
3.5	To modify Package Information	P10~13	JUL/19/2001
3.6	Cancel "Ultraviolet Erasable" wording in General Description	P1	AUG/20/2001
3.7	To modify Package Information	P10~13	NOV/19/2002
3.8	To modify 32-PLCC package information	P12	AUG/26/2003
	A1: from 0.50mm(0.020 inch)/nom. to 0.58mm(0.023 inch)/nom.		
	from 0.66mm(0.026 inch)/nom. to 0.81mm(0.032 inch)/nom.		

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