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N08T1630CxB

8Mb Ultra-Low Power Asynchronous CMOS SRAM

512Kx16 bit

Overview

The N08T1630CxB is an integrated memory device containing a low power 8 Mbit SRAM built using a self-refresh DRAM array organized as 512,288 words by 16 bits. It is designed to be identical in operation and interface to standard 6T SRAMS. The device is designed for low standby and operating current and includes a power-down feature to automatically enter standby mode. The device operates with two chip enable ($\overline{CE1}$ and CE2) controls and output enable ($\overline{OE}$) to allow for easy memory expansion. Byte controls ($\overline{UB}$ and $\overline{LB}$) allow the upper and lower bytes to be accessed independently and can also be used to deselect the device. The N08T1630CxB is optimal for various applications where low-power is critical such as battery backup and hand-held devices. The device can operate over a very wide temperature range of -40^{o}C to +85^{o}C and is available in JEDEC standard BGA and TSOP2 packages compatible with other standard 512Kb x 16 SRAMs.

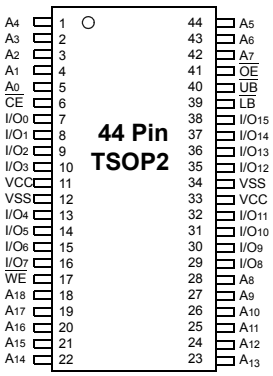
Features

- **Single Wide Power Supply Range**
  2.7 to 3.6 Volts
- **Very low standby current**
  70µA at 3.0V (Max)
- **Very low operating current**
  2.0mA at 3.0V and 1µs (Typical)
- **Simple memory control**
  Dual Chip Enables ($\overline{CE1}$ and CE2)
  Byte control for independent byte operation
  Output Enable ($\overline{OE}$) for memory expansion
- **Very fast access time**
  55ns address access option
  30ns $\overline{OE}$ access time
- **Automatic power down to standby mode**
- **TTL compatible three-state output driver**
- **Green package option for TSOP and BGA**

Product Family

Part Number	Package Type	Operating Temperature	Power Supply (Vcc)	Speed	Standby Current (I_{SB}), Max @ 3.0V	Operating Current (Icc), Max
N08T1630C2BZ	48 - BGA	-40^{o}C to +85^{o}C	2.7V - 3.6V	55/70ns @ 2.7V	70 µA	3 mA @ 1MHz
N08T1630C2BZ2	Green 48 - BGA					
N08T1630C1BT	44- TSOP2					
N08T1630C1BT2	Green 44- TSOP2					

Pin Configuration (Top View)



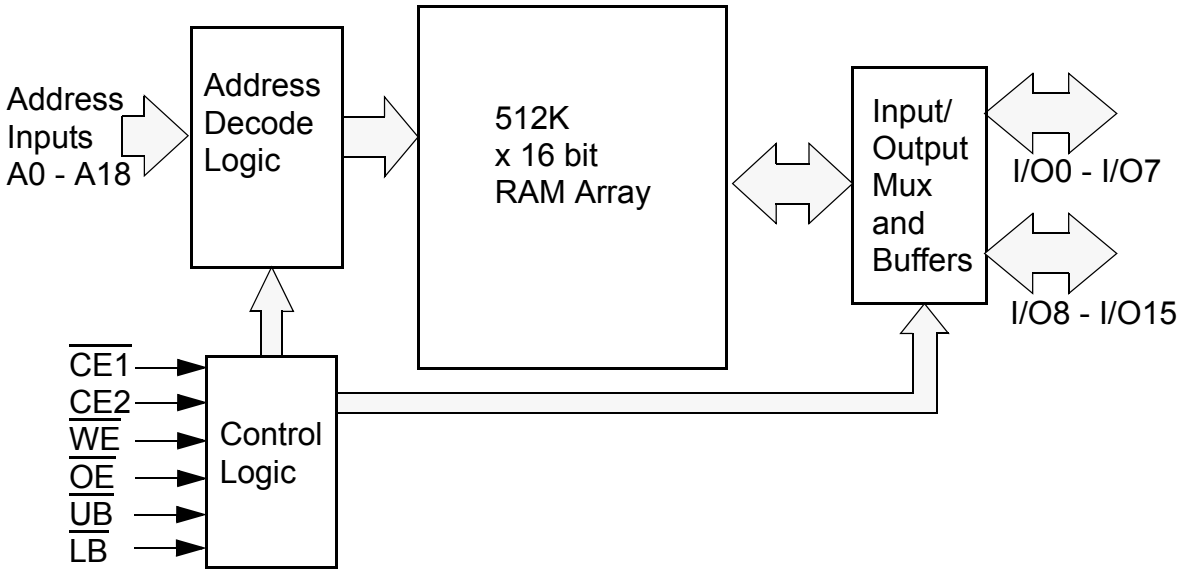
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	V_{SS}	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

48 Ball BGA
6 x 8 mm

Pin Descriptions

Pin Name	Pin Function
A_0-A_{18}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input (BGA only)
$\overline{OE}$	Output Enable Input
$\overline{LB}$	Lower Byte Enable Input
$\overline{UB}$	Upper Byte Enable Input
I/O_0-I/O_{15}	Data Inputs/Outputs
V_{CC}	Power
V_{SS}	Ground
NC	Not Connected

Functional Block Diagram



Functional Description

$\overline{CE1}$	CE2[1]	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O_0 - I/O_{15}[2]	MODE	POWER
H	X	X	X	X	X	High Z	Standby[3]	Standby
X	L	X	X	X	X	High Z	Standby[3]	Standby
L	H	X	X	H	H	High Z	Standby[3]	Standby
L	H	L	X[4]	L[2]	L[2]	Data In	Write	Active
L	H	H	L	L[2]	L[2]	Data Out	Read	Active
L	H	H	H	L[2]	L[2]	High Z	Active	Active

1. CE2 only applies to BGA package.
2. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - I/O_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown.
3. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
4. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.

Capacitance[1]

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

1. These parameters are verified in device characterization and are not 100% tested

Absolute Maximum Ratings[1]

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to 4.5	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	–40 to 125	°C
Operating Temperature	T_A	-40 to +85	°C
Soldering Temperature and Time	T_{SOLDER}	260°C, 10sec	°C

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Characteristics (Over Specified Temperature Range)

Item	Symbol	Test Conditions	Min.	Typ[1]	Max	Unit
Supply Voltage	V_{CC}		2.7	3.0	3.6	V
Input High Voltage	V_{IH}		2.2		V_{CC}+0.3	V
Input Low Voltage	V_{IL}		–0.3		0.6	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA	V_{CC}–0.4			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA			0.4	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}			0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled			0.5	µA
Read/Write Operating Supply Current @ 1 µs Cycle Time[2]	I_{CC1}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		3.0	5.0	mA
Read/Write Operating Supply Current @ 70 ns Cycle Time[2]	I_{CC2}	V_{CC}=3.6 V, V_{IN}=V_{IH} or V_{IL} Chip Enabled, I_{OUT} = 0		12.0	25.0	mA
Maximum Standby Current	I_{SB1}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, V_{CC} = 3.0 V			70.0	µA
Maximum Standby Current	I_{SB2}	V_{IN} = V_{CC} or 0V Chip Disabled t_A= 85°C, V_{CC} = 3.6 V			80.0	µA

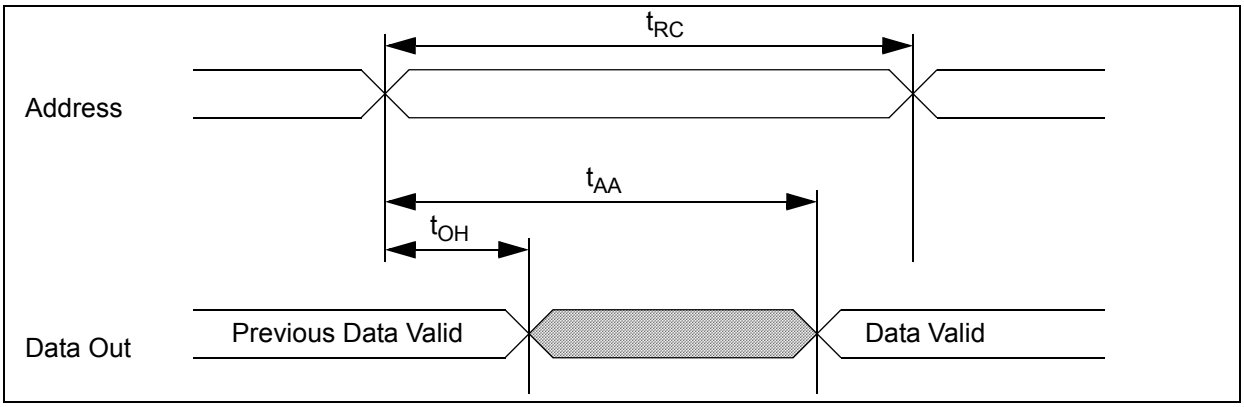
1. Typical values are measured at Vcc=Vcc Typ., T_A=25°C and not 100% tested.

2. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

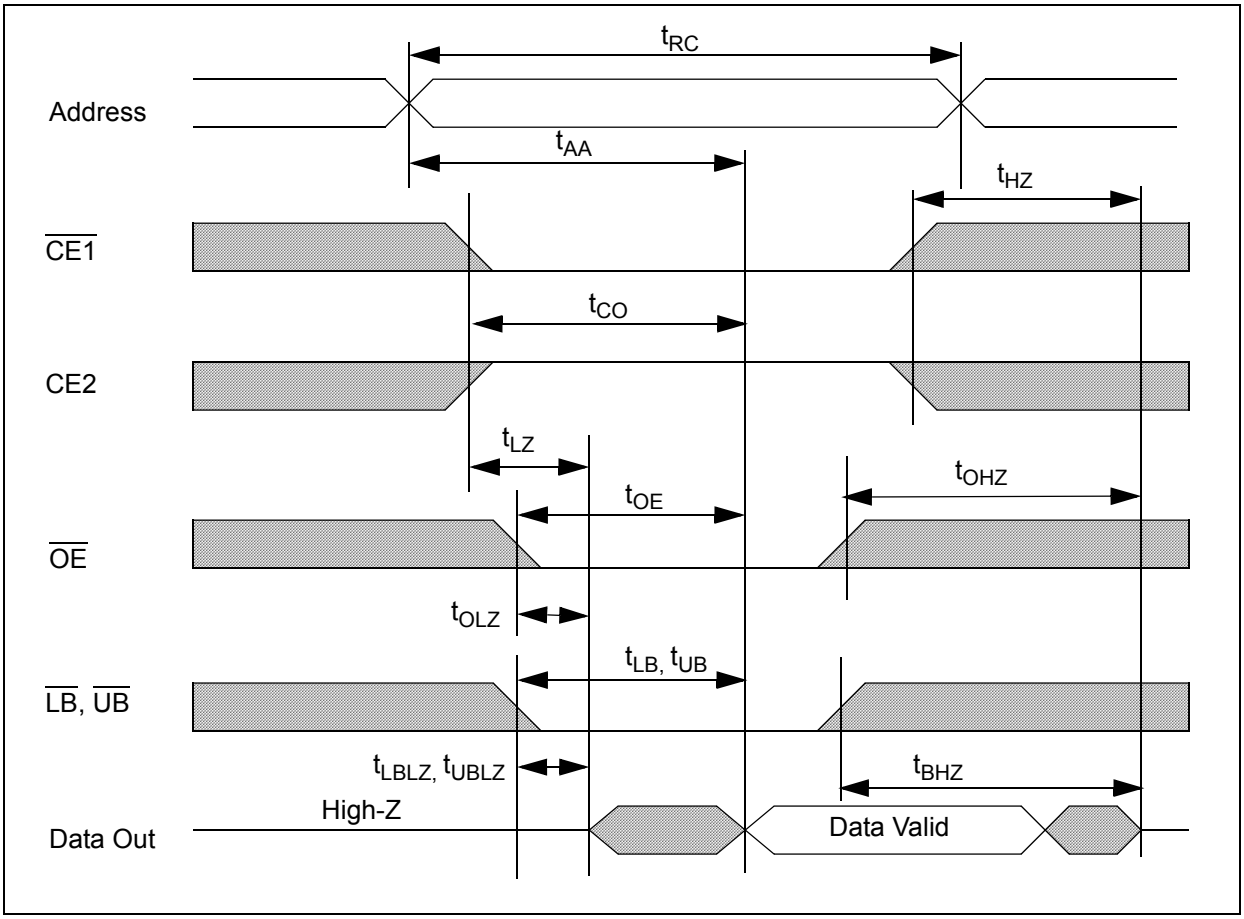
Timing

Item	Symbol	-55		-70		Units
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	55		70		ns
Address Access Time	t_{AA}		55		70	ns
Chip Enable to Valid Output	t_{CO}		55		70	ns
Output Enable to Valid Output	t_{OE}		30		35	ns
Byte Select to Valid Output	t_{LB}, t_{UB}		55		70	ns
Chip Enable to Low-Z output	t_{LZ}	5		5		ns
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns
Byte Select to Low-Z Output	t_{BLZ}	5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	20	0	25	ns
Output Disable to High-Z Output	t_{OHZ}	0	20	0	25	ns
Byte Select Disable to High-Z Output	t_{BHZ}	0	20	0	25	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Write Cycle Time	t_{WC}	55		70		ns
Chip Enable to End of Write	t_{CW}	45		55		ns
Address Valid to End of Write	t_{AW}	45		55		ns
Byte Select to End of Write	t_{BW}	45		55		ns
Write Pulse Width	t_{WP}	45		55		ns
Address Setup Time	t_{AS}	0		0		ns
Write Recovery Time	t_{WR}	0		0		ns
Write to High-Z Output	t_{WHZ}		25		25	ns
Data to Write Time Overlap	t_{DW}	40		40		ns
Data Hold from Write Time	t_{DH}	0		0		ns
End Write to Low-Z Output	t_{OW}	5		5		ns

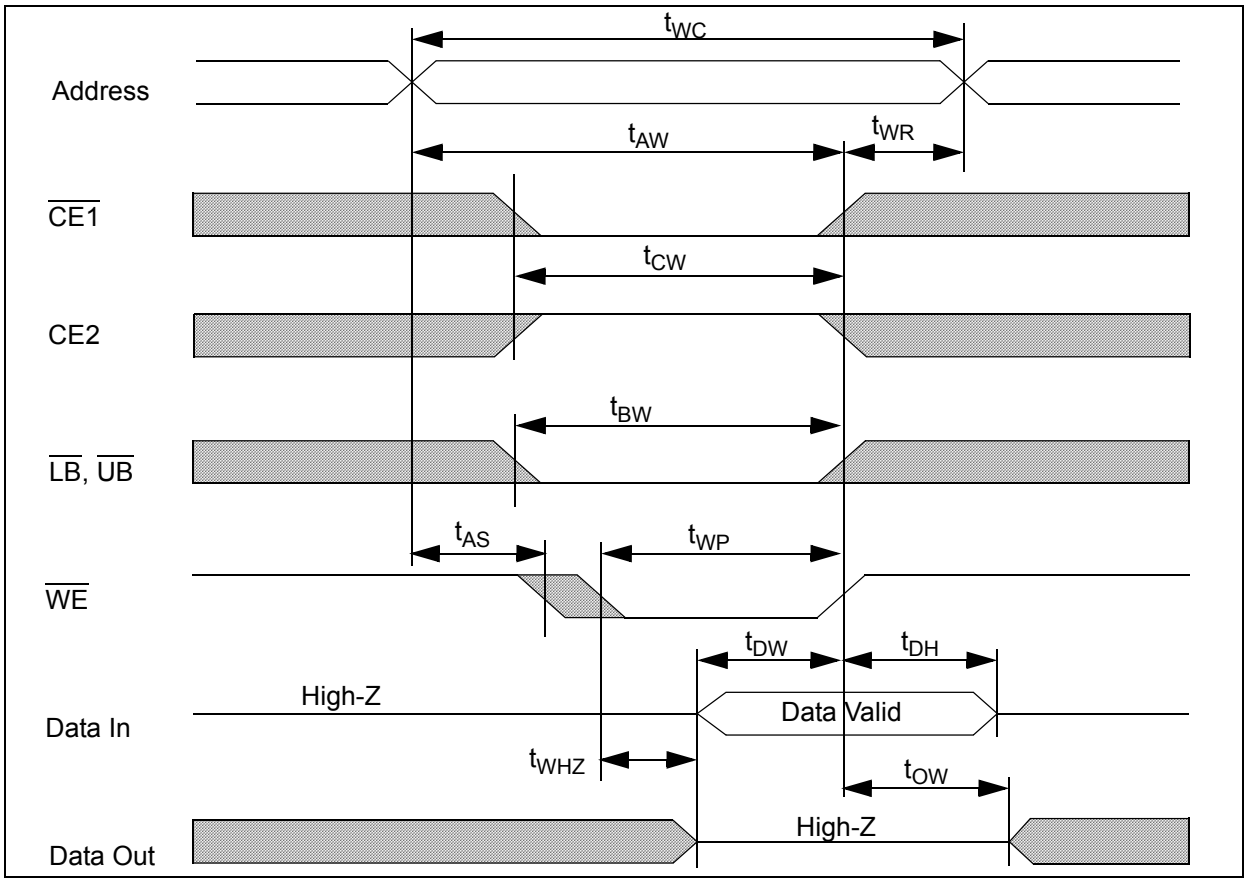
Timing of Read Cycle ($\overline{CE1}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = CE2 = V_{IH})



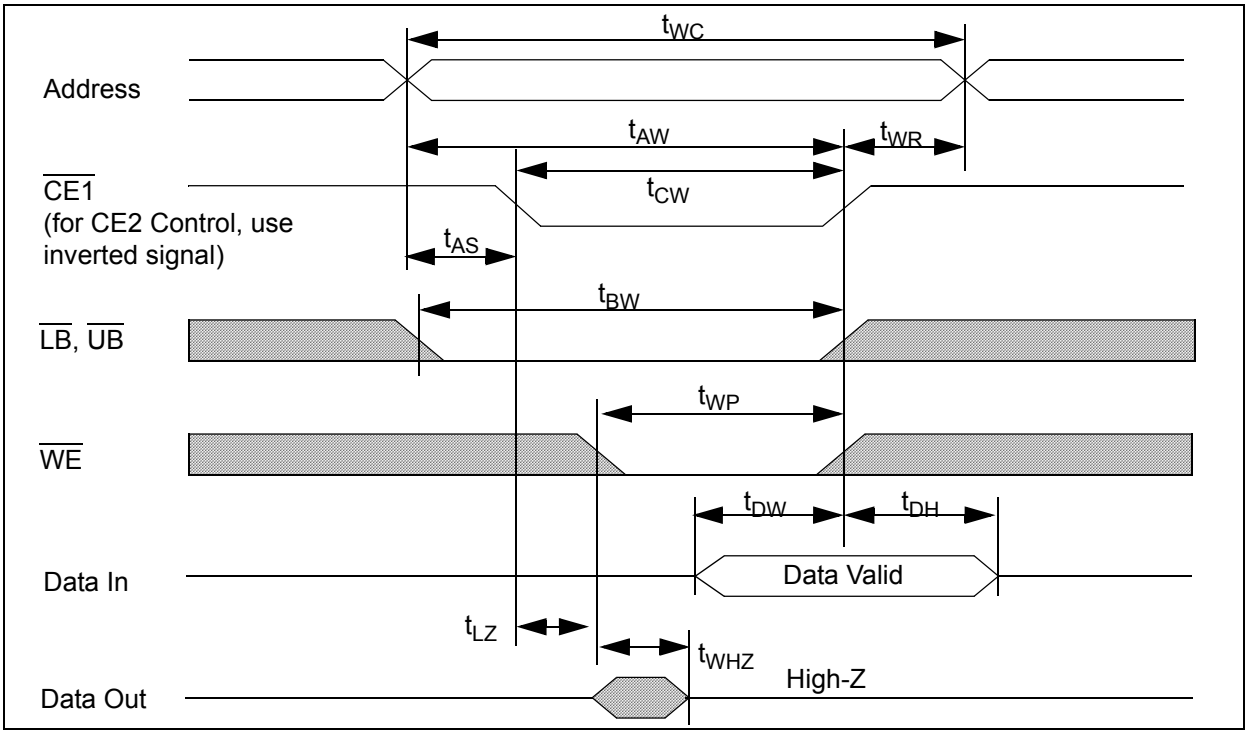
Timing Waveform of Read Cycle ($\overline{WE}$=V_{IH})



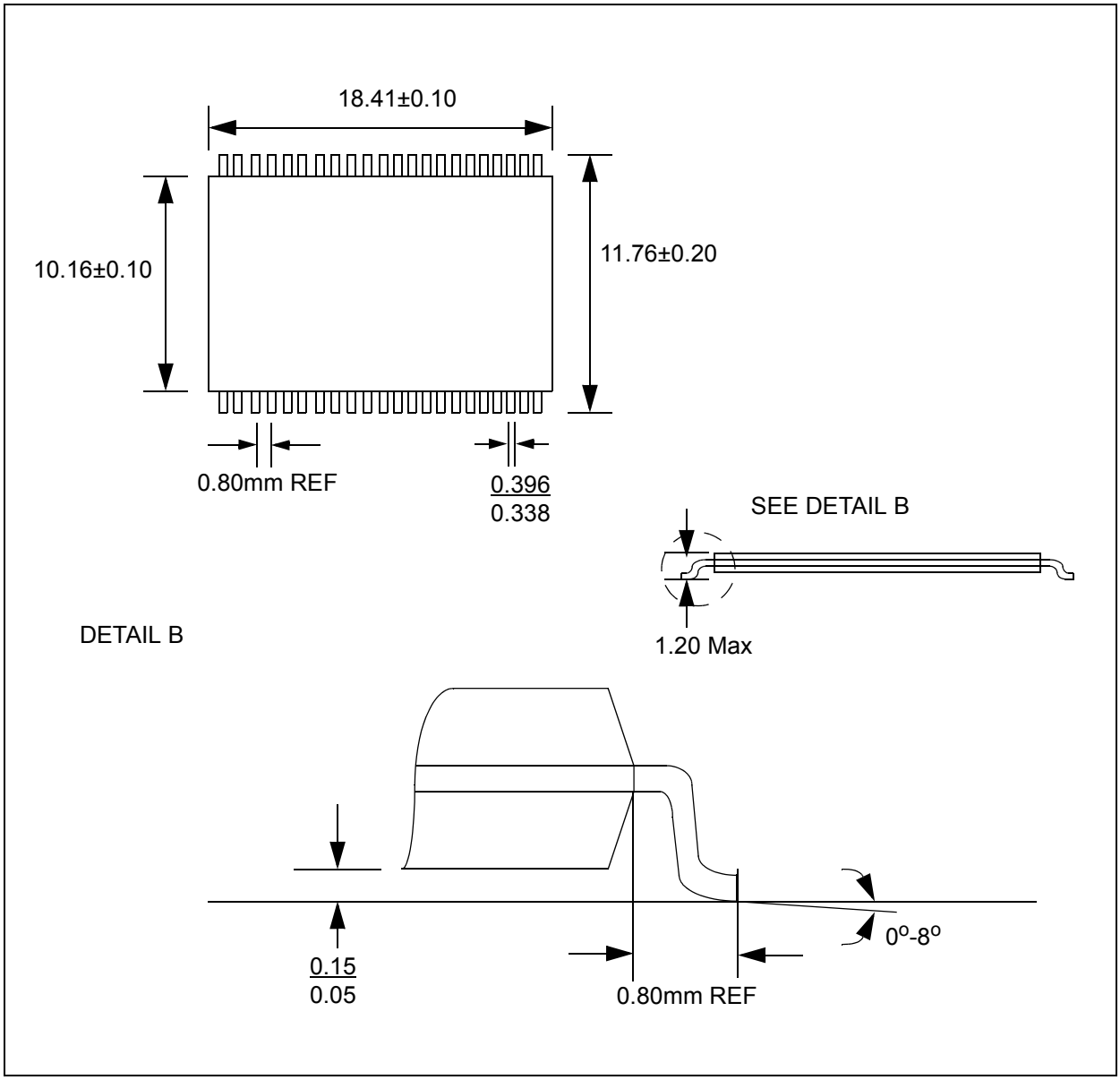
Timing Waveform of Write Cycle ($\overline{WE}$ control)



Timing Waveform of Write Cycle ($\overline{CE1}$ Control)

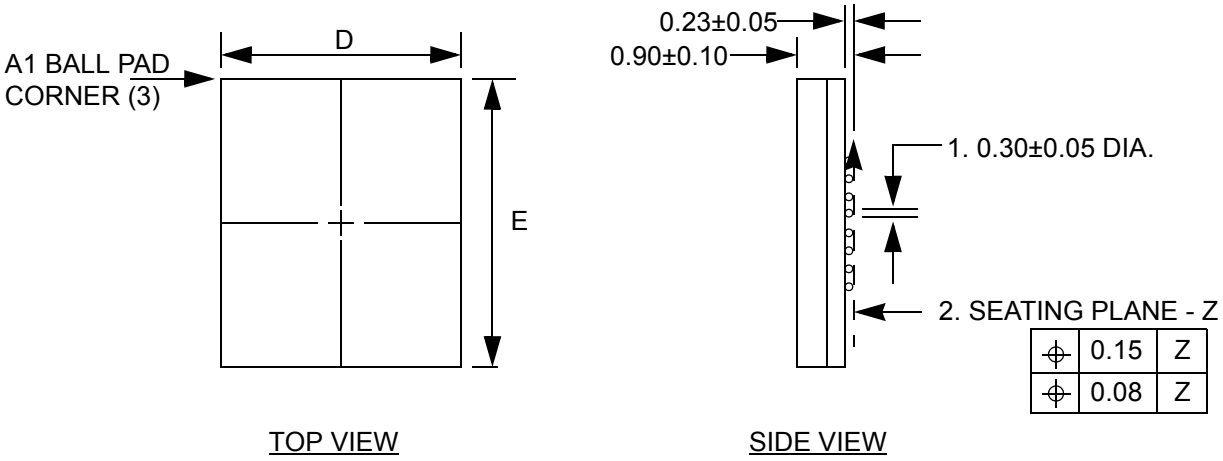


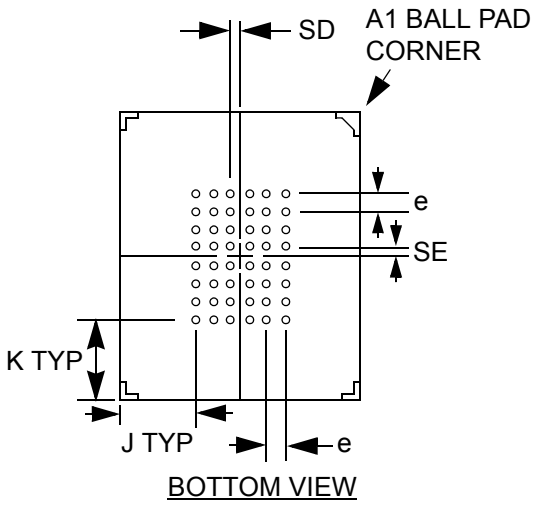
44-Lead TSOP II Package (T44)



Note:
1. All dimensions in inches (Millimeters)
2. Package dimensions exclude molding flash

Ball Grid Array Package





1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

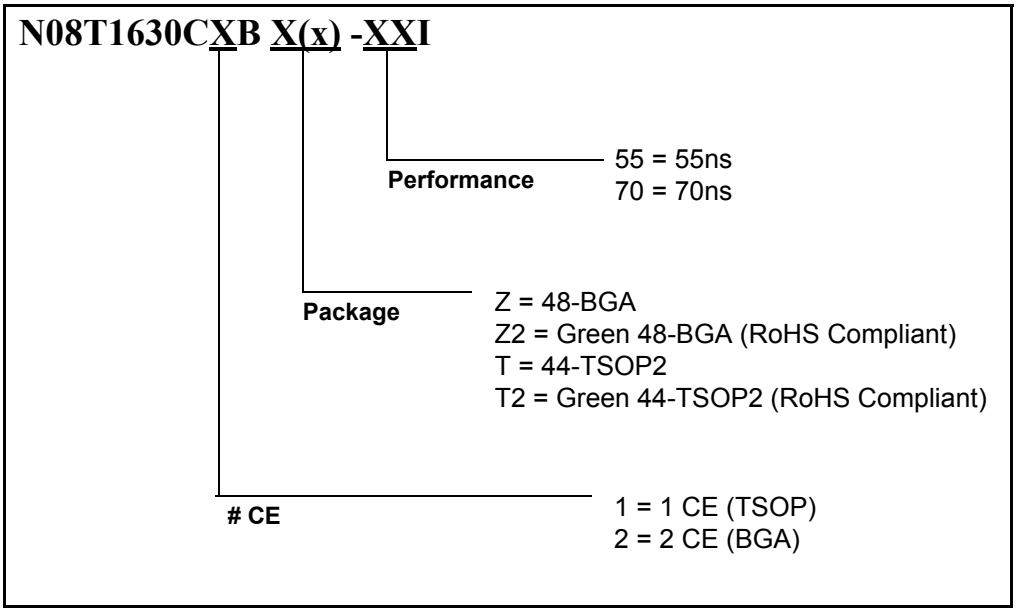
2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

Ordering Information



Revision History

Revision	Date	Change Description
A	August 2002	Initial Preliminary Release
B	Sept 2002	Added TSOP option to ordering information
C	November 2002	Added 55ns sort
D	February 2003	Updated BGA package thickness from 1.2mm to 1.0mm
E	April 2003	Updated for dual CE in BGA only
F	September 2003	Change I_{SB} @ 3.0v to 60 uA Change t_{HZ} to 20ns for 55ns part Change t_{DW} to 40ns for both 55ns and 70ns part
G	November 2003	Change I_{SB} @ 3.0v to 70 uA
H	January 2005	Added Green package offering