

# 8-input multiplexer (3-State)

# 74F251A

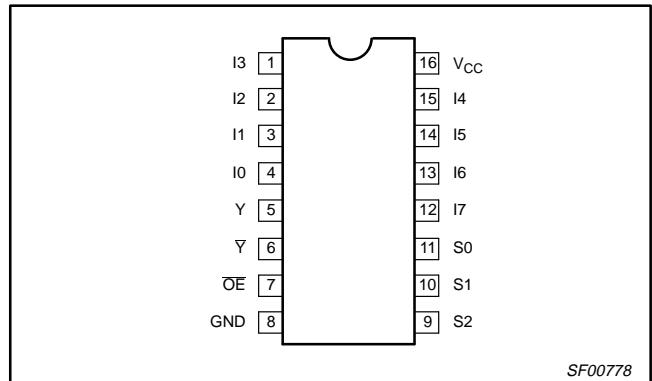
## FEATURES

- High speed 8-to-1 multiplexing
- On chip decoding
- Multifunction capability
- Inverting and Non-Inverting outputs
- Both outputs are 3-State for further multiplexer expansion

## DESCRIPTION

The 74F251A is a logic implementation of a single 8-position switch with the switch position controlled by the state of three Select (S0, S1, S2) inputs. True (Y) and complementary ( $\bar{Y}$ ) outputs are both provided. The output enable ( $\bar{OE}$ ) is active Low. When  $\bar{OE}$  is High, both outputs are in High impedance state, allowing multiple output connections to a common bus without driving nor loading the bus significantly. All but one device must be in High impedance state to avoid high currents that would exceed the maximum ratings when the outputs of the 3-State devices are tied together. When the output of more than one device is tied together the user must ensure that there is no overlap in the active Low portion of the output enable voltages.

## PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F251A	4.5ns	19mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
16-pin plastic DIP	N74F251AN	SOT38-4
16-pin plastic SO	N74F251AD	SOT162-1

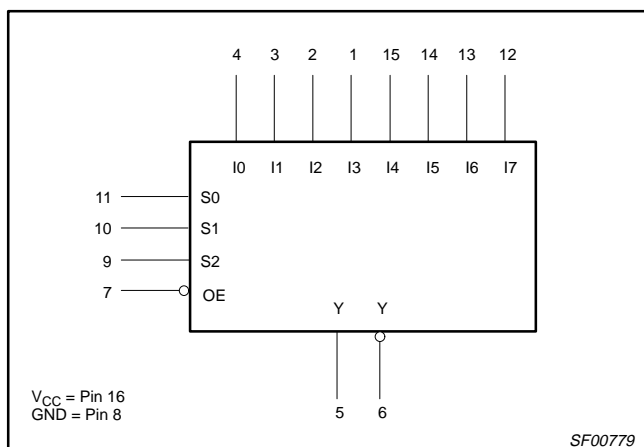
## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
I0–I7	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
S0–S2	Select inputs	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{OE}$	Output Enable input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
Y, $\bar{Y}$	Data outputs	150/40	3mA/24mA

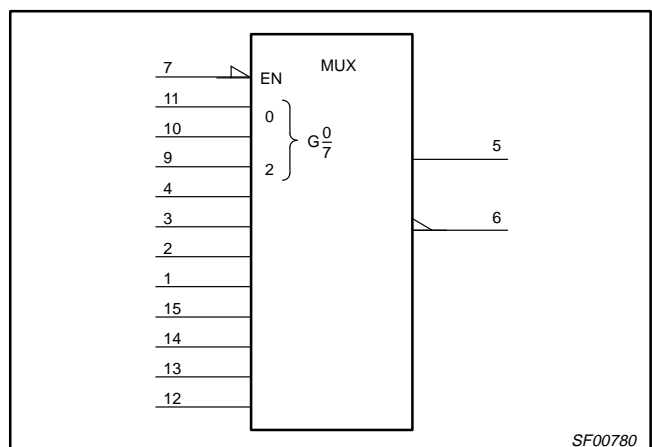
### NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



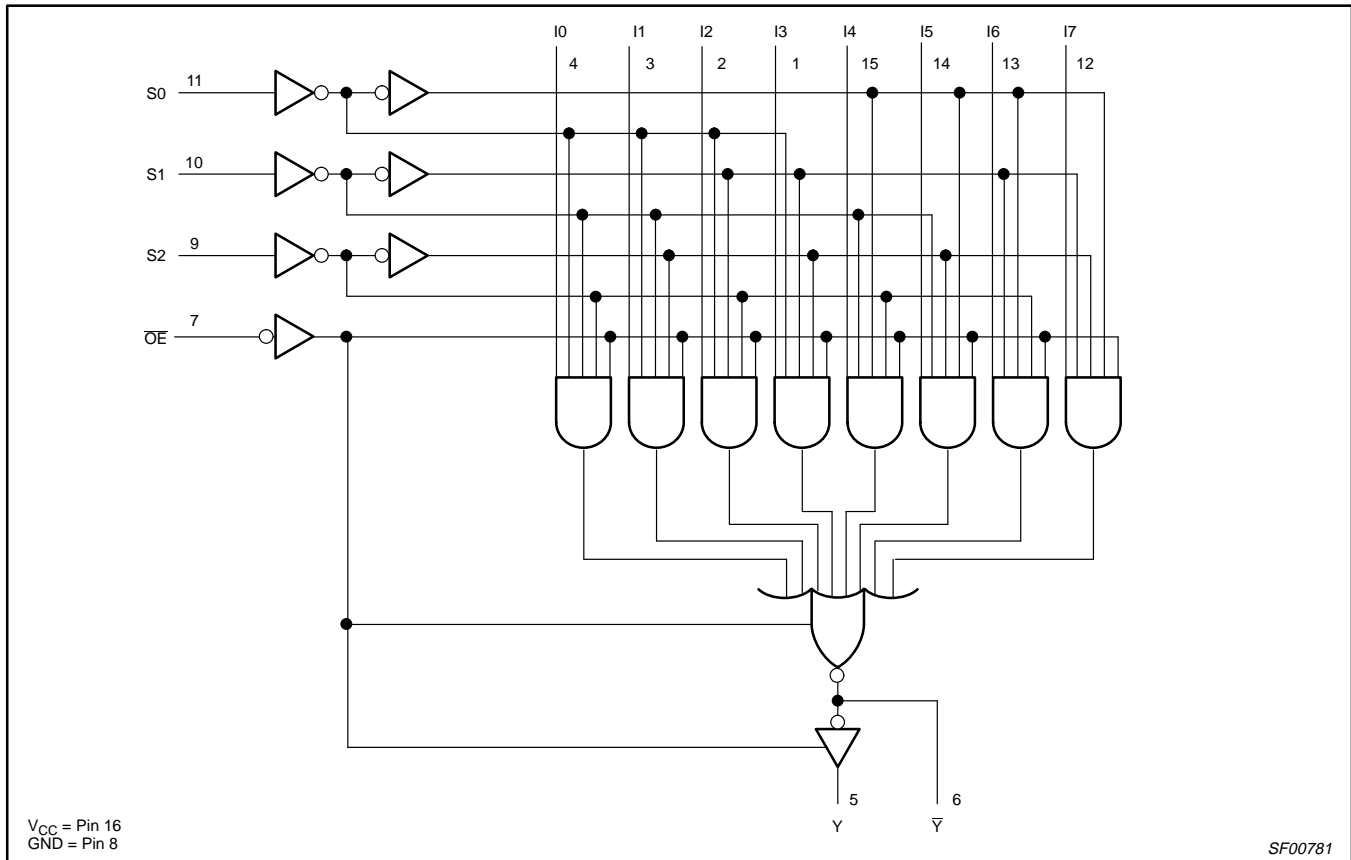
## IEC/IEEE SYMBOL



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### LOGIC DIAGRAM



### FUNCTION TABLE

INPUTS				OUTPUTS	
S2	S1	S0	OE	Y	Ȳ
X	X	X	H	Z	Z
L	L	L	L	I0	Ī0
L	L	H	L	I1	Ī1
L	H	L	L	I2	Ī2
L	H	H	L	I3	Ī3
H	L	L	L	I4	Ī4
H	L	H	L	I5	Ī5
H	H	L	L	I6	Ī6
H	H	H	L	I7	Ī7

#### NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care
- Z = High impedance "off" state

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limit set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	48	mA
$T_{amb}$	Operating free-air temperature range	0 to +70	°C
$T_{stg}$	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-3	mA
$I_{OL}$	Low-level output current			24	mA
$T_{amb}$	Operating free-air temperature range	0		70	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\%V_{CC}$	2.4		V	
			$\pm 5\%V_{CC}$	2.7	3.3	V	
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\%V_{CC}$		0.35	0.50	V
			$\pm 5\%V_{CC}$		0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
$I_I$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0V$			100	$\mu A$	
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7V$			20	$\mu A$	
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5V$			-0.6	mA	
$I_{OZH}$	Off-state output current High-level voltage applied	$V_{CC} = \text{MAX}, V_I = 2.7V$			50	$\mu A$	
$I_{OZL}$	Off-state output current Low-level voltage applied	$V_{CC} = \text{MAX}, V_I = 0.5V$			-50	mA	
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$	-60		-150	mA	
$I_{CC}$	Supply current (total)	$I_{CCH}$		20	27	mA	
		$I_{CCL}$		17	24	mA	
		$I_{CCZ}$		21	29	mA	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at  $V_{CC} = 5V, T_{amb} = 25^\circ C$ .
- Not more than one output should be shorted at a time. For testing  $I_{OS}$ , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

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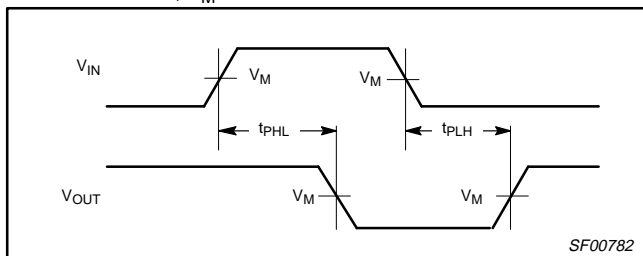
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## AC ELECTRICAL CHARACTERISTICS

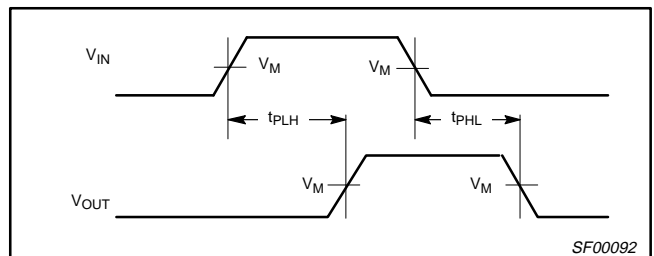
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to Y	Waveform 2	3.0 3.0	5.0 5.0	7.0 7.0	2.5 3.0	8.0 8.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay In to $\bar{Y}$	Waveform 1	2.5 1.0	4.5 2.5	7.0 5.0	2.0 1.0	7.5 5.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> to Y	Waveform 1 Waveform 2	4.5 4.0	6.5 5.5	10.0 9.0	4.0 3.5	11.5 9.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay S <sub>n</sub> to $\bar{Y}$	Waveform 1 Waveform 2	3.5 2.5	6.0 4.5	9.0 7.0	3.5 2.5	9.5 7.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time $\bar{OE}$ to Y	Waveform 3 Waveform 4	3.5 3.5	5.5 5.0	7.5 7.5	3.0 3.0	8.5 8.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time $\bar{OE}$ to Y	Waveform 3 Waveform 4	2.5 1.0	4.0 4.0	6.5 6.0	2.0 1.0	7.0 6.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time $\bar{OE}$ to $\bar{Y}$	Waveform 3 Waveform 4	2.5 2.5	4.0 4.0	6.5 6.5	2.0 2.5	7.0 7.0	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time $\bar{OE}$ to $\bar{Y}$	Waveform 3 Waveform 4	3.5 1.0	5.0 2.0	7.5 4.5	3.0 1.0	8.0 4.5	ns

## AC WAVEFORMS

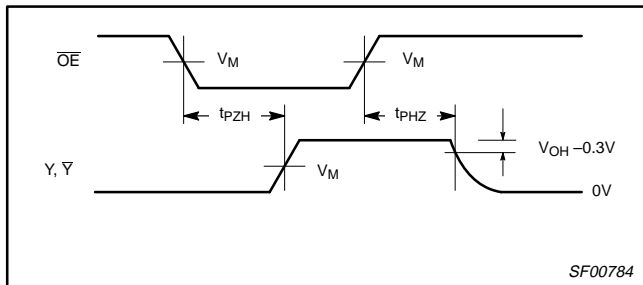
For all waveforms, V<sub>M</sub> = 1.5V



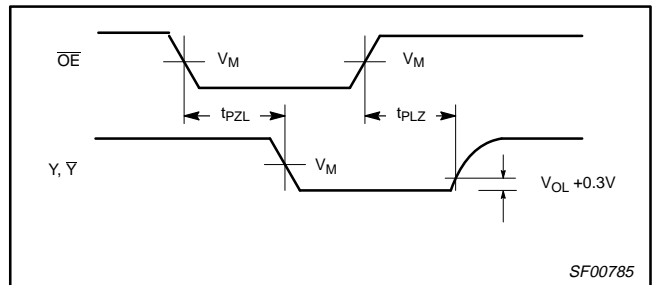
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

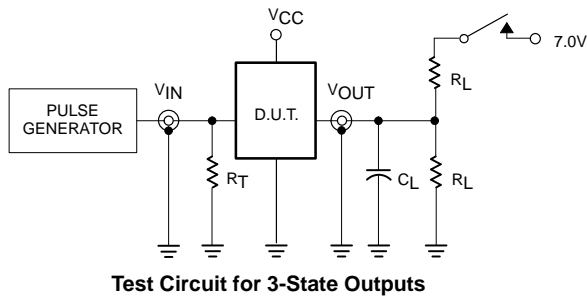


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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## TEST CIRCUIT AND WAVEFORMS



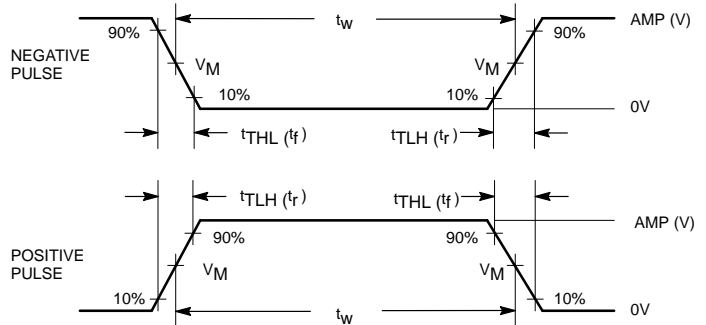
Test Circuit for 3-State Outputs

### SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

### DEFINITIONS:

$R_L$  = Load resistor; see AC electrical characteristics for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777