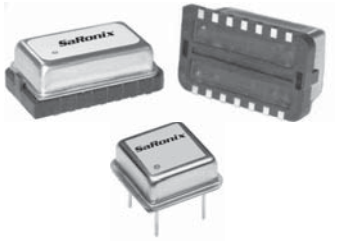
SaRonix

Crystal Clock Oscillator 3.3V, LVCMOS / HCMOS, Tri-State

Technical Data

NTH / NCH Series



ACTUAL SIZE

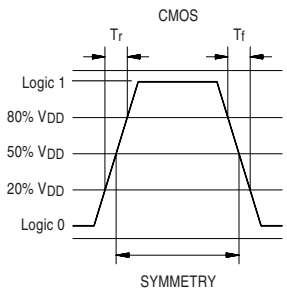
Description

A crystal controlled, low current, low jitter and high frequency oscillator with precise rise and fall times demanded in networking applications. The tri-state function on the NTH enables the output to go high impedance. Device is packaged in a 14 or an 8-pin DIP compatible resistance welded, all metal grounded case to reduce EMI. True SMD DIL14 versions for IR reflow are available, select option "S" in part number builder. See separate data sheet for SMD package dimensions.

Applications & Features

- ADSL, DSL
- DS3, ES3, E1, STS-1, T1
- Ethernet Switch, Gigabit Ethernet
- Fibre Channel Controller
- MPEG
- Network Processors
- Voice Over Packet
- 32 Bit Microprocessors
- Tri-State output on NTH
- LVCMOS / HCMOS compatible
- Available up to 106.25 MHz

Output Waveform



Frequency Range:		0.5 MHz to 106.25 MHz
Frequency Stability:		±20, ±25, ±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, 30 day aging, shock and vibration.
Temperature Range:		
	Operating:	0 to +70°C or -40 to +85°C, See Part Numbering Guide
	Storage:	-55 to +125°C
Supply Voltage:		
	Recommended Operating:	3.3V ±10%
Supply Current:		20mA max, 0.5 to 30 MHz 25mA max, 30+ to 50 MHz 30mA max, 50+ to 80 MHz 35mA max, 80+ to 106.25 MHz
Output Drive:		
HCMOS	Symmetry:	45/55% max 0.5 to 70 MHz max 40/60% max @ 50% V_{DD}
	Rise and Fall Times:	4ns max 0.5 to 50 MHz, 20% to 80% V_{DD} 3ns max 50+ to 80 MHz 1.5ns max 80+ to 106.25 MHz
	Logic 0:	10% V_{DD} max
	Logic 1:	90% V_{DD} min
	Load:	50 pF, 0.5 to 50 MHz 30pF, 50+ to 70 MHz 15pF, 70+ to 106.25 MHz
	Period Jitter RMS:	8ps max
Mechanical:		
	Shock:	MIL-STD-883, Method 2002, Condition B
	Solderability:	MIL-STD-883, Method 2003
	Terminal Strength:	MIL-STD-883, Method 2004, Conditions A & C
	Vibration:	MIL-STD-883, Method 2007, Condition A
	Solvent Resistance:	MIL-STD-202, Method 215
	Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C
Environmental:		
	Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
	Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2
	Thermal Shock:	MIL-STD-883, Method 1011, Condition A
	Moisture Resistance:	MIL-STD-883, Method 1004

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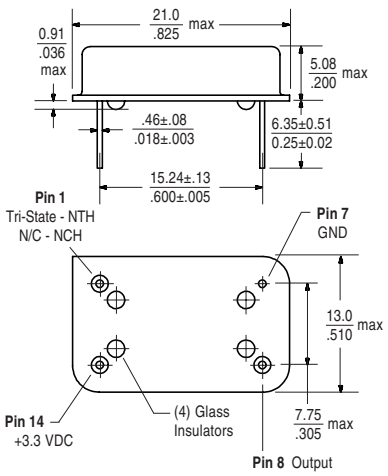
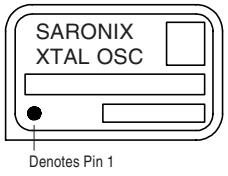
Package Details

FULL SIZE PACKAGE

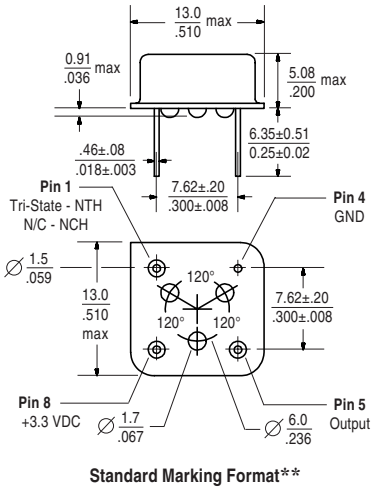


Standard Marking Format**

Includes Date Code, Frequency & Part Number



HALF SIZE PACKAGE



Standard Marking Format**

Includes Date Code, Frequency & Part Number

****Exact location of items may vary**

Part Numbering Guide

NTH 0 8 0 C 3 - 40.0000 (T)

NTH = Pin 1: Tri state, LVCMOS
NCH = Pin 1: N/C, LVCMOS

Symmetry
0 = 40/60% max, 0 to 70°C
2 = 40/60% max, -40 to 85°C
A = 45/55% max, 0 to 70°C, 70 MHz max
C = 45/55% max, -40 to 85°C, 70 MHz max

Frequency Range
3 = 0.5 to 6 MHz
6 = 6+ to 24 MHz
8 = 24+ to 106.25 MHz

Package
0 = Full Size, Thru-Hole
9 = Half Size, Thru-Hole
K = Full Size, Gull Wing
J = Half Size, Gull Wing
N = Half Size, Gull Wing, Spanked Leads
S = Full Size, True SMD Adaptor (see separate data sheet for dimensions)

Stability Tolerance
C = ±100ppm
B = ±50ppm
A = ±25ppm, 0 to +70°C only
AA = ±20ppm, 0 to +70°C only

3.3V Supply

Frequency (MHz)

Packing Method
(T) = Tape & Reel for SMD versions, full reel increments only, 200pcs (full size) or 250pcs (half size)
Blank = Bulk

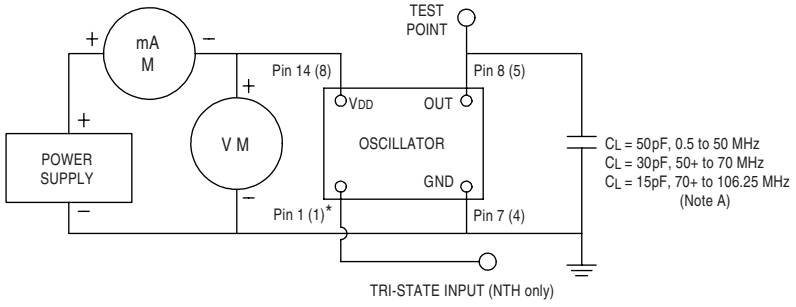
Tri-State Logic Table (NTH only)

Pin 1 Input	Pin 8 (5) Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:
Logic 1 = 2.2V min
Logic 0 = 0.8V max

Output:	Oscillation @ V_{IN}, 2.2V min
Output:	High Impedance @ V_{IN}, 0.8V max
Internal Pullup Resistance	50KΩ min
Control Input:	Disable Output Delay: 100ns max

Test Circuit



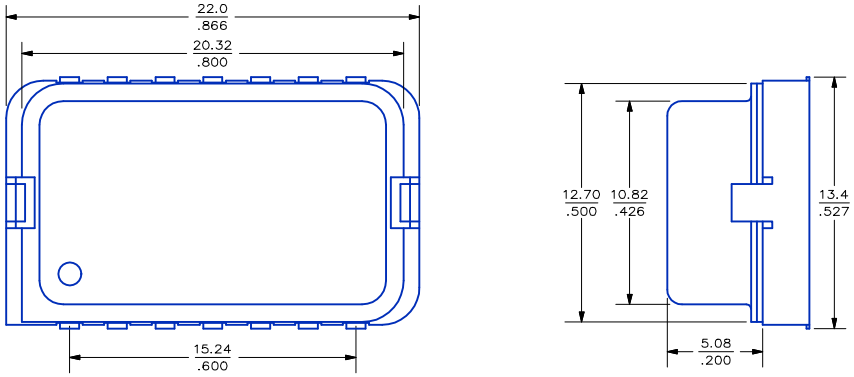
NOTE A: C_L includes probe and fixture capacitance
*( ) Indicates pin numbers for half-size package

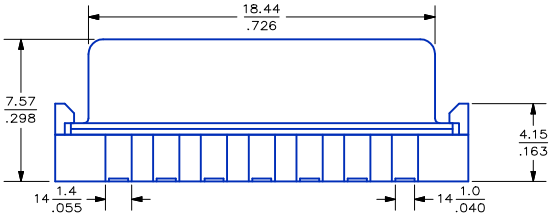
All specifications are subject to change without notice.

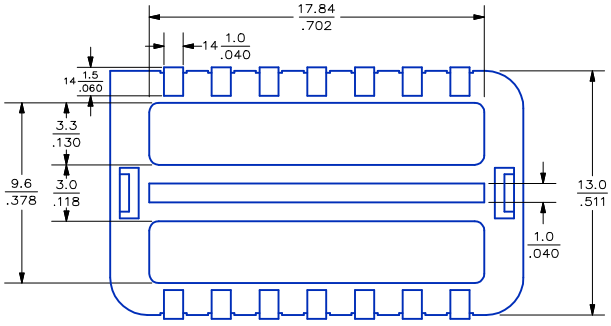
DS-159 REV D

True SMD Adaptor - 7.57mm High

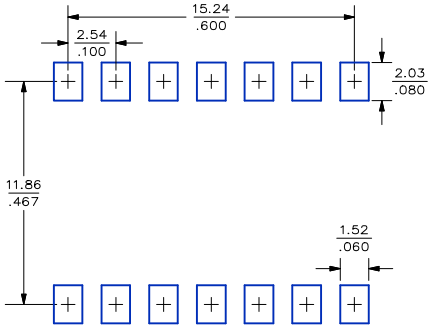
Technical Data







RECOMMENDED LAND PATTERN



REV A