NCV8506 Series

Micropower 400 mA LDO Linear Regulators with DELAY and $\overline{\text{RESET}}$

The NCV8506 is a family of precision micropower voltage regulators. Their output current capability is 400 mA. The family has output voltage options for Adjustable, 2.5 V, 3.3 V and 5.0 V.

The output voltage is accurate within ± 2.0% with a maximum dropout voltage of 0.6 V at 400 mA. Low quiescent current is a feature drawing only 100 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text{RESET}}$ (with DELAY).

The active $\overline{\text{RESET}}$ circuit operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops below the regulation limits.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

Features

- Output Voltage Options: Adjustable, 2.5 V, 3.3 V, 5.0 V
- ± 2.0% Output
- Low 100 μA Quiescent Current
- Fixed or Adjustable Output Voltage
- Active $\overline{\text{RESET}}$
- 400 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - −15 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control

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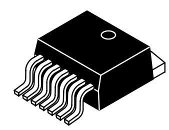
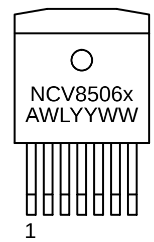
MARKING DIAGRAM



D²PAK−7
DPS SUFFIX
CASE 936AB



x = Voltage Ratings as Indicated Below:
A = Adjustable
2 = 2.5 V
3 = 3.3 V
5 = 5.0 V
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

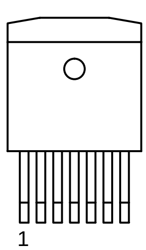
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

PIN CONNECTIONS

ADJUSTABLE OUTPUT

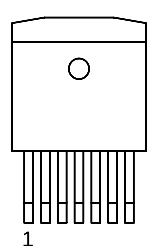
D²PAK−7



Tab = GND
Lead 1. DELAY
2. NC
3. $\overline{\text{RESET}}$
4. GND
5. V_{ADJ}
6. V_{OUT}
7. V_{IN}

FIXED OUTPUT

D²PAK−7



Tab = GND
Lead 1. DELAY
2. NC
3. $\overline{\text{RESET}}$
4. GND
5. SENSE
6. V_{OUT}
7. V_{IN}

January, 2004 − Rev. 3
Publication Order Number:
NCV8506/D

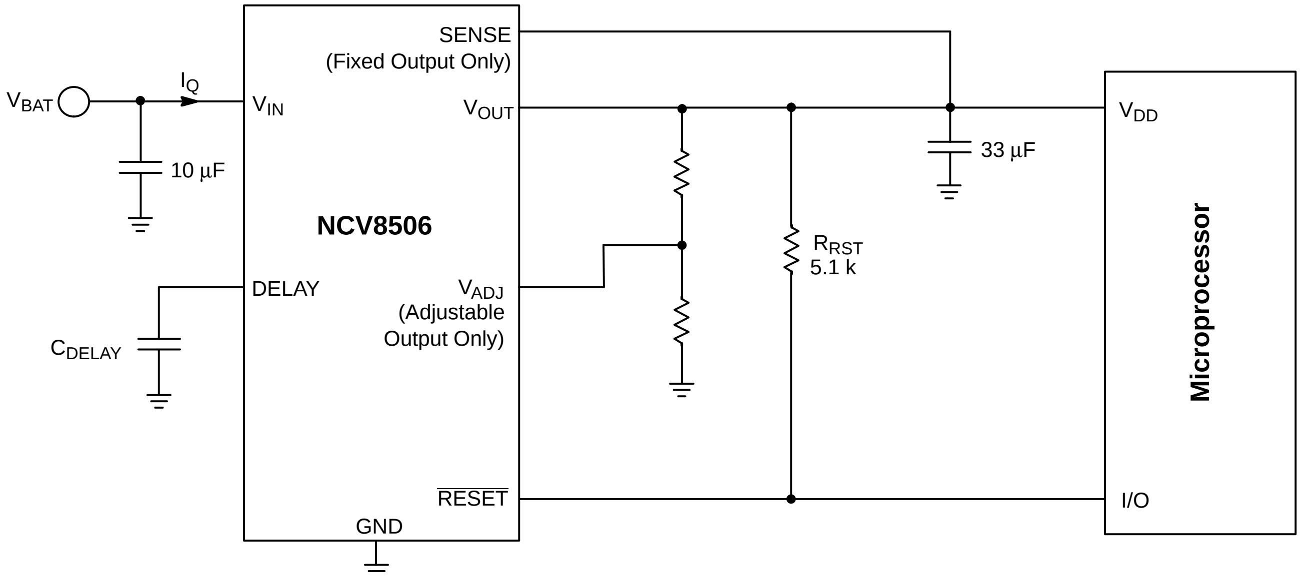


Figure 1. Application Diagram

MAXIMUM RATINGS*†

Rating		Value	Unit
V_{IN} (DC)		−15 to 45	V
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)		60	V
Operating Voltage		45	V
V_{OUT} (DC)		16	V
Voltage Range ($\overline{RESET}$, DELAY)		−0.3 to 10	V
Input Voltage Range V_{ADJ}		−0.3 to 16	V
ESD Susceptibility	(Human Body Model) (Machine Model)	4.0 200	kV V
Junction Temperature, T_J		−40 to +150	°C
Storage Temperature, T_S		−55 to 150	°C
Package Thermal Resistance, 7 Lead D^2PAK Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$		 2.0 10−50**	 °C/W °C/W
Lead Temperature Soldering:	Reflow: (SMD styles only) (Note 1)	240 peak (Note 2)	°C

1. 60 second maximum above 183°C.
2. −5°C/+0°C allowable conditions.

*The maximum package power dissipation must be observed.
**Depending on thermal properties of substrate, $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.
†During the voltage range which exceeds the maximum tested voltage of V_{IN}, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

ELECTRICAL CHARACTERISTICS (I_{OUT} = 1.0 mA, −40°C ≤ T_J ≤ 150°C; V_{IN} = dependent on voltage option (Note 3); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage for 2.5 V Option (V_O)	6.5 V < V_{IN} < 16 V, 1.0 mA ≤ I_{OUT} ≤ 400 mA **4.5 V < V_{IN} < 26 V**, 1.0 mA ≤ I_{OUT} ≤ 400 mA	2.450 2.425	2.5 2.5	2.550 2.575	V V
Output Voltage for 3.3 V Option (V_O)	7.3 V < V_{IN} < 16 V, 1.0 mA ≤ I_{OUT} ≤ 400 mA **4.5 V < V_{IN} < 26 V**, 1.0 mA ≤ I_{OUT} ≤ 400 mA	3.234 3.201	3.3 3.3	3.366 3.399	V V
Output Voltage for 5.0 V Option (V_O)	9.0 V < V_{IN} < 16 V, 1.0 mA ≤ I_{OUT} ≤ 400 mA **6.0 V < V_{IN} < 26 V**, 1.0 mA ≤ I_{OUT} ≤ 400 mA	4.90 4.85	5.0 5.0	5.10 5.15	V V
Output Voltage for Adjustable Option (V_O)	$V_{OUT} = V_{ADJ}$ (Unity Gain) 6.5 V < V_{IN} < 16 V, 1.0 mA < I_{OUT} < 400 mA **4.5 V < V_{IN} < 26 V**, 1.0 mA < I_{OUT} < 400 mA	 1.274 1.261	 1.300 1.306	 1.326 1.339	 V V
Dropout Voltage ($V_{IN} − V_{OUT}$) (5.0 V and Adj. > 5.0 V Options Only)	I_{OUT} = 400 mA I_{OUT} = 1.0 mA	− −	400 30	600 150	mV mV
Load Regulation	V_{IN} = 14 V, 5.0 mA ≤ I_{OUT} ≤ 400 mA	−30	5.0	30	mV
Line Regulation (2.5 V, 3.3 V, and Adjustable Options)	4.5 V < V_{IN} < 26 V, I_{OUT} = 1.0 mA	−	5.0	25	mV
Line Regulation (5.0 V Option)	6.0 V < V_{IN} < 26 V, I_{OUT} = 1.0 mA	−	5.0	25	mV
Quiescent Current, (I_Q) Active Mode	I_{OUT} = 100 μA, V_{IN} = 12 V, Delay = 3.0 V I_{OUT} = 75 mA, V_{IN} = 14 V, Delay = 3.0 V I_{OUT} ≤ 400 mA, V_{IN} = 14 V, Delay = 3.0 V	− − −	100 2.5 25	150 5.0 45	μA mA mA
Current Limit	−	425	800	−	mA
Short Circuit Output Current	V_{OUT} = 0 V	100	500	−	mA
Thermal Shutdown	(Guaranteed by Design)	150	180	−	°C

3. Voltage range specified in the Output Stage of the Electrical Characteristics in boldface type.

ELECTRICAL CHARACTERISTICS (continued) (I_{OUT} = 1.0 mA, −40°C ≤ T_J ≤ 150°C; V_{IN} = dependent on voltage option (Note 4); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reset Function ($\overline{RESET}$)					
$\overline{RESET}$ Threshold for 2.5 V Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	V_{IN} = 4.5 V (Note 5) (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	 2.35 2.30 25	 − − −	 1.0 × V_O − −	 V V mV
$\overline{RESET}$ Threshold for 3.3 V Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	V_{IN} = 4.5 V (Note 5) (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	 3.10 3.00 35	 − − −	 1.0 × V_O − −	 V V mV
$\overline{RESET}$ Threshold for 5.0 V Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	V_{IN} = 6.0 V (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	 4.70 4.60 50	 − − −	 1.0 × V_O − −	 V V mV
$\overline{RESET}$ Threshold for Adjustable Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	V_{IN} = 4.5 V (Note 5) (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	 1.22 1.19 10	 − − −	 1.0 × V_O − −	 V V mV
Output Voltage Low (V_{RLO})	V_{IN} = Minimum (Note 6) (Note 7) 1.0 V ≤ V_{OUT} ≤ V_{RL}, $R_{\overline{RESET}}$ = 5.1 k	−	0.1	0.4	V
DELAY Switching Threshold (V_{DT}) (2.5 V, 3.3 V, and 5.0 V Options)	V_{IN} = Minimum (Note 6) (Note 7)	1.4	1.8	2.2	V
DELAY Switching Threshold (V_{DT}) (Adjustable Option)	V_{IN} = Minimum (Note 6) (Note 7)	1.0	1.3	1.6	V
DELAY Low Voltage	V_{IN} = Minimum (Note 6) (Note 7) V_{OUT} < $\overline{RESET}$ Threshold Low(min)	−	−	0.2	V
DELAY Charge Current	V_{IN} = Minimum (Note 6) (Note 7) DELAY = 1.0 V, V_{OUT} > V_{RH}	2.5	4.0	5.5	μA
DELAY Discharge Current	V_{IN} = Minimum (Note 6) (Note 7) DELAY = 1.0 V, V_{OUT} < V_{RL}	5.0	−	−	mA
Voltage Adjust (Adjustable Output only)					
Input Current	V_{ADJ} = 1.25 V	−0.5	−	0.5	μA

4. Voltage range specified in the Output Stage of the Electrical Characteristics in boldface type.
5. For V_{IN} ≤ 4.5 V, a $\overline{RESET}$ = Low may occur with the output in regulation.
6. Part is guaranteed by design to meet specification over the entire V_{IN} voltage range, but is production tested only at the specified V_{IN} voltage.
7. Minimum V_{IN} = 4.5 V for 2.5 V, 3.3 V, and Adjustable options. Minimum V_{IN} = 6.0 V for 5.0 V option.

PACKAGE PIN DESCRIPTION, ADJUSTABLE OUTPUT

Pin Number	Pin Symbol	Function
1	DELAY	Timing capacitor for $\overline{RESET}$ function.
2	NC	No connection.
3	$\overline{RESET}$	Active reset (accurate to $V_{OUT} \geq 1.0$ V)
4	GND	Ground. All GND leads must be connected to Ground.
5	V_{ADJ}	Voltage Adjust. A resistor divider from V_{OUT} to this lead sets the output voltage.
6	V_{OUT}	±2.0%, 400 mA output.
7	V_{IN}	Input Voltage.

PACKAGE PIN DESCRIPTION, FIXED OUTPUT

Pin Number	Pin Symbol	Function
1	DELAY	Timing capacitor for $\overline{RESET}$ function.
2	NC	No connection.
3	$\overline{RESET}$	Active reset (accurate to $V_{OUT} \geq 1.0$ V)
4	GND	Ground. All GND leads must be connected to Ground.
5	SENSE	Kelvin connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not desired, connect to V_{OUT}.
6	V_{OUT}	±2.0%, 400 mA output.
7	V_{IN}	Input Voltage.

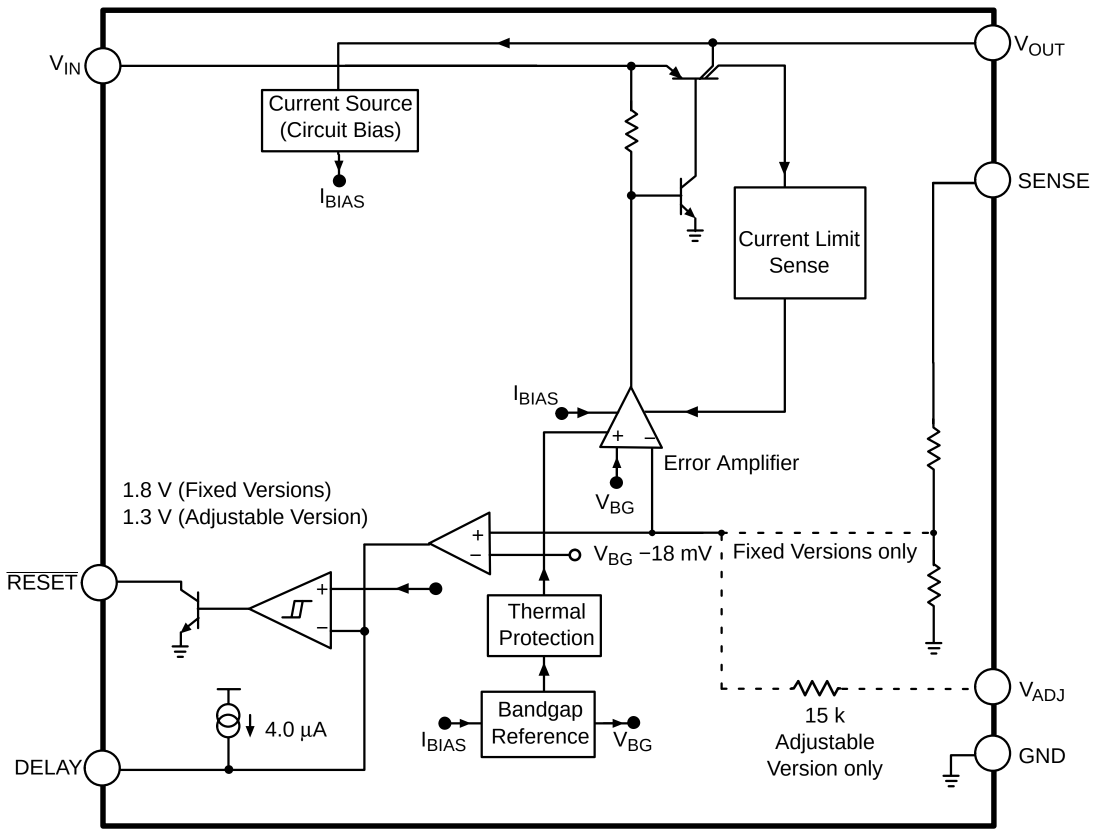


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

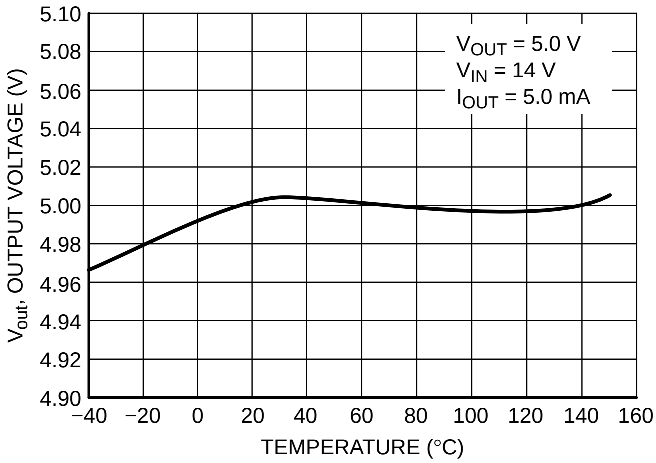


Figure 3. 5 V Output Voltage vs Temperature

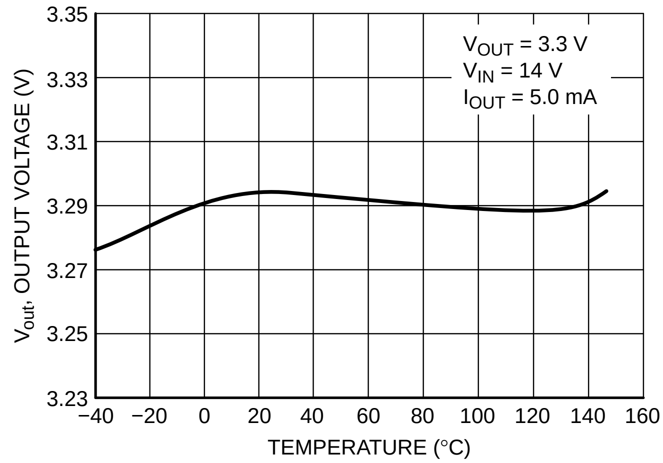


Figure 4. 3.3 V Output Voltage vs Temperature

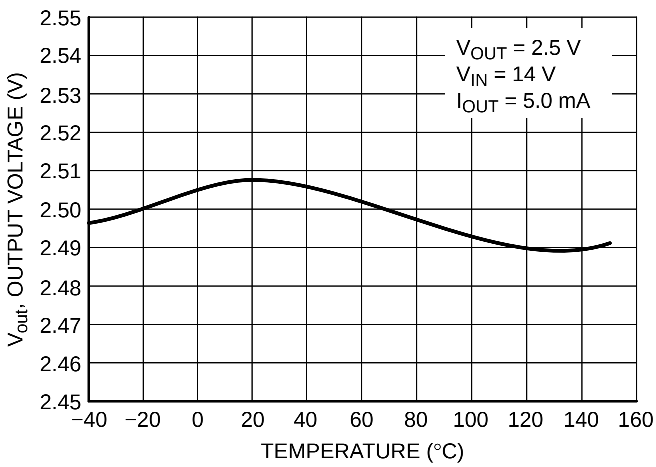


Figure 5. 2.5 V Output Voltage vs Temperature

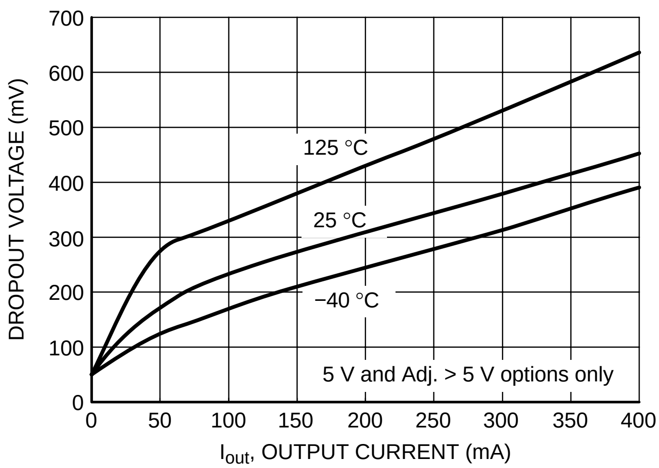


Figure 6. Dropout Voltage vs Output Current

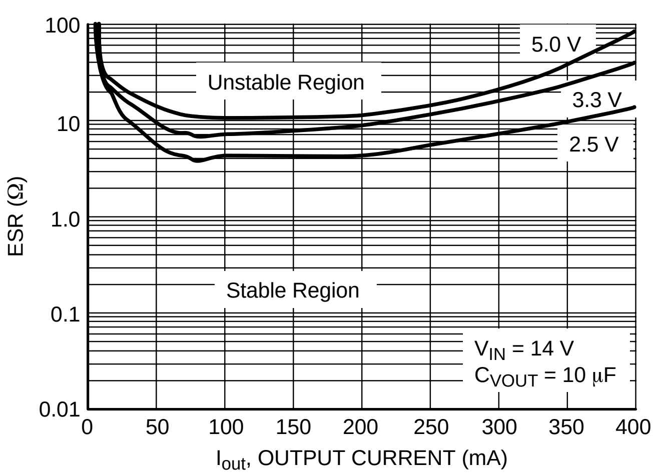


Figure 7. Output Stability with Output Voltage Change

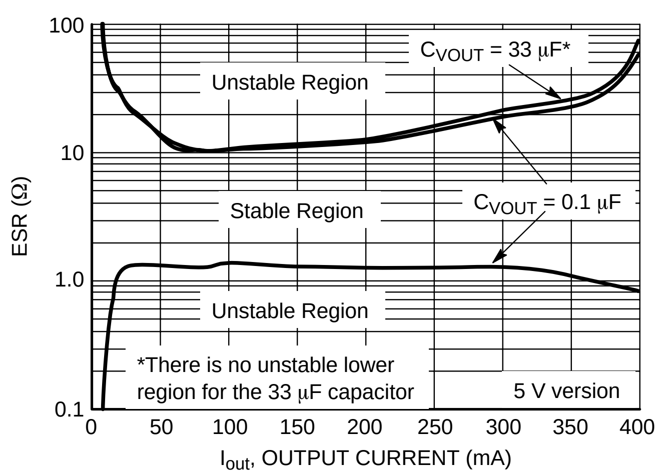


Figure 8. Output Stability with Output Capacitor Change

TYPICAL PERFORMANCE CHARACTERISTICS

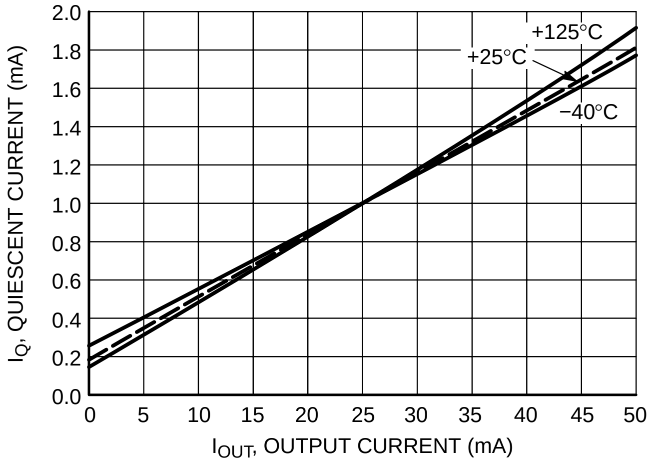


Figure 9. Quiescent Current vs Output Current

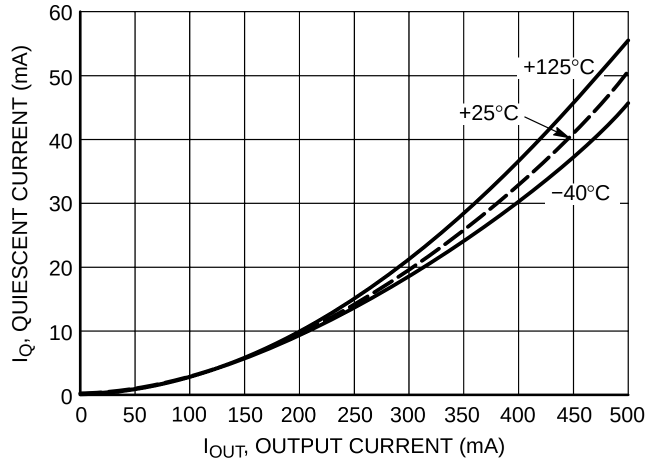


Figure 10. Quiescent Current vs Output Current

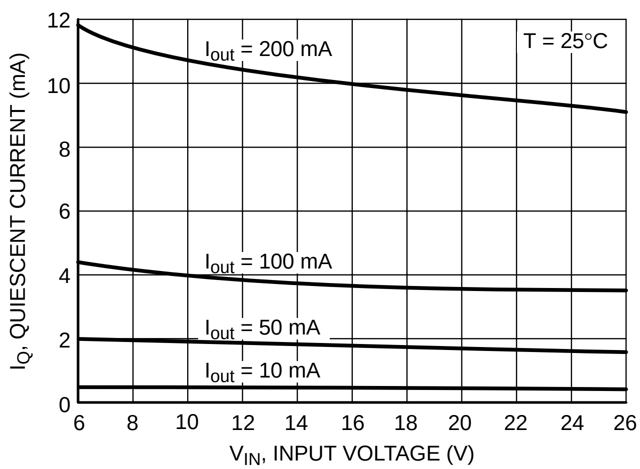


Figure 11. Quiescent Current vs Input Voltage

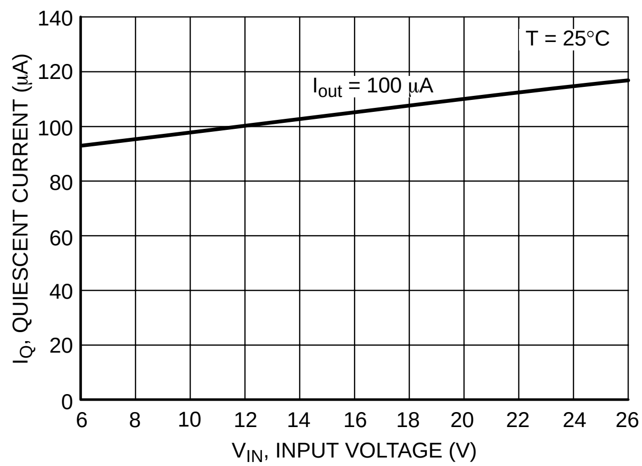


Figure 12. Quiescent Current vs Input Voltage

CIRCUIT DESCRIPTION

REGULATOR CONTROL FUNCTIONS

The NCV8506 contains the microprocessor compatible control function $\overline{\text{RESET}}$ (Figure 13).

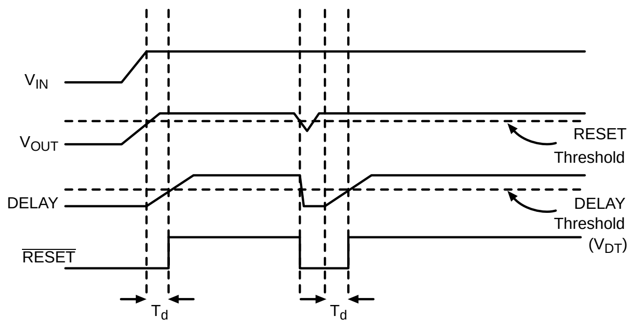


Figure 13. Reset and Delay Circuit Wave Forms

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up until V_{OUT} is within 1.5% of the regulated output voltage, or when V_{OUT} drops out of regulation,and is lower than 4.0% below the regulated output voltage. Hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

DELAY Function

The reset delay circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead.

The DELAY lead provides source current (typically 4.0 μA) to the external DELAY capacitor during the following proceedings:

1. During Power Up (once the regulation threshold has been verified).
2. After a reset event has occurred and the device is back in regulation. The DELAY capacitor is discharged when the regulation ($\overline{\text{RESET}}$ threshold) has been violated. This is a latched incident. The capacitor will fully discharge and wait for the device to regulate before going through the delay time event again.

Voltage Adjust

Figure 14 shows the device setup for a user configurable output voltage. The feedback to the V_{ADJ} pin is taken from a voltage divider referenced to the output voltage. The loop is balanced around the Unity Gain threshold (1.30 V typical).

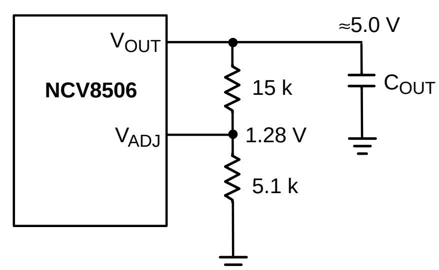


Figure 14. Adjustable Output Voltage

APPLICATION NOTES

SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$t_{DELAY} = \frac{[C_{DELAY}(V_{dt} - \text{Reset Delay Low Voltage})]}{\text{Delay Charge Current}}$$

Example:

Using C_{DELAY} = 33 nF.

Assume reset Delay Low Voltage = 0.

Use the typical value for V_{dt} = 1.8 V (2.5 V, 3.3 V, and 5.0 V options).

Use the typical value for Delay Charge Current = 4.2 μA.

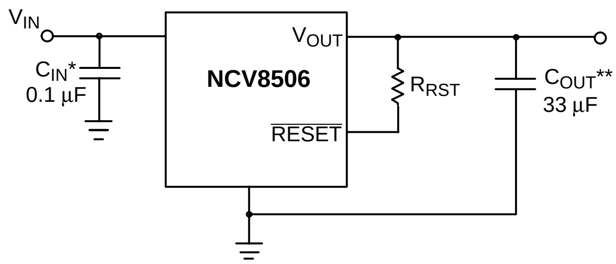
$$t_{DELAY} = \frac{[33\ \text{nF}(1.8 - 0)]}{4.2\ \mu\text{A}} = 14\ \text{ms}$$

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 15 should work for most applications, however it is not necessarily the optimized solution.



*C_{IN} required if regulator is located far from the power supply filter.
**C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

Figure 15. Test and Application Circuit Showing Output Compensation

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 16) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}] I_{OUT(max)} + V_{IN(max)} I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

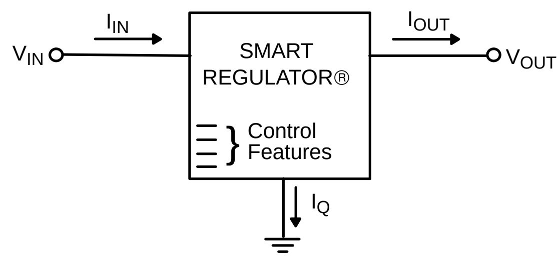


Figure 16. Single Output Regulator with Key Performance Parameters Labeled

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION

Device	Output Voltage	Package	Shipping†
NCV8506D2TADJ	Adjustable	D^2PAK−7	50 Units/Rail
NCV8506D2TADJR4			750 Tape & Reel
NCV8506D2T25	2.5 V		50 Units/Rail
NCV8506D2T25R4			750 Tape & Reel
NCV8506D2T33	3.3 V		50 Units/Rail
NCV8506D2T33R4			750 Tape & Reel
NCV8506D2T50	5.0 V		50 Units/Rail
NCV8506D2T50R4			750 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

D^{2}PAK−7
DPS SUFFIX
CASE 936AB−01
ISSUE O

For D^{2}PAK Outline and Dimensions − Contact Factory

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PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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ON Semiconductor Website: http://onsemi.com

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