

DOT MATRIX LCD 80-OUT SEGMENT DRIVER

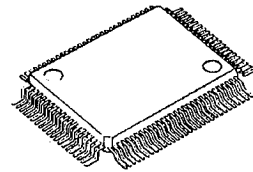
■ GENERAL DESCRIPTION

The NJU6446 is a serial input, 80-out segment driver for dot matrix LCDs, especially useful as extension driver for LCD controller drivers. It consists of bidirectional shift register, 80-bit latch, and 80-out high voltage LCD drivers.

The bidirectional shift register performs the efficient extension driver allocation according to the number of characters and easy wiring with the LCD panel.

As the 80-driver has 4 level voltage input to drive the LCD, adjustable driving voltage according to the LCD panel can be supplied from the external power source.

■ PACKAGE OUTLINE

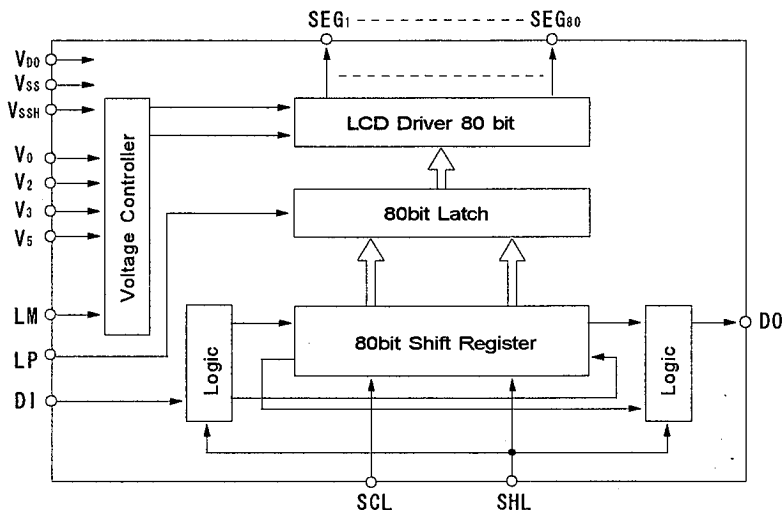


NJU6446F

■ FEATURES

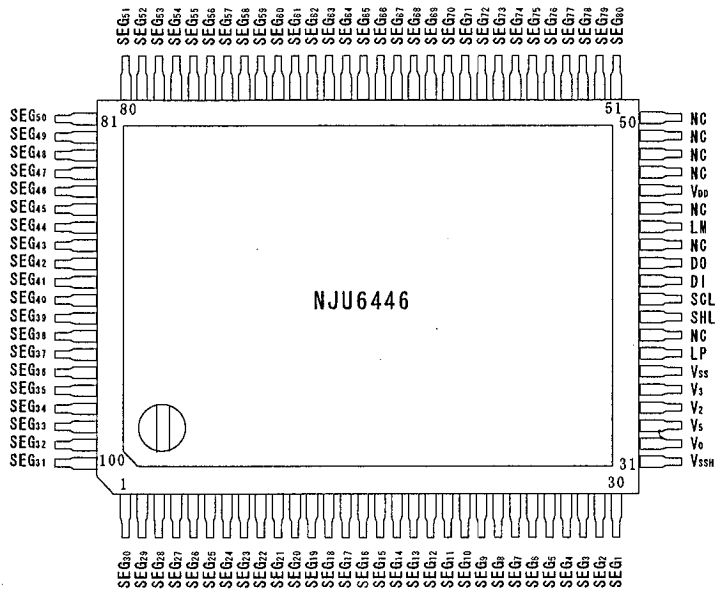
- 80 Segment Drivers
- 80-bit Shift Register (Bidirectional Shift Register)
- Two of Shift Direction Select Terminal
- Fast Data Transmission (Shift Clock 3.3 MHz min.)
- External Power Supply for LCD Driving Voltage
- LCD Driving Voltage --- $V_{DD} - 3.0V \sim V_{DD} - 10.0V$
- Operating Voltage --- $5.0V \pm 10\%$
- Package Outline --- QFP100/Chip
- C-MOS Technology

■ BLOCK DIAGRAM

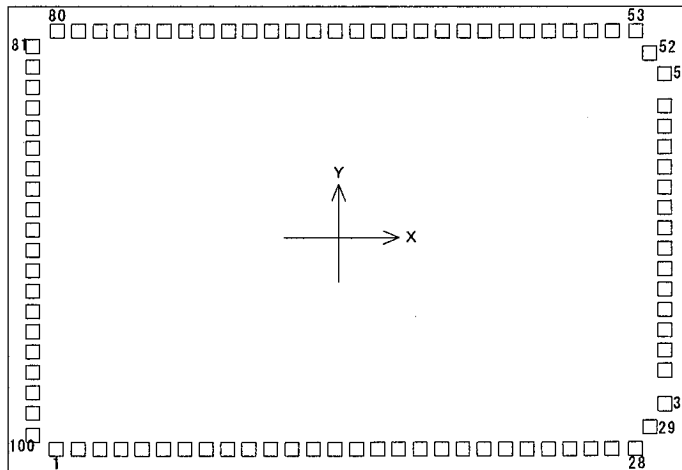


Mar.1999
Ver.1

■ PIN CONFIGURATION



■ PAD LOCATION



PAD size : 90um × 90um



NJU6446

■ TERMINAL DESCRIPTION

Chip Size 3.69mm × 2.61mm(Chip Center X=0um, Y=0um)

PAD No.	Terminal	X=(um)	Y=(um)
1	SEG30	-1599	-1183
2	SEG29	-1479	-1183
3	SEG28	-1359	-1183
4	SEG27	-1239	-1183
5	SEG26	-1119	-1183
6	SEG25	-999	-1183
7	SEG24	-879	-1183
8	SEG23	-759	-1183
9	SEG22	-639	-1183
10	SEG21	-519	-1183
11	SEG20	-399	-1183
12	SEG19	-279	-1183
13	SEG18	-159	-1183
14	SEG17	-39	-1183
15	SEG16	81	-1183
16	SEG15	201	-1183
17	SEG14	321	-1183
18	SEG13	441	-1183
19	SEG12	561	-1183
20	SEG11	681	-1183
21	SEG10	801	-1183
22	SEG9	921	-1183
23	SEG8	1041	-1183
24	SEG7	1161	-1183
25	SEG6	1281	-1183
26	SEG5	1401	-1183
27	SEG4	1521	-1183
28	SEG3	1641	-1183
29	SEG2	1683	-1050
30	SEG1	1723	-920
31	VSSH	1723	-780
32	V0	1723	-660
33	V5	1723	-540
34	V2	1723	-420
35	V3	1723	-300
36	VSS	1723	-180
37	LP	1723	-60
38	NC	Non-PAD	
39	SHL	1723	60
40	SCL	1723	180
41	DI	1723	300
42	DO	1723	420
43	NC	Non-PAD	
44	LM	1723	540
45	NC	Non-PAD	
46	VDD	1723	660
47	NC	Non-PAD	
48	NC	Non-PAD	
49	NC	Non-PAD	
50	DUMMY	1723	780

PAD No.	Terminal	X=(um)	Y=(um)
51	SEG80	1723	920
52	SEG79	1683	1050
53	SEG78	1641	1183
54	SEG77	1521	1183
55	SEG76	1401	1183
56	SEG75	1281	1183
57	SEG74	1161	1183
58	SEG73	1041	1183
59	SEG72	921	1183
60	SEG71	801	1183
61	SEG70	681	1183
62	SEG69	561	1183
63	SEG68	441	1183
64	SEG67	321	1183
65	SEG66	201	1183
66	SEG65	81	1183
67	SEG64	-39	1183
68	SEG63	-159	1183
69	SEG62	-279	1183
70	SEG61	-399	1183
71	SEG60	-519	1183
72	SEG59	-639	1183
73	SEG58	-759	1183
74	SEG57	-879	1183
75	SEG56	-999	1183
76	SEG55	-1119	1183
77	SEG54	-1239	1183
78	SEG53	-1359	1183
79	SEG52	-1479	1183
80	SEG51	-1599	1183
81	SEG50	-1721	1140
82	SEG49	-1721	1020
83	SEG48	-1721	900
84	SEG47	-1721	780
85	SEG46	-1721	660
86	SEG45	-1721	540
87	SEG44	-1721	420
88	SEG43	-1721	300
89	SEG42	-1721	180
90	SEG41	-1721	60
91	SEG40	-1721	-60
92	SEG39	-1721	-180
93	SEG38	-1721	-300
94	SEG37	-1721	-420
95	SEG36	-1721	-540
96	SEG35	-1721	-660
97	SEG34	-1721	-780
98	SEG33	-1721	-900
99	SEG32	-1721	-1020
100	SEG31	-1721	-1140

New Japan Radio Co., Ltd.

■ TERMINAL DESCRIPTION

No	SYMBOL	FUNCTION
1~30 51~100	SEG ₃₀ ~SEG ₁ SEG ₈₀ ~SEG ₃₁	LCD segment driving terminal. Each terminal corresponds to each bit of shift register
41	DI	Data input terminal. The DI terminal is fixed the input terminal regardless the shift direction. Display data is input synchronized with the clock signal.
42	DO	Data output terminal. The DO terminal is fixed the output terminal regardless the shift direction. The data is output synchronized with the clock signal.
40	SCL	Shift register clock pulse input terminal. The data is shifted in the shift register by the falling edge of the clock pulse. A data setup time and hold time are required between data input and SCL. Clock pulse rising time and falling time should be set less than 50ns (MAX) respectively.
39	SHL	Shift direction select terminal. "H" : Shift direction is from 80th bit to 1st bit. "L" : Shift direction is from 1st bit to 80th bit. The DI and DO terminals are fixed input and output terminal respectively regardless this terminal input level.
37	LP	Latch pulse input terminal. The data in the shift register is latched to the Latch by this signal. "H" : Data writing, "L" : Data latch
44	LM	Alternate signal input for LCD driving.
46,36	V _{DD} , V _{SS}	Power supply terminal (connect to the controller's V _{DD} terminal) Power supply terminal (connect to the controller's V _{SS} terminal)
32,34,35, 33,31	V ₀ , V ₂ , V ₃ , V ₅ , V _{SSH}	LCD driving power source terminals. V _{DD} ≥ V ₀ ≥ V ₂ ≥ V ₃ ≥ V ₅ ≥ V _{SSH}
38,43,45, 47~50	NC	Non connection.(Normally open)

■ FUNCTIONAL DESCRIPTION

(1)Shift register control

The 80-bit shift register is a bidirectional register.

The shift direction of 80-bit bidirectional shift register is shown below:

Control Terminal	Input	Shift Direction
SHL	"H"	80→1
	"L"	1→80

Note) DI and DO terminals are fixed input and output terminal respectively regardless the SHL input level.

(2)LCD driver output truth table

Input Data	Selection/ Non-selection	LM	Driver Output (SEG1 to SEG80)
"H"	Selection	H	V5
		L	V0
"L"	Non-selection	H	V3
		L	V2

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage(1)	V _{DD}	-0.3~+7.0	V
Supply Voltage(2) Note1)	V ₀ , V ₂ , V ₃ , V ₅ , V _{SSH}	V _{DD} -11~V _{DD} +0.3	V
Input Voltage	V _{IN}	-0.3~V _{DD} +0.3	V
Operating Temperature	T _{opr}	-30~+80	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note 1) The relation : V_{DD} ≥ V₀ ≥ V₂ ≥ V₃ ≥ V₅ ≥ V_{SSH} must be maintained.

■ ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5V ± 10%, Ta=20 ~ +75°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Note1)	V _{IH}		0.8V _{DD}		V _{DD}	V
	V _{IL}				0.2V _{DD}	V
Input Current Note1)	I _{IH}	V _{IH} =V _{DD}			1	μA
	I _{IL}	V _{IL} =0V	-1			μA
Output Voltage Note2)	V _{OH}	I _o =-40μA	4.2			V
	V _{OL}	I _o =0.4mA			0.4	V
Driver On-resistance Note3)	R _{ON}	I _d =0.05mA			5	kΩ
Operating Current (Logic Part)	I _{SSO}	(LM,LP)=130us cycle SCL=1.5MHz Every one bit Inverted Data. No Load.		1.1	1.5	mA
Operating Current (LCD Driver Part)	I _{SSHO}	(LM,LP)=130us cycle SCL=1.5MHz Every one bit Inverted Data. No Load.		70	100	μA
LCD Driving Voltage	V _{LCD}	V _{SSH} Terminal, V _{DD} =5V	V _{DD} -3.0		V _{DD} -10	V

Note 2) Apply to LM, LP, SCL, SHL and DI terminals.

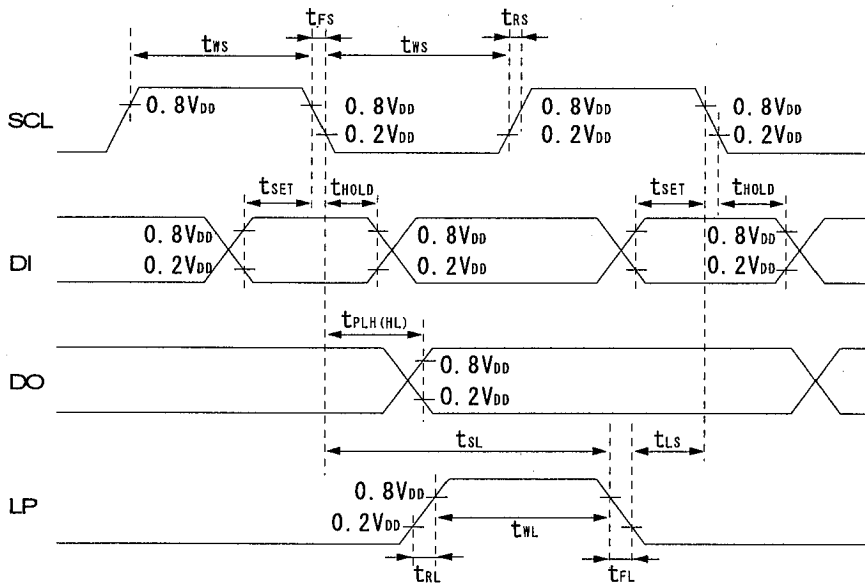
Note 3) Apply to DO terminal.

Note 4) Apply to SEG₁ ~ SEG₈₀ terminals.

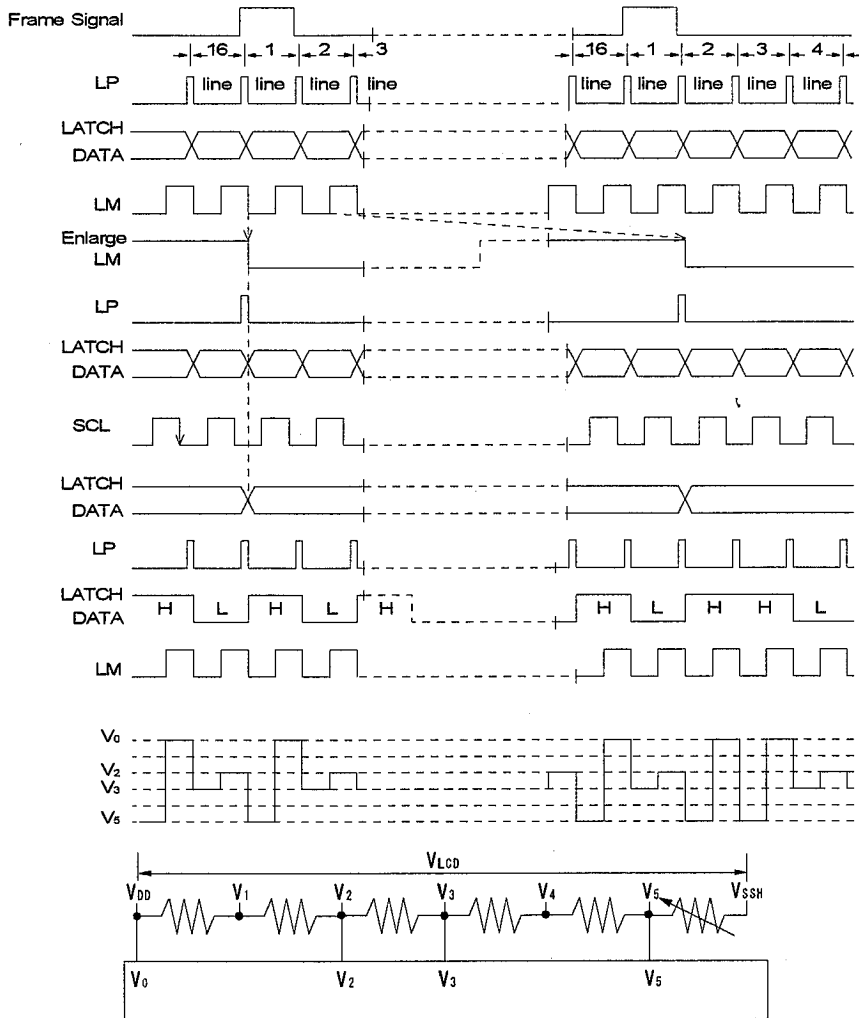
AC Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Time	$t_{PLH(HL)}$		-	-	250	ns
Maximum Operating Frequency	f_{SCL}	Duty=50%	3.3	-	-	MHz
SCL Pulse Width	t_{WS}		125	-	-	ns
LP Pulse Width	t_{WL}		125	-	-	ns
Set Up Time	t_{SET}		50	-	-	ns
SCL → LP Time	t_{SL}		250	-	-	ns
LP → SCL Time	t_{LS}		0	-	-	ns
Data Hold Time	t_{HOLD}		50	-	-	ns
SCL Rise, Fall Time	t_{RS}, t_{FS}		-	-	50	ns
LP Rise, Fall Time	t_{RL}, t_{FL}		-	-	1	us

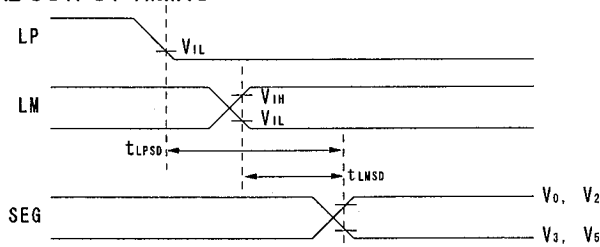
■ AC CHARACTERISTICS TIMING CHART



■ TIMING CHART
1/5 Bias, 1/16 Duty Ratio



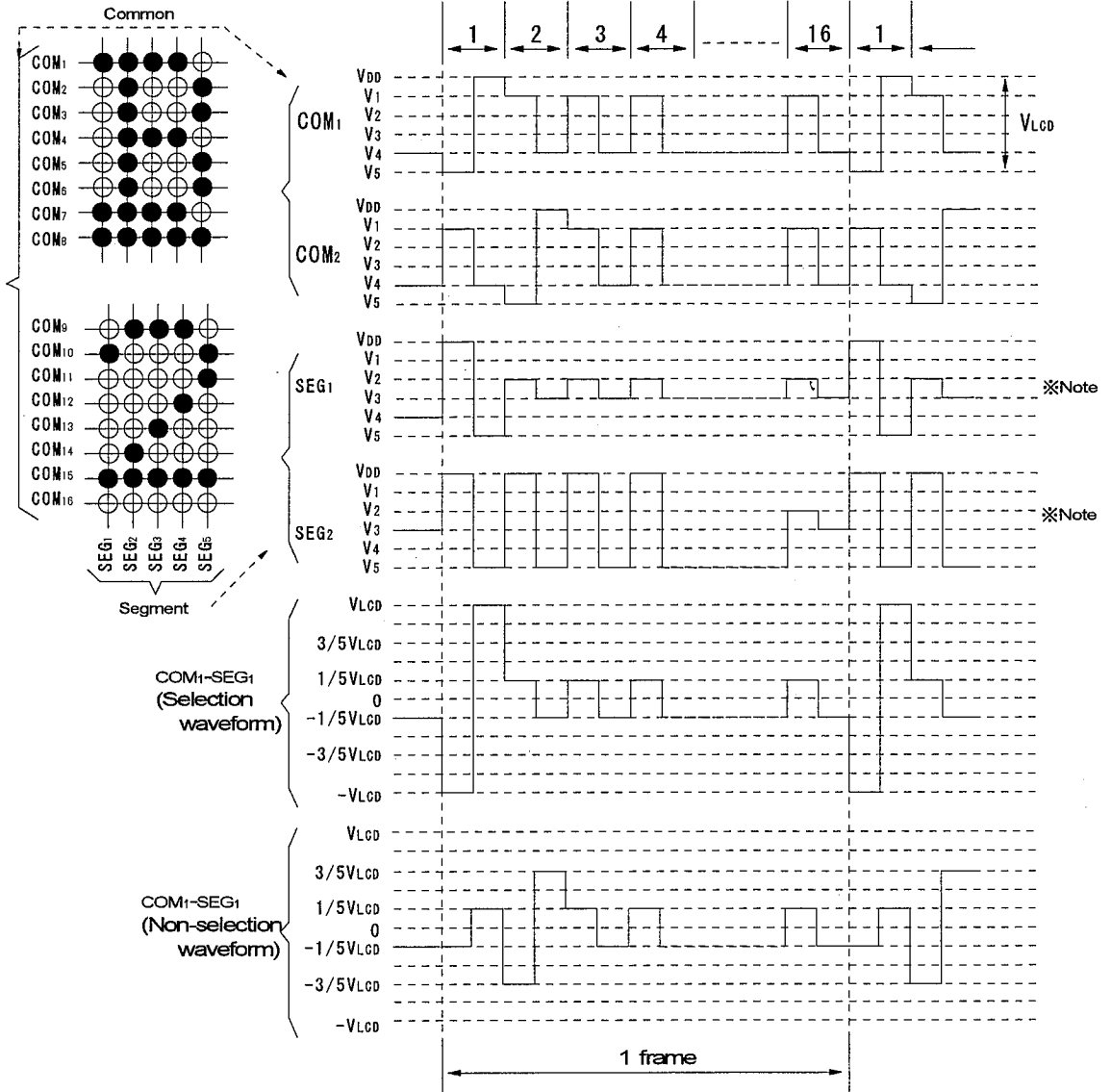
■ SEGMENT SIGNAL OUTPUT TIMING



PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
LP-SEG Output Delay Time	tLPSD	CL=100pF	-	-	4.5	us
LM-SEG Output Delay Time	tLMSD	CL=100pF	-	-	4.5	us

■ LCD DRIVING WAVEFORM EXAMPLE

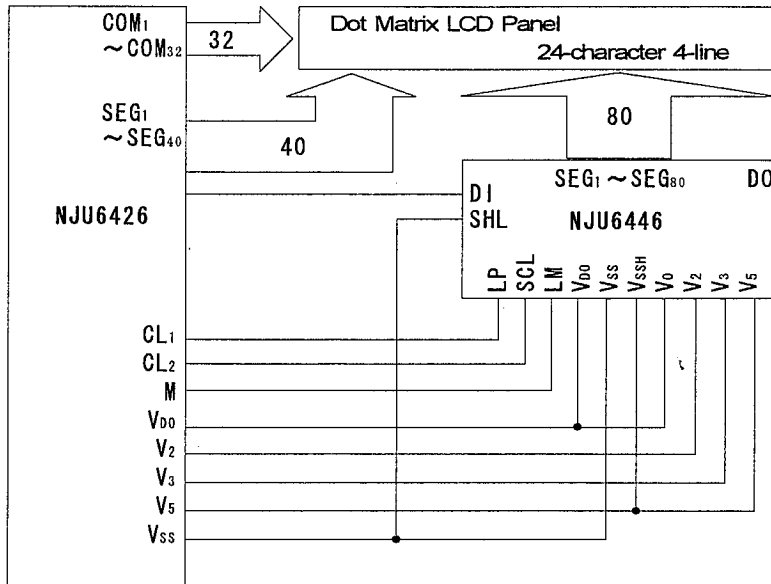
1/5 Bias, 1/16 Duty Ratio



※ Note : In case of V0 terminal connected to the V_{DD}.

■ APPLICATION CIRCUIT

24-character 4-line Display Example (NJU6426 + NJU6446)



MEMO

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