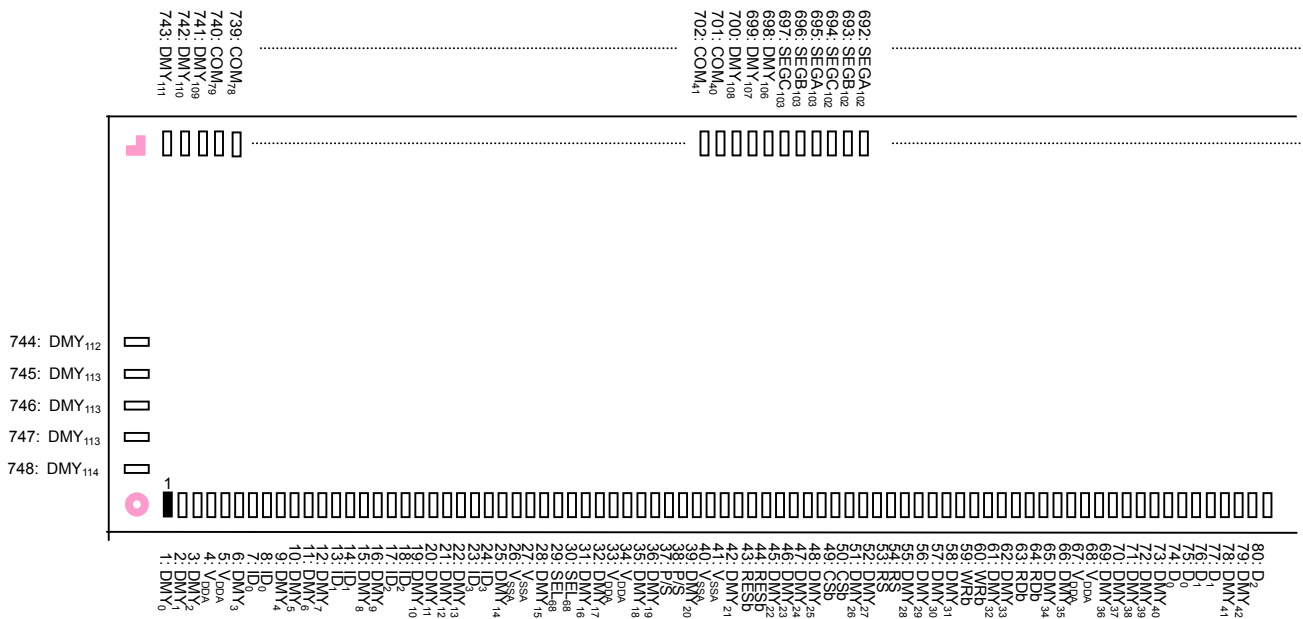


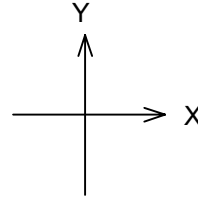
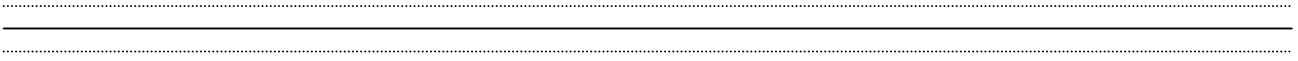
NJU6818

■ PAD LOCATION



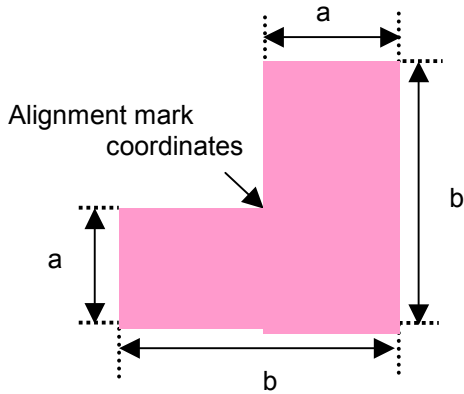
Note 1) The same name PADs are shorted mutually in the LSI.
 Note 2) The DMY PADs are electrically open.

- Chip Center : X= 0μm, Y= 0μm
- Chip Size : 19.25mm x 2.50mm
- Chip Thickness : 625μm ± 25μm
- Bump Size : 26μm x 120μm
- Bump Pitch : 45μm(Min)
- Bump high : 17.5μm(Typ.)
- Bump Material : Au



81: D ₂	82: D ₁	83: D ₄	84: DM _Y 43	85: DM _Y 44	86: DM _Y 45	87: D ₄	88: D ₁	89: D ₅	90: DM _Y 46	91: DM _Y 48	92: D ₅	93: D ₆	94: D ₁	95: DM _Y 47	96: V _{SSA}	97: V _{SSA}	98: DM _Y 48	99: V _{SSA}	100: D ₈	101: D ₈	102: D ₈	103: D ₈	104: DM _Y 49	105: DM _Y 50	106: D ₁₀	107: D ₁₀	108: D ₁₁	109: D ₁₁	110: DM _Y 51	111: DM _Y 52	112: D ₁₂	113: D ₁₂	114: D ₉	115: D ₉	116: DM _Y 54	117: DM _Y 54	118: D ₁₄	119: D ₁₄	120: D ₁₅	121: D ₁₅	122: DM _Y 55	123: V _{DD}	131: V _{DD}	132: DM _Y 56	133: CL	134: CL	135: FL _M	136: FL _M	137: DM _Y 57	138: DM _Y 58	139: ER	140: ER	141: CL _K	142: CL _K	143: DM _Y 59	144: DM _Y 60	145: OS _{C1}	146: OS _{C1}	147: DM _Y 61	148: DM _Y 62	149: OS _{C2}	150: OS _{C2}	151: V _{SS}	159: V _{SS}	160: DM _Y 63	161: V _{SS}	168: V _{DD}	169: DM _Y 64	170: V _{DD}	177: V ₁	178: V ₁	185: V ₂	186: DM _Y 66
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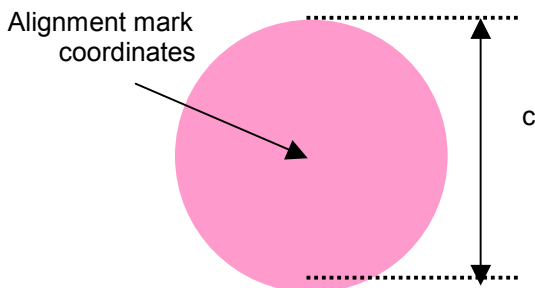
● Alignment mark 1



a : 25μm
b : 50μm

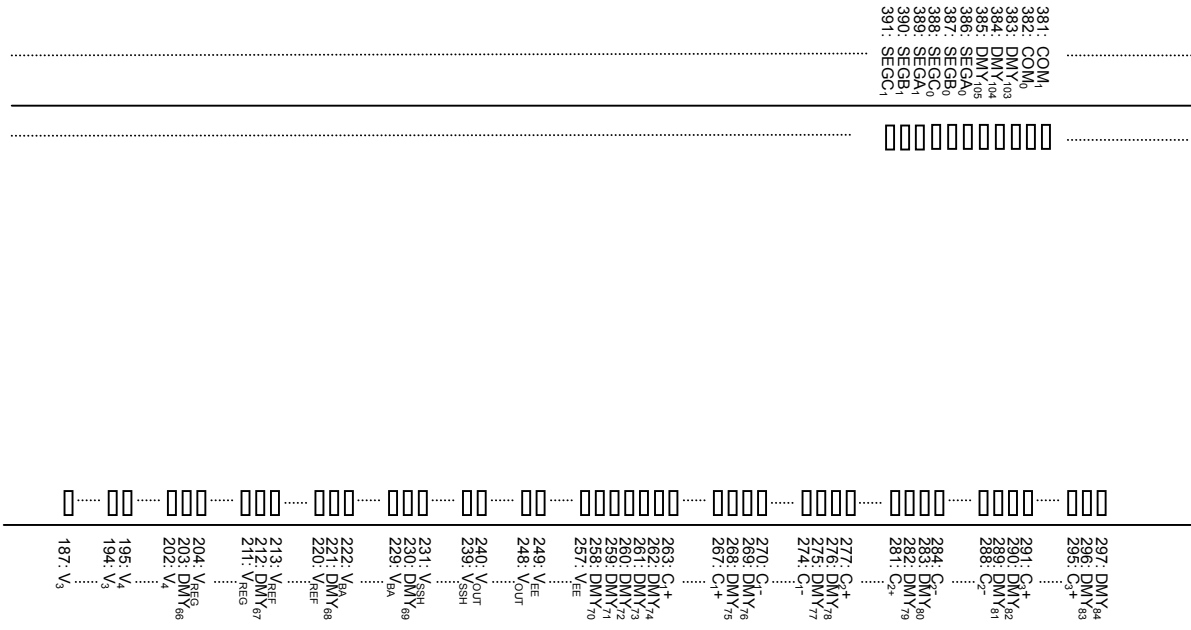
Alignment mark coordinates
(-9445, 1070)
(9445, -1070)

● Alignment mark 2

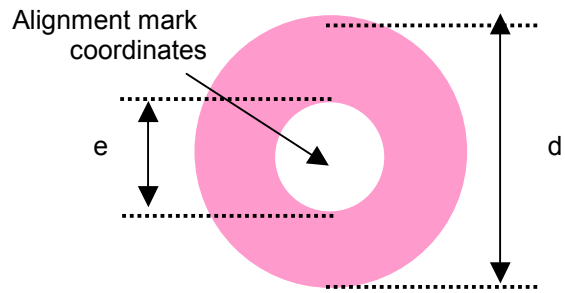


a : 50μm

Alignment mark coordinates
(9257, -1068)

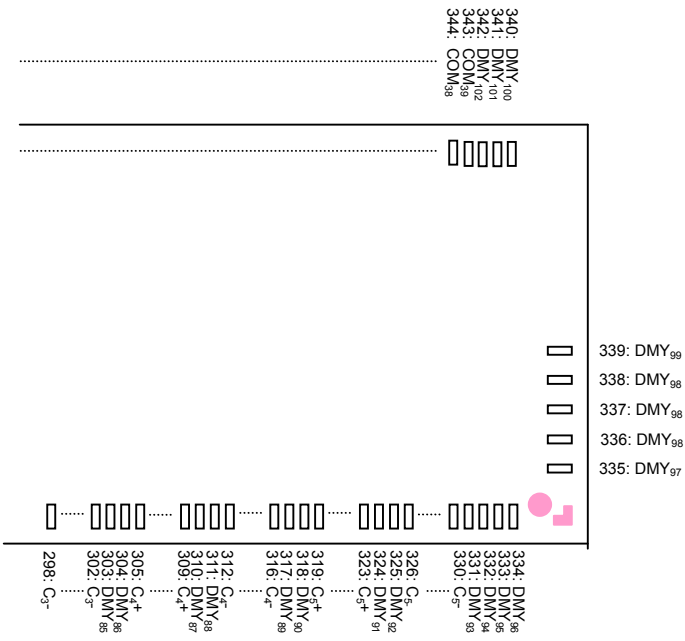


- Alignment mark 3



d : 50 μ m
e : 20 μ m

Alignment mark coordinates
(-9257, -1068)



■ PAD COORDINATES 1

Chip Size 19250μm x 2500μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
1	DMY ₀	-9067.5	-1055	52	DMY ₂₇	-6772.5	-1055	103	D ₉	-3487.5	-1055
2	DMY ₁	-9022.5	-1055	53	RS	-6727.5	-1055	104	DMY ₄₉	-3442.5	-1055
3	DMY ₂	-8977.5	-1055	54	RS	-6682.5	-1055	105	DMY ₅₀	-3307.5	-1055
4	V _{DDA}	-8932.5	-1055	55	DMY ₂₈	-6637.5	-1055	106	D ₁₀	-3262.5	-1055
5	V _{DDA}	-8887.5	-1055	56	DMY ₂₉	-6592.5	-1055	107	D ₁₀	-3217.5	-1055
6	DMY ₃	-8842.5	-1055	57	DMY ₃₀	-6547.5	-1055	108	D ₁₁	-3082.5	-1055
7	ID ₀	-8797.5	-1055	58	DMY ₃₁	-6502.5	-1055	109	D ₁₁	-3037.5	-1055
8	ID ₀	-8752.5	-1055	59	WRb	-6457.5	-1055	110	DMY ₅₁	-2992.5	-1055
9	DMY ₄	-8707.5	-1055	60	WRb	-6412.5	-1055	111	DMY ₅₂	-2857.5	-1055
10	DMY ₅	-8662.5	-1055	61	DMY ₃₂	-6367.5	-1055	112	D ₁₂	-2812.5	-1055
11	DMY ₆	-8617.5	-1055	62	DMY ₃₃	-6322.5	-1055	113	D ₁₂	-2767.5	-1055
12	DMY ₇	-8572.5	-1055	63	RD _b	-6277.5	-1055	114	D ₁₃	-2632.5	-1055
13	ID ₁	-8527.5	-1055	64	RD _b	-6232.5	-1055	115	D ₁₃	-2587.5	-1055
14	ID ₁	-8482.5	-1055	65	DMY ₃₄	-6187.5	-1055	116	DMY ₅₃	-2542.5	-1055
15	DMY ₈	-8437.5	-1055	66	DMY ₃₅	-6142.5	-1055	117	DMY ₅₄	-2407.5	-1055
16	DMY ₉	-8392.5	-1055	67	V _{DDA}	-6097.5	-1055	118	D ₁₄	-2362.5	-1055
17	ID ₂	-8347.5	-1055	68	V _{DDA}	-6052.5	-1055	119	D ₁₄	-2317.5	-1055
18	ID ₂	-8302.5	-1055	69	DMY ₃₆	-6007.5	-1055	120	D ₁₅	-2182.5	-1055
19	DMY ₁₀	-8257.5	-1055	70	DMY ₃₇	-5962.5	-1055	121	D ₁₅	-2137.5	-1055
20	DMY ₁₁	-8212.5	-1055	71	DMY ₃₈	-5917.5	-1055	122	DMY ₅₅	-2092.5	-1055
21	DMY ₁₂	-8167.5	-1055	72	DMY ₃₉	-5872.5	-1055	123	V _{DD}	-1957.5	-1055
22	DMY ₁₃	-8122.5	-1055	73	DMY ₄₀	-5737.5	-1055	124	V _{DD}	-1912.5	-1055
23	ID ₃	-8077.5	-1055	74	D ₀ /SCL	-5692.5	-1055	125	V _{DD}	-1867.5	-1055
24	ID ₃	-8032.5	-1055	75	D ₀ /SCL	-5647.5	-1055	126	V _{DD}	-1822.5	-1055
25	DMY ₁₄	-7987.5	-1055	76	D ₁ /SDA	-5512.5	-1055	127	V _{DD}	-1777.5	-1055
26	V _{SSA}	-7942.5	-1055	77	D ₁ /SDA	-5467.5	-1055	128	V _{DD}	-1732.5	-1055
27	V _{SSA}	-7897.5	-1055	78	DMY ₄₁	-5422.5	-1055	129	V _{DD}	-1687.5	-1055
28	DMY ₁₅	-7852.5	-1055	79	DMY ₄₂	-5287.5	-1055	130	V _{DD}	-1642.5	-1055
29	SEL ₆₈	-7807.5	-1055	80	D ₂	-5242.5	-1055	131	V _{DD}	-1597.5	-1055
30	SEL ₆₈	-7762.5	-1055	81	D ₂	-5197.5	-1055	132	DMY ₅₆	-1372.5	-1055
31	DMY ₁₆	-7717.5	-1055	82	D ₃ /SMODE	-5062.5	-1055	133	CL	-1327.5	-1055
32	DMY ₁₇	-7672.5	-1055	83	D ₃ /SMODE	-5017.5	-1055	134	CL	-1282.5	-1055
33	V _{DDA}	-7627.5	-1055	84	DMY ₄₃	-4972.5	-1055	135	FLM	-1147.5	-1055
34	V _{DDA}	-7582.5	-1055	85	DMY ₄₄	-4837.5	-1055	136	FLM	-1102.5	-1055
35	DMY ₁₈	-7537.5	-1055	86	D ₄ /SPOL	-4792.5	-1055	137	DMY ₅₇	-1057.5	-1055
36	DMY ₁₉	-7492.5	-1055	87	D ₄ /SPOL	-4747.5	-1055	138	DMY ₅₈	-922.5	-1055
37	P/S	-7447.5	-1055	88	D ₅	-4612.5	-1055	139	FR	-877.5	-1055
38	P/S	-7402.5	-1055	89	D ₅	-4567.5	-1055	140	FR	-832.5	-1055
39	DMY ₂₀	-7357.5	-1055	90	DMY ₄₅	-4522.5	-1055	141	CLK	-697.5	-1055
40	V _{SSA}	-7312.5	-1055	91	DMY ₄₆	-4387.5	-1055	142	CLK	-652.5	-1055
41	V _{SSA}	-7267.5	-1055	92	D ₆	-4342.5	-1055	143	DMY ₅₉	-607.5	-1055
42	DMY ₂₁	-7222.5	-1055	93	D ₆	-4297.5	-1055	144	DMY ₆₀	-472.5	-1055
43	RES _b	-7177.5	-1055	94	D ₇	-4162.5	-1055	145	OSC ₁	-427.5	-1055
44	RES _b	-7132.5	-1055	95	D ₇	-4117.5	-1055	146	OSC ₁	-382.5	-1055
45	DMY ₂₂	-7087.5	-1055	96	DMY ₄₇	-4072.5	-1055	147	DMY ₆₁	-337.5	-1055
46	DMY ₂₃	-7042.5	-1055	97	V _{SSA}	-3937.5	-1055	148	DMY ₆₂	-292.5	-1055
47	DMY ₂₄	-6997.5	-1055	98	V _{SSA}	-3892.5	-1055	149	OSC ₂	-157.5	-1055
48	DMY ₂₅	-6952.5	-1055	99	DMY ₄₈	-3757.5	-1055	150	OSC ₂	-112.5	-1055
49	CS _b	-6907.5	-1055	100	D ₈	-3712.5	-1055	151	V _{SS}	22.5	-1055
50	CS _b	-6862.5	-1055	101	D ₈	-3667.5	-1055	152	V _{SS}	67.5	-1055
51	DMY ₂₆	-6817.5	-1055	102	D ₉	-3532.5	-1055	153	V _{SS}	112.5	-1055

■ PAD COORDINATES 2

Chip Size 19250μm x 2500μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
154	V _{SS}	157.5	-1055	205	V _{REG}	2812.5	-1055	256	V _{EE}	5467.5	-1055
155	V _{SS}	202.5	-1055	206	V _{REG}	2857.5	-1055	257	V _{EE}	5512.5	-1055
156	V _{SS}	247.5	-1055	207	V _{REG}	2902.5	-1055	258	DMY ₇₀	5647.5	-1055
157	V _{SS}	292.5	-1055	208	V _{REG}	2947.5	-1055	259	DMY ₇₁	5692.5	-1055
158	V _{SS}	337.5	-1055	209	V _{REG}	2992.5	-1055	260	DMY ₇₂	5737.5	-1055
159	V _{SS}	382.5	-1055	210	V _{REG}	3037.5	-1055	261	DMY ₇₃	5782.5	-1055
160	DMY ₆₃	517.5	-1055	211	V _{REG}	3082.5	-1055	262	DMY ₇₄	5827.5	-1055
161	V _{LCD}	652.5	-1055	212	DMY ₆₇	3127.5	-1055	263	C1+	5872.5	-1055
162	V _{LCD}	697.5	-1055	213	V _{REF}	3172.5	-1055	264	C1+	5917.5	-1055
163	V _{LCD}	742.5	-1055	214	V _{REF}	3217.5	-1055	265	C1+	5962.5	-1055
164	V _{LCD}	787.5	-1055	215	V _{REF}	3262.5	-1055	266	C1+	6007.5	-1055
165	V _{LCD}	832.5	-1055	216	V _{REF}	3307.5	-1055	267	C1+	6052.5	-1055
166	V _{LCD}	877.5	-1055	217	V _{REF}	3352.5	-1055	268	DMY ₇₅	6097.5	-1055
167	V _{LCD}	922.5	-1055	218	V _{REF}	3397.5	-1055	269	DMY ₇₆	6142.5	-1055
168	V _{LCD}	967.5	-1055	219	V _{REF}	3442.5	-1055	270	C1-	6187.5	-1055
169	DMY ₆₄	1012.5	-1055	220	V _{REF}	3487.5	-1055	271	C1-	6232.5	-1055
170	V ₁	1057.5	-1055	221	DMY ₆₈	3532.5	-1055	272	C1-	6277.5	-1055
171	V ₁	1102.5	-1055	222	V _{BA}	3577.5	-1055	273	C1-	6322.5	-1055
172	V ₁	1147.5	-1055	223	V _{BA}	3622.5	-1055	274	C1-	6367.5	-1055
173	V ₁	1192.5	-1055	224	V _{BA}	3667.5	-1055	275	DMY ₇₇	6412.5	-1055
174	V ₁	1237.5	-1055	225	V _{BA}	3712.5	-1055	276	DMY ₇₈	6457.5	-1055
175	V ₁	1282.5	-1055	226	V _{BA}	3757.5	-1055	277	C2+	6502.5	-1055
176	V ₁	1327.5	-1055	227	V _{BA}	3802.5	-1055	278	C2+	6547.5	-1055
177	V ₁	1372.5	-1055	228	V _{BA}	3847.5	-1055	279	C2+	6592.5	-1055
178	V ₂	1507.5	-1055	229	V _{BA}	3892.5	-1055	280	C2+	6637.5	-1055
179	V ₂	1552.5	-1055	230	DMY ₆₉	3937.5	-1055	281	C2+	6682.5	-1055
180	V ₂	1597.5	-1055	231	V _{SSH}	3982.5	-1055	282	DMY ₇₉	6727.5	-1055
181	V ₂	1642.5	-1055	232	V _{SSH}	4027.5	-1055	283	DMY ₈₀	6772.5	-1055
182	V ₂	1687.5	-1055	233	V _{SSH}	4072.5	-1055	284	C2-	6817.5	-1055
183	V ₂	1732.5	-1055	234	V _{SSH}	4117.5	-1055	285	C2-	6862.5	-1055
184	V ₂	1777.5	-1055	235	V _{SSH}	4162.5	-1055	286	C2-	6907.5	-1055
185	V ₂	1822.5	-1055	236	V _{SSH}	4207.5	-1055	287	C2-	6952.5	-1055
186	DMY ₆₅	1867.5	-1055	237	V _{SSH}	4252.5	-1055	288	C2-	6997.5	-1055
187	V ₃	1912.5	-1055	238	V _{SSH}	4297.5	-1055	289	DMY ₈₁	7042.5	-1055
188	V ₃	1957.5	-1055	239	V _{SSH}	4342.5	-1055	290	DMY ₈₂	7087.5	-1055
189	V ₃	2002.5	-1055	240	V _{OUT}	4567.5	-1055	291	C3+	7132.5	-1055
190	V ₃	2047.5	-1055	241	V _{OUT}	4612.5	-1055	292	C3+	7177.5	-1055
191	V ₃	2092.5	-1055	242	V _{OUT}	4657.5	-1055	293	C3+	7222.5	-1055
192	V ₃	2137.5	-1055	243	V _{OUT}	4702.5	-1055	294	C3+	7267.5	-1055
193	V ₃	2182.5	-1055	244	V _{OUT}	4747.5	-1055	295	C3+	7312.5	-1055
194	V ₃	2227.5	-1055	245	V _{OUT}	4792.5	-1055	296	DMY ₈₃	7357.5	-1055
195	V ₄	2362.5	-1055	246	V _{OUT}	4837.5	-1055	297	DMY ₈₄	7402.5	-1055
196	V ₄	2407.5	-1055	247	V _{OUT}	4882.5	-1055	298	C3-	7447.5	-1055
197	V ₄	2452.5	-1055	248	V _{OUT}	4927.5	-1055	299	C3-	7492.5	-1055
198	V ₄	2497.5	-1055	249	V _{EE}	5152.5	-1055	300	C3-	7537.5	-1055
199	V ₄	2542.5	-1055	250	V _{EE}	5197.5	-1055	301	C3-	7582.5	-1055
200	V ₄	2587.5	-1055	251	V _{EE}	5242.5	-1055	302	C3-	7627.5	-1055
201	V ₄	2632.5	-1055	252	V _{EE}	5287.5	-1055	303	DMY ₈₅	7672.5	-1055
202	V ₄	2677.5	-1055	253	V _{EE}	5332.5	-1055	304	DMY ₈₆	7717.5	-1055
203	DMY ₆₆	2722.5	-1055	254	V _{EE}	5377.5	-1055	305	C4+	7762.5	-1055
204	V _{REG}	2767.5	-1055	255	V _{EE}	5422.5	-1055	306	C4+	7807.5	-1055

■ PAD COORDINATES 3

Chip Size 19250μm x 2500μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
307	C ₄₊	7852.5	-1055	358	COM ₂₄	8257.5	1055	409	SEGC ₇	5962.5	1055
308	C ₄₊	7897.5	-1055	359	COM ₂₃	8212.5	1055	410	SEGA ₈	5917.5	1055
309	C ₄₊	7942.5	-1055	360	COM ₂₂	8167.5	1055	411	SEGB ₈	5872.5	1055
310	DMY ₈₇	7987.5	-1055	361	COM ₂₁	8122.5	1055	412	SEGC ₈	5827.5	1055
311	DMY ₈₈	8032.5	-1055	362	COM ₂₀	8077.5	1055	413	SEGA ₉	5782.5	1055
312	C ₄₋	8077.5	-1055	363	COM ₁₉	8032.5	1055	414	SEGB ₉	5737.5	1055
313	C ₄₋	8122.5	-1055	364	COM ₁₈	7987.5	1055	415	SEGC ₉	5692.5	1055
314	C ₄₋	8167.5	-1055	365	COM ₁₇	7942.5	1055	416	SEGA ₁₀	5647.5	1055
315	C ₄₋	8212.5	-1055	366	COM ₁₆	7897.5	1055	417	SEGB ₁₀	5602.5	1055
316	C ₄₋	8257.5	-1055	367	COM ₁₅	7852.5	1055	418	SEGC ₁₀	5557.5	1055
317	DMY ₈₉	8302.5	-1055	368	COM ₁₄	7807.5	1055	419	SEGA ₁₁	5512.5	1055
318	DMY ₉₀	8347.5	-1055	369	COM ₁₃	7762.5	1055	420	SEGB ₁₁	5467.5	1055
319	C ₅₊	8392.5	-1055	370	COM ₁₂	7717.5	1055	421	SEGC ₁₁	5422.5	1055
320	C ₅₊	8437.5	-1055	371	COM ₁₁	7672.5	1055	422	SEGA ₁₂	5377.5	1055
321	C ₅₊	8482.5	-1055	372	COM ₁₀	7627.5	1055	423	SEGB ₁₂	5332.5	1055
322	C ₅₊	8527.5	-1055	373	COM ₉	7582.5	1055	424	SEGC ₁₂	5287.5	1055
323	C ₅₊	8572.5	-1055	374	COM ₈	7537.5	1055	425	SEGA ₁₃	5242.5	1055
324	DMY ₉₁	8617.5	-1055	375	COM ₇	7492.5	1055	426	SEGB ₁₃	5197.5	1055
325	DMY ₉₂	8662.5	-1055	376	COM ₆	7447.5	1055	427	SEGC ₁₃	5152.5	1055
326	C ₅₋	8707.5	-1055	377	COM ₅	7402.5	1055	428	SEGA ₁₄	5107.5	1055
327	C ₅₋	8752.5	-1055	378	COM ₄	7357.5	1055	429	SEGB ₁₄	5062.5	1055
328	C ₅₋	8797.5	-1055	379	COM ₃	7312.5	1055	430	SEGC ₁₄	5017.5	1055
329	C ₅₋	8842.5	-1055	380	COM ₂	7267.5	1055	431	SEGA ₁₅	4972.5	1055
330	C ₅₋	8887.5	-1055	381	COM ₁	7222.5	1055	432	SEGB ₁₅	4927.5	1055
331	DMY ₉₃	8932.5	-1055	382	COM ₀	7177.5	1055	433	SEGC ₁₅	4882.5	1055
332	DMY ₉₄	8977.5	-1055	383	DMY ₁₀₃	7132.5	1055	434	SEGA ₁₆	4837.5	1055
333	DMY ₉₅	9022.5	-1055	384	DMY ₁₀₄	7087.5	1055	435	SEGB ₁₆	4792.5	1055
334	DMY ₉₆	9067.5	-1055	385	DMY ₁₀₅	7042.5	1055	436	SEGC ₁₆	4747.5	1055
335	DMY ₉₇	9430	-964	386	SEGA ₀	6997.5	1055	437	SEGA ₁₇	4702.5	1055
336	DMY ₉₈	9430	-919	387	SEGB ₀	6952.5	1055	438	SEGB ₁₇	4657.5	1055
337	DMY ₉₈	9430	-874	388	SEGC ₀	6907.5	1055	439	SEGC ₁₇	4612.5	1055
338	DMY ₉₈	9430	-829	389	SEGA ₁	6862.5	1055	440	SEGA ₁₈	4567.5	1055
339	DMY ₉₉	9430	-784	390	SEGB ₁	6817.5	1055	441	SEGB ₁₈	4522.5	1055
340	DMY ₁₀₀	9067.5	1055	391	SEGC ₁	6772.5	1055	442	SEGC ₁₈	4477.5	1055
341	DMY ₁₀₁	9022.5	1055	392	SEGA ₂	6727.5	1055	443	SEGA ₁₉	4432.5	1055
342	DMY ₁₀₂	8977.5	1055	393	SEGB ₂	6682.5	1055	444	SEGB ₁₉	4387.5	1055
343	COM ₃₉	8932.5	1055	394	SEGC ₂	6637.5	1055	445	SEGC ₁₉	4342.5	1055
344	COM ₃₈	8887.5	1055	395	SEGA ₃	6592.5	1055	446	SEGA ₂₀	4297.5	1055
345	COM ₃₇	8842.5	1055	396	SEGB ₃	6547.5	1055	447	SEGB ₂₀	4252.5	1055
346	COM ₃₆	8797.5	1055	397	SEGC ₃	6502.5	1055	448	SEGC ₂₀	4207.5	1055
347	COM ₃₅	8752.5	1055	398	SEGA ₄	6457.5	1055	449	SEGA ₂₁	4162.5	1055
348	COM ₃₄	8707.5	1055	399	SEGB ₄	6412.5	1055	450	SEGB ₂₁	4117.5	1055
349	COM ₃₃	8662.5	1055	400	SEGC ₄	6367.5	1055	451	SEGC ₂₁	4072.5	1055
350	COM ₃₂	8617.5	1055	401	SEGA ₅	6322.5	1055	452	SEGA ₂₂	4027.5	1055
351	COM ₃₁	8572.5	1055	402	SEGB ₅	6277.5	1055	453	SEGB ₂₂	3982.5	1055
352	COM ₃₀	8527.5	1055	403	SEGC ₅	6232.5	1055	454	SEGC ₂₂	3937.5	1055
353	COM ₂₉	8482.5	1055	404	SEGA ₆	6187.5	1055	455	SEGA ₂₃	3892.5	1055
354	COM ₂₈	8437.5	1055	405	SEGB ₆	6142.5	1055	456	SEGB ₂₃	3847.5	1055
355	COM ₂₇	8392.5	1055	406	SEGC ₆	6097.5	1055	457	SEGC ₂₃	3802.5	1055
356	COM ₂₆	8347.5	1055	407	SEGA ₇	6052.5	1055	458	SEGA ₂₄	3757.5	1055
357	COM ₂₅	8302.5	1055	408	SEGB ₇	6007.5	1055	459	SEGB ₂₄	3712.5	1055

PAD COORDINATES 4

Chip Size 19250μm x 2500μm (Chip Center 0μm x 0μm)

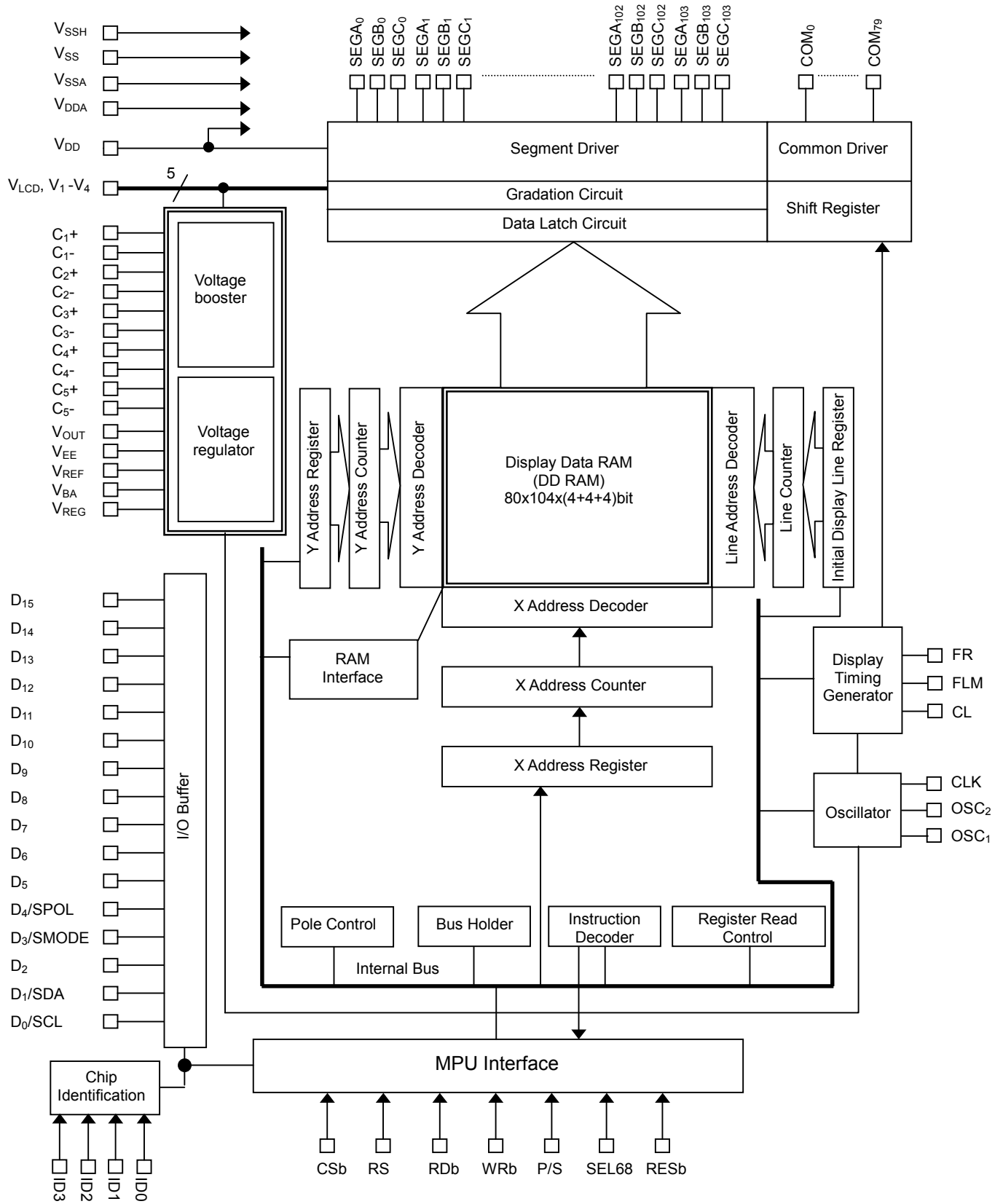
PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
460	SEGC ₂₄	3667.5	1055	511	SEGC ₄₁	1372.5	1055	562	SEGC ₅₈	-922.5	1055
461	SEGA ₂₅	3622.5	1055	512	SEGA ₄₂	1327.5	1055	563	SEGA ₅₉	-967.5	1055
462	SEGB ₂₅	3577.5	1055	513	SEGB ₄₂	1282.5	1055	564	SEGB ₅₉	-1012.5	1055
463	SEGC ₂₅	3532.5	1055	514	SEGC ₄₂	1237.5	1055	565	SEGC ₅₉	-1057.5	1055
464	SEGA ₂₆	3487.5	1055	515	SEGA ₄₃	1192.5	1055	566	SEGA ₆₀	-1102.5	1055
465	SEGB ₂₆	3442.5	1055	516	SEGB ₄₃	1147.5	1055	567	SEGB ₆₀	-1147.5	1055
466	SEGC ₂₆	3397.5	1055	517	SEGC ₄₃	1102.5	1055	568	SEGC ₆₀	-1192.5	1055
467	SEGA ₂₇	3352.5	1055	518	SEGA ₄₄	1057.5	1055	569	SEGA ₆₁	-1237.5	1055
468	SEGB ₂₇	3307.5	1055	519	SEGB ₄₄	1012.5	1055	570	SEGB ₆₁	-1282.5	1055
469	SEGC ₂₇	3262.5	1055	520	SEGC ₄₄	967.5	1055	571	SEGC ₆₁	-1327.5	1055
470	SEGA ₂₈	3217.5	1055	521	SEGA ₄₅	922.5	1055	572	SEGA ₆₂	-1372.5	1055
471	SEGB ₂₈	3172.5	1055	522	SEGB ₄₅	877.5	1055	573	SEGB ₆₂	-1417.5	1055
472	SEGC ₂₈	3127.5	1055	523	SEGC ₄₅	832.5	1055	574	SEGC ₆₂	-1462.5	1055
473	SEGA ₂₉	3082.5	1055	524	SEGA ₄₆	787.5	1055	575	SEGA ₆₃	-1507.5	1055
474	SEGB ₂₉	3037.5	1055	525	SEGB ₄₆	742.5	1055	576	SEGB ₆₃	-1552.5	1055
475	SEGC ₂₉	2992.5	1055	526	SEGC ₄₆	697.5	1055	577	SEGC ₆₃	-1597.5	1055
476	SEGA ₃₀	2947.5	1055	527	SEGA ₄₇	652.5	1055	578	SEGA ₆₄	-1642.5	1055
477	SEGB ₃₀	2902.5	1055	528	SEGB ₄₇	607.5	1055	579	SEGB ₆₄	-1687.5	1055
478	SEGC ₃₀	2857.5	1055	529	SEGC ₄₇	562.5	1055	580	SEGC ₆₄	-1732.5	1055
479	SEGA ₃₁	2812.5	1055	530	SEGA ₄₈	517.5	1055	581	SEGA ₆₅	-1777.5	1055
480	SEGB ₃₁	2767.5	1055	531	SEGB ₄₈	472.5	1055	582	SEGB ₆₅	-1822.5	1055
481	SEGC ₃₁	2722.5	1055	532	SEGC ₄₈	427.5	1055	583	SEGC ₆₅	-1867.5	1055
482	SEGA ₃₂	2677.5	1055	533	SEGA ₄₉	382.5	1055	584	SEGA ₆₆	-1912.5	1055
483	SEGB ₃₂	2632.5	1055	534	SEGB ₄₉	337.5	1055	585	SEGB ₆₆	-1957.5	1055
484	SEGC ₃₂	2587.5	1055	535	SEGC ₄₉	292.5	1055	586	SEGC ₆₆	-2002.5	1055
485	SEGA ₃₃	2542.5	1055	536	SEGA ₅₀	247.5	1055	587	SEGA ₆₇	-2047.5	1055
486	SEGB ₃₃	2497.5	1055	537	SEGB ₅₀	202.5	1055	588	SEGB ₆₇	-2092.5	1055
487	SEGC ₃₃	2452.5	1055	538	SEGC ₅₀	157.5	1055	589	SEGC ₆₇	-2137.5	1055
488	SEGA ₃₄	2407.5	1055	539	SEGA ₅₁	112.5	1055	590	SEGA ₆₈	-2182.5	1055
489	SEGB ₃₄	2362.5	1055	540	SEGB ₅₁	67.5	1055	591	SEGB ₆₈	-2227.5	1055
490	SEGC ₃₄	2317.5	1055	541	SEGC ₅₁	22.5	1055	592	SEGC ₆₈	-2272.5	1055
491	SEGA ₃₅	2272.5	1055	542	SEGA ₅₂	-22.5	1055	593	SEGA ₆₉	-2317.5	1055
492	SEGB ₃₅	2227.5	1055	543	SEGB ₅₂	-67.5	1055	594	SEGB ₆₉	-2362.5	1055
493	SEGC ₃₅	2182.5	1055	544	SEGC ₅₂	-112.5	1055	595	SEGC ₆₉	-2407.5	1055
494	SEGA ₃₆	2137.5	1055	545	SEGA ₅₃	-157.5	1055	596	SEGA ₇₀	-2452.5	1055
495	SEGB ₃₆	2092.5	1055	546	SEGB ₅₃	-202.5	1055	597	SEGB ₇₀	-2497.5	1055
496	SEGC ₃₆	2047.5	1055	547	SEGC ₅₃	-247.5	1055	598	SEGC ₇₀	-2542.5	1055
497	SEGA ₃₇	2002.5	1055	548	SEGA ₅₄	-292.5	1055	599	SEGA ₇₁	-2587.5	1055
498	SEGB ₃₇	1957.5	1055	549	SEGB ₅₄	-337.5	1055	600	SEGB ₇₁	-2632.5	1055
499	SEGC ₃₇	1912.5	1055	550	SEGC ₅₄	-382.5	1055	601	SEGC ₇₁	-2677.5	1055
500	SEGA ₃₈	1867.5	1055	551	SEGA ₅₅	-427.5	1055	602	SEGA ₇₂	-2722.5	1055
501	SEGB ₃₈	1822.5	1055	552	SEGB ₅₅	-472.5	1055	603	SEGB ₇₂	-2767.5	1055
502	SEGC ₃₈	1777.5	1055	553	SEGC ₅₅	-517.5	1055	604	SEGC ₇₂	-2812.5	1055
503	SEGA ₃₉	1732.5	1055	554	SEGA ₅₆	-562.5	1055	605	SEGA ₇₃	-2857.5	1055
504	SEGB ₃₉	1687.5	1055	555	SEGB ₅₆	-607.5	1055	606	SEGB ₇₃	-2902.5	1055
505	SEGC ₃₉	1642.5	1055	556	SEGC ₅₆	-652.5	1055	607	SEGC ₇₃	-2947.5	1055
506	SEGA ₄₀	1597.5	1055	557	SEGA ₅₇	-697.5	1055	608	SEGA ₇₄	-2992.5	1055
507	SEGB ₄₀	1552.5	1055	558	SEGB ₅₇	-742.5	1055	609	SEGB ₇₄	-3037.5	1055
508	SEGC ₄₀	1507.5	1055	559	SEGC ₅₇	-787.5	1055	610	SEGC ₇₄	-3082.5	1055
509	SEGA ₄₁	1462.5	1055	560	SEGA ₅₈	-832.5	1055	611	SEGA ₇₅	-3127.5	1055
510	SEGB ₄₁	1417.5	1055	561	SEGB ₅₈	-877.5	1055	612	SEGB ₇₅	-3172.5	1055

PAD COORDINATES 5

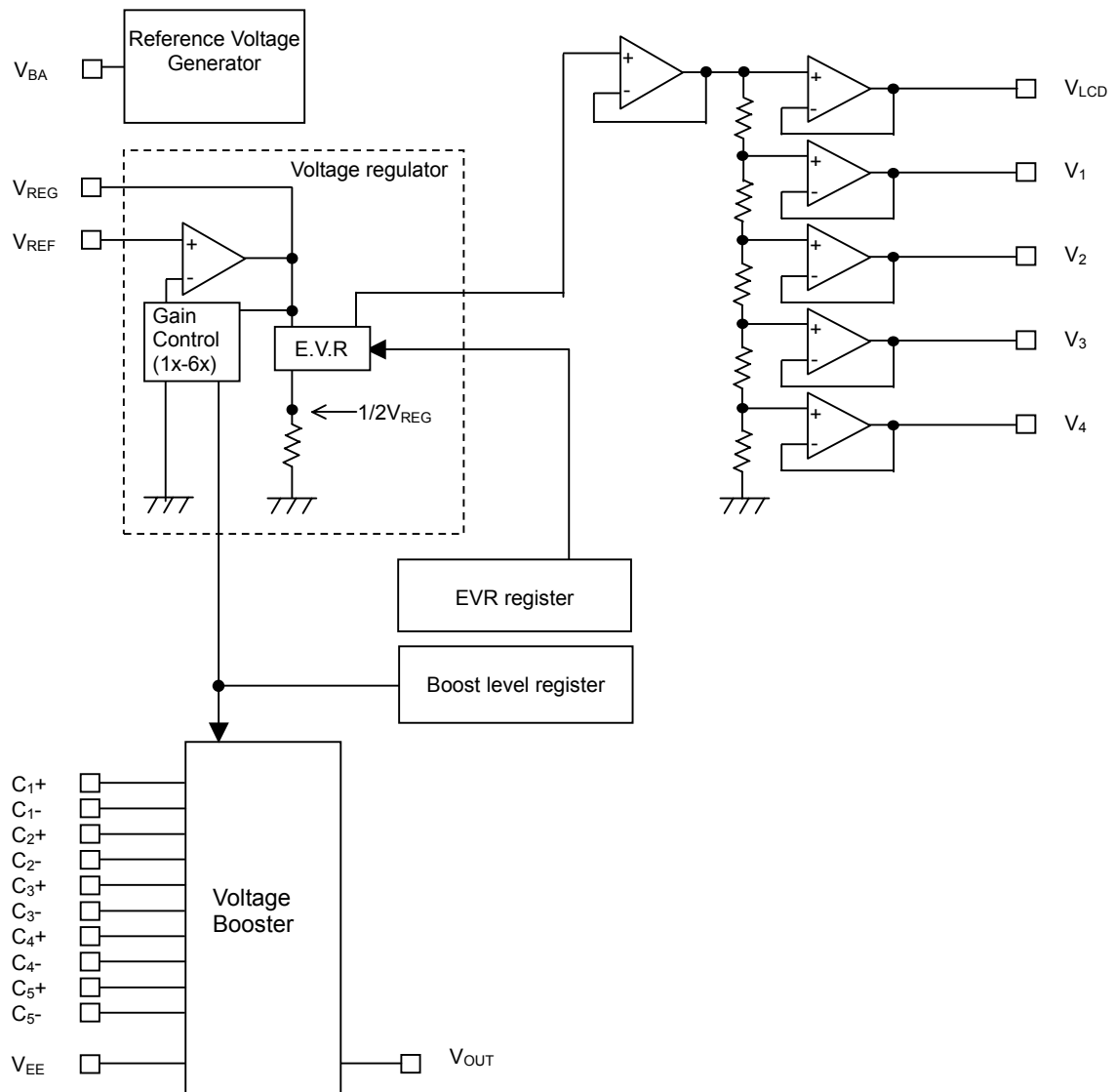
Chip Size 19250μm x 2500μm (Chip Center 0μm x 0μm)

PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)	PAD No.	Terminal	X(μm)	Y(μm)
613	SEGC ₇₅	-3217.5	1055	664	SEGC ₉₂	-5512.5	1055	715	COM ₅₄	-7807.5	1055
614	SEGA ₇₆	-3262.5	1055	665	SEGA ₉₃	-5557.5	1055	716	COM ₅₅	-7852.5	1055
615	SEGB ₇₆	-3307.5	1055	666	SEGB ₉₃	-5602.5	1055	717	COM ₅₆	-7897.5	1055
616	SEGC ₇₆	-3352.5	1055	667	SEGC ₉₃	-5647.5	1055	718	COM ₅₇	-7942.5	1055
617	SEGA ₇₇	-3397.5	1055	668	SEGA ₉₄	-5692.5	1055	719	COM ₅₈	-7987.5	1055
618	SEGB ₇₇	-3442.5	1055	669	SEGB ₉₄	-5737.5	1055	720	COM ₅₉	-8032.5	1055
619	SEGC ₇₇	-3487.5	1055	670	SEGC ₉₄	-5782.5	1055	721	COM ₆₀	-8077.5	1055
620	SEGA ₇₈	-3532.5	1055	671	SEGA ₉₅	-5827.5	1055	722	COM ₆₁	-8122.5	1055
621	SEGB ₇₈	-3577.5	1055	672	SEGB ₉₅	-5872.5	1055	723	COM ₆₂	-8167.5	1055
622	SEGC ₇₈	-3622.5	1055	673	SEGC ₉₅	-5917.5	1055	724	COM ₆₃	-8212.5	1055
623	SEGA ₇₉	-3667.5	1055	674	SEGA ₉₆	-5962.5	1055	725	COM ₆₄	-8257.5	1055
624	SEGB ₇₉	-3712.5	1055	675	SEGB ₉₆	-6007.5	1055	726	COM ₆₅	-8302.5	1055
625	SEGC ₇₉	-3757.5	1055	676	SEGC ₉₆	-6052.5	1055	727	COM ₆₆	-8347.5	1055
626	SEGA ₈₀	-3802.5	1055	677	SEGA ₉₇	-6097.5	1055	728	COM ₆₇	-8392.5	1055
627	SEGB ₈₀	-3847.5	1055	678	SEGB ₉₇	-6142.5	1055	729	COM ₆₈	-8437.5	1055
628	SEGC ₈₀	-3892.5	1055	679	SEGC ₉₇	-6187.5	1055	730	COM ₆₉	-8482.5	1055
629	SEGA ₈₁	-3937.5	1055	680	SEGA ₉₈	-6232.5	1055	731	COM ₇₀	-8527.5	1055
630	SEGB ₈₁	-3982.5	1055	681	SEGB ₉₈	-6277.5	1055	732	COM ₇₁	-8572.5	1055
631	SEGC ₈₁	-4027.5	1055	682	SEGC ₉₈	-6322.5	1055	733	COM ₇₂	-8617.5	1055
632	SEGA ₈₂	-4072.5	1055	683	SEGA ₉₉	-6367.5	1055	734	COM ₇₃	-8662.5	1055
633	SEGB ₈₂	-4117.5	1055	684	SEGB ₉₉	-6412.5	1055	735	COM ₇₄	-8707.5	1055
634	SEGC ₈₂	-4162.5	1055	685	SEGC ₉₉	-6457.5	1055	736	COM ₇₅	-8752.5	1055
635	SEGA ₈₃	-4207.5	1055	686	SEGA ₁₀₀	-6502.5	1055	737	COM ₇₆	-8797.5	1055
636	SEGB ₈₃	-4252.5	1055	687	SEGB ₁₀₀	-6547.5	1055	738	COM ₇₇	-8842.5	1055
637	SEGC ₈₃	-4297.5	1055	688	SEGC ₁₀₀	-6592.5	1055	739	COM ₇₈	-8887.5	1055
638	SEGA ₈₄	-4342.5	1055	689	SEGA ₁₀₁	-6637.5	1055	740	COM ₇₉	-8932.5	1055
639	SEGB ₈₄	-4387.5	1055	690	SEGB ₁₀₁	-6682.5	1055	741	DMY ₁₀₉	-8977.5	1055
640	SEGC ₈₄	-4432.5	1055	691	SEGC ₁₀₁	-6727.5	1055	742	DMY ₁₁₀	-9022.5	1055
641	SEGA ₈₅	-4477.5	1055	692	SEGA ₁₀₂	-6772.5	1055	743	DMY ₁₁₁	-9067.5	1055
642	SEGB ₈₅	-4522.5	1055	693	SEGB ₁₀₂	-6817.5	1055	744	DMY ₁₁₂	-9430	-784
643	SEGC ₈₅	-4567.5	1055	694	SEGC ₁₀₂	-6862.5	1055	745	DMY ₁₁₃	-9430	-829
644	SEGA ₈₆	-4612.5	1055	695	SEGA ₁₀₃	-6907.5	1055	746	DMY ₁₁₃	-9430	-874
645	SEGB ₈₆	-4657.5	1055	696	SEGB ₁₀₃	-6952.5	1055	747	DMY ₁₁₃	-9430	-919
646	SEGC ₈₆	-4702.5	1055	697	SEGC ₁₀₃	-6997.5	1055	748	DMY ₁₁₄	-9430	-964
647	SEGA ₈₇	-4747.5	1055	698	DMY ₁₀₆	-7042.5	1055	749			
648	SEGB ₈₇	-4792.5	1055	699	DMY ₁₀₇	-7087.5	1055	750			
649	SEGC ₈₇	-4837.5	1055	700	DMY ₁₀₈	-7132.5	1055	751			
650	SEGA ₈₈	-4882.5	1055	701	COM ₄₀	-7177.5	1055	752			
651	SEGB ₈₈	-4927.5	1055	702	COM ₄₁	-7222.5	1055	753			
652	SEGC ₈₈	-4972.5	1055	703	COM ₄₂	-7267.5	1055	754			
653	SEGA ₈₉	-5017.5	1055	704	COM ₄₃	-7312.5	1055	755			
654	SEGB ₈₉	-5062.5	1055	705	COM ₄₄	-7357.5	1055	756			
655	SEGC ₈₉	-5107.5	1055	706	COM ₄₅	-7402.5	1055	757			
656	SEGA ₉₀	-5152.5	1055	707	COM ₄₆	-7447.5	1055	758			
657	SEGB ₉₀	-5197.5	1055	708	COM ₄₇	-7492.5	1055	759			
658	SEGC ₉₀	-5242.5	1055	709	COM ₄₈	-7537.5	1055	760			
659	SEGA ₉₁	-5287.5	1055	710	COM ₄₉	-7582.5	1055	761			
660	SEGB ₉₁	-5332.5	1055	711	COM ₅₀	-7627.5	1055	762			
661	SEGC ₉₁	-5377.5	1055	712	COM ₅₁	-7672.5	1055	763			
662	SEGA ₉₂	-5422.5	1055	713	COM ₅₂	-7717.5	1055	764			
663	SEGB ₉₂	-5467.5	1055	714	COM ₅₃	-7762.5	1055	765			

■ BLOCK DIAGRAM



POWER SUPPLY CIRCUITS BLOCK DIAGRAM



■ TERMINAL DESCRIPTION 1

No.	Symbol	I/O	Function						
123~131	V _{DD}	Power	Power supply for logic circuits						
151~159	V _{SS}	Power	GND for logic circuits						
231~239	V _{SSH}	Power	GND for high voltage circuits						
4,5 33,34 67,68	V _{DDA}	Power	This terminal is internally connected to the V _{DD} level. <ul style="list-style-type: none"> This terminal is used to fix the selection terminals to the V_{DD} level. Note) Do not use this terminal for a main power supply.						
26,27 40,41 97,98	V _{SSA}	Power	This terminal is internally connected to the V _{SS} level. <ul style="list-style-type: none"> This terminal is used to fix the selection terminals to the V_{SS} level. Note) Do not use this terminal for a main GND.						
161~168 170~177 178~185 187~194 195~202	V _{LCD} V ₁ V ₂ V ₃ V ₄	Power/O	LCD driving voltages <ul style="list-style-type: none"> When the internal voltage booster is not used, the external LCD driving voltages (V₁ to V₄ and V_{LCD}) must be supplied on these terminals. And the external voltages must be maintained with the following relation. V_{SS}<V₄<V₃<V₂<V₁<V_{LCD} When the internal voltage booster is used, the LCD driving voltages (V₁ to V₄ and V_{LCD}) are enabled by the "Power control" instruction. The capacitors between the V_{SS} and these terminals are necessary. 						
263~267 270~274	C ₁₊ C ₁₋	O	Capacitor connection terminals for the voltage booster						
277~281 284~288	C ₂₊ C ₂₋	O	Capacitor connection terminals for the voltage booster						
291~295 298~302	C ₃₊ C ₃₋	O	Capacitor connection terminals for the voltage booster						
305~309 312~216	C ₄₊ C ₄₋	O	Capacitor connection terminals for the voltage booster						
319~323 326~330	C ₅₊ C ₅₋	O	Capacitor connection terminals for the voltage booster						
222~229	V _{BA}	O	Output of the reference-voltage generator						
213~220	V _{REF}	I	Input of the voltage regulator						
249~257	V _{EE}	Power	Input of the voltage booster <ul style="list-style-type: none"> This terminal is normally connected to the V_{DD} level. 						
240~248	V _{OUT}	Power/O	Output of the voltage booster Input for high voltage circuits in using external power supply						
204~211	V _{REG}	O	Output of the voltage regulator						
43,44	RESb	I	Reset Active "0"						
29,30	SEL68	I	MPU interface type select <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>SEL86</td> <td>H</td> <td>L</td> </tr> <tr> <td>Status</td> <td>68 series</td> <td>80 series</td> </tr> </table>	SEL86	H	L	Status	68 series	80 series
SEL86	H	L							
Status	68 series	80 series							
7,8 13,14 17,18 23,24	ID ₀ ID ₁ ID ₂ ID ₃	I	Chip Identification This terminal must be fixed to "1" or "0" The NJU6818 can read ID data, which is determined by fixing ID ₃ , ID ₂ , ID ₁ and ID ₀ pins to "1" or "0".						

■ TERMINAL DESCRIPTION 2

No.	Symbol	I/O	Function						
74,75	D ₀ /SCL	I/O	Parallel interface: D ₇ to D ₀ : 8-bit bi-directional bus • In the parallel interface mode (P/S="1"), these terminals connect to 8-bit bi-directional MPU bus.						
76,77	D ₁ /SDA	I/O							
82,83	D ₃ /SMODE	I/O	Serial interface: SDA : Serial data SCL : Serial clock SMODE : 3-/4-line serial interface mode selection SPOL : RS polarity selection (in the 3-line serial interface mode)						
86,87	D ₄ /SPOL	I/O							
80,81 88,89 92,93 94,95	D ₂ D ₅ D ₆ D ₇	I/O	• In the 3-/4-line serial interface mode (P/S="0"), the D ₀ terminal is assigned to the SCL, and the D ₁ terminal to the SDA. • In the 3-line serial interface mode, the D ₄ terminal is assigned to the SPOL. • Serial data on the SDA is fetched at the rising edge of the SCL signal in the order of the D ₇ , D ₆ ...D ₀ , and the fetched data is converted into 8-bit parallel data at the falling edge of the 8th SCL signal. • The SCL signal must be set to "0" after data transmissions or during non-access.						
100,101 102,103 106,107 108,109 112,113 114,115 118,119 120,121	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	8-bit bi-directional bus • In the 16-bit data bus mode, these terminals are assigned to the upper 8-bit data bus. • In the serial interface mode or the 8-bit data bus mode of the parallel interface, these terminals must be fixed to "1" or "0".						
49,50	CSb	I	Chip select Active "0"						
53,54	RS	I	Register select • This signal distinguishes transferred data as an instruction or display data as follows.						
			<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">RS</td> <td style="text-align: center;">H</td> <td style="text-align: center;">L</td> </tr> <tr> <td style="text-align: center;">Distinct.</td> <td style="text-align: center;">Instruction</td> <td style="text-align: center;">Display data</td> </tr> </table>	RS	H	L	Distinct.	Instruction	Display data
RS	H	L							
Distinct.	Instruction	Display data							
63,64	RDb (E)	I	80 series MPU interface (P/S="1", SEL68="0") RDb signal. Active "0". 68 series MPU interface (P/S="1", SEL68="1") Enable signal. Active "1".						
59,60	WRb (R/W)	I	80 series MPU interface (P/S="1", SEL68="0") WRb signal. Active "0". 68 series MPU interface (P/S="1", SEL68="1") R/W signal.						
			<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">R/W</td> <td style="text-align: center;">H</td> <td style="text-align: center;">L</td> </tr> <tr> <td style="text-align: center;">Status</td> <td style="text-align: center;">Read</td> <td style="text-align: center;">Write</td> </tr> </table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

■ TERMINAL DESCRIPTION 3

No.	Symbol	I/O	Function																		
37,38	P/S	I	Parallel / serial interface mode selection <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>P/S</th> <th>Chip Select</th> <th>Data/ Instruction</th> <th>Data</th> <th>Read/ Write</th> <th>Serial clock</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>CSb</td> <td>RS</td> <td>D₀ ~ D₇</td> <td>RDb, WRb</td> <td>-</td> </tr> <tr> <td>L</td> <td>CSb</td> <td>RS</td> <td>SDA (D1)</td> <td>Write only</td> <td>SCL (D0)</td> </tr> </tbody> </table> <ul style="list-style-type: none"> Since the D₁₅ to D₅ and D₂ terminals are in high impedance in the serial interface mode (P/S="0"), they must be fixed to "1" or "0". The RDb and WRb terminals also must be "1" or "0". 	P/S	Chip Select	Data/ Instruction	Data	Read/ Write	Serial clock	H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-	L	CSb	RS	SDA (D1)	Write only	SCL (D0)
P/S	Chip Select	Data/ Instruction	Data	Read/ Write	Serial clock																
H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-																
L	CSb	RS	SDA (D1)	Write only	SCL (D0)																
133,134	CL	O	This terminal must be opened.																		
135,136	FLM	O	This terminal must be opened.																		
139,140	FR	O	This terminal must be opened.																		
141,142	CLK	O	This terminal must be opened.																		
145,146 149,150	OSC ₁ OSC ₂	I O	OSC <ul style="list-style-type: none"> When the internal oscillator clock is used, the OSC₁ terminal must be fixed to "1" or "0", and the OSC₂ terminal must be opened. When the oscillation frequency from the internal oscillator is adjusted by an external resistor between OSC₁ terminal and OSC₂. When an external oscillator is used, external clock is input to the OSC₁ terminal, or an external resistor is connected between the OSC₁ and OSC₂ terminals. 																		
386~697	SEGA ₀ ~ SEGA ₁₀₃ , SEGB ₀ ~ SEGB ₁₀₃ , SEGC ₀ ~ SEGC ₁₀₃	O	Segment output <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>REV Mode</th> <th>Turn-off</th> <th>Turn-on</th> </tr> </thead> <tbody> <tr> <td>Normal</td> <td>0</td> <td>1</td> </tr> <tr> <td>Reverse</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <ul style="list-style-type: none"> These terminals output LCD driving waveforms in accordance with the combination of the FR signal and display data. <p><u>In the B/W mode</u></p> <div style="display: flex; align-items: flex-start;"> <div style="margin-right: 20px;"> <p>FR signal</p> <p>Display data</p> <p>Normal display mode</p> <p>Reverse display mode</p> </div> </div>	REV Mode	Turn-off	Turn-on	Normal	0	1	Reverse	1	0									
REV Mode	Turn-off	Turn-on																			
Normal	0	1																			
Reverse	1	0																			
343~382 701~740	COM ₀ ~ COM ₇₉	O	Common output <ul style="list-style-type: none"> These terminals output LCD driving waveforms in accordance with the combination of the FR signal and scanning data. <table border="1" style="margin: 10px auto; border-collapse: collapse; text-align: center;"> <thead> <tr> <th>Data</th> <th>FR</th> <th>Output level</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>H</td> <td>V_{SS}</td> </tr> <tr> <td>L</td> <td>H</td> <td>V₁</td> </tr> <tr> <td>H</td> <td>L</td> <td>V_{LCD}</td> </tr> <tr> <td>L</td> <td>L</td> <td>V₄</td> </tr> </tbody> </table>	Data	FR	Output level	H	H	V _{SS}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄			
Data	FR	Output level																			
H	H	V _{SS}																			
L	H	V ₁																			
H	L	V _{LCD}																			
L	L	V ₄																			

(Terminal No. 1~3,6, 9~12, 15, 16, 19~22, 25, 28, 31, 32, 35, 36, 39, 42, 45~48, 51, 52, 55~58, 61, 62, 65, 66, 69~73, 78, 79, 84, 85, 90, 91, 96, 99, 104, 105, 110, 111, 116, 117, 122, 132, 137, 138, 143, 144, 147, 148, 160, 169, 186, 203, 212, 221, 230, 258~262, 268, 269, 275, 276, 282, 283, 289, 290, 296, 297, 303, 304, 310, 311, 317, 318, 324, 325, 331~342, 383~385, 698~700, 741~748 are dummy.)

■ Functional Description

(1) MPU Interface

(1-1) Selection of parallel / serial interface mode

The P/S terminal is used to select the parallel or serial interface mode, as shown in the following table. In the serial interface mode, it is not possible to read out display data from the DDRAM or status data from the internal registers.

Table 1

P/S	P/S mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68	/	/	D7-D0 (D15-D0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

Note 1) “-” : Fix to “1” or “0”.

(1-2) Selection of MPU interface type

In the parallel interface mode, the SEL68 terminal is used to select 68- or 80-series MPU interface type, as shown in the following table.

Table 2

SEL68	MPU type	CSb	RS	RDb	WRb	Data
H	68 series MPU	CSb	RS	E	R/W	D7-D0 (D15-D0)
L	80 series MPU	CSb	RS	RDb	WRb	D7-D0 (D15-D0)

(1-3) Data distinction

In the parallel interface mode, the combination of the RS, RDb and WRb (R/W) signals distinguishes transferred data between the LSI and MPU as instruction or display data, as shown in the following table.

Table 3

RS	68 series	80 series		Function
	R/W	RDb	WRb	
H	H	L	H	Read out instruction data
H	L	H	L	Write instruction data
L	H	L	H	Read out display data
L	L	H	L	Write display data

(1-4) Selection of serial interface mode

In the serial interface mode, the SMODE terminal is used to select the 3- or 4-line serial interface mode, as shown in the following table.

Table 4

SMODE	Serial interface mode
H	3-line
L	4-line

(1-5) 4-line serial interface mode

In the 4-line serial interface mode, when the chip select is active (CSb="0"), the SDA and the SCL are enabled. When the chip select is not active (CSb="1"), the SDA and the SCL are disabled, and the internal shift register and the counter are being initialized. 8-bit serial data on the SDA is fetched at the rising edge of the SCL signal (serial clock) in order of the D₇, D₆...D₀, and the fetched data is converted into 8-bit parallel data at the rising edge of the 8th SCL signal.

In the 4-line serial interface mode, transferred data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS signal.

Table 5

RS	Data distinction
H	Instruction data
L	Display data

Since the serial interface operation is sensitive to external noises, the SCL should be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of 8-bit data transmissions. The following figure illustrates the interface timing of the 4-line serial interface operation.

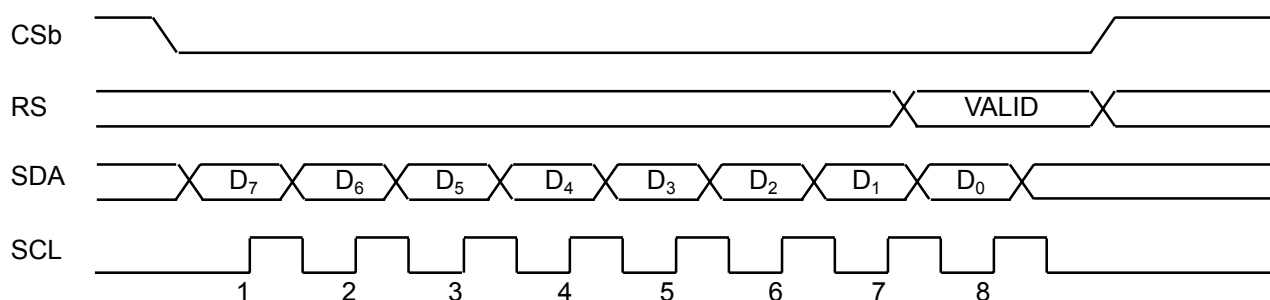


Fig 1 4-line serial interface timing

(1-6) 3-line serial interface mode

In the 3-line serial interface mode, when the chip select is active (CSb="0"), the SDA and the SCL are enabled. When the chip select is not active (CSb="1"), the SDA and the SCL are disabled, and the internal shift register and counter are being initialized. 9-bit serial data on the SDA is fetched at the rising edge of the SCL signal in order of the RS, D₇, D₆...D₀, and the fetched data is converted into 9-bit parallel data at the rising edge of the 9th SCL signal.

In the 3-line serial interface mode, data on the SDA is distinguished as display data or instruction data in accordance with the condition of the RS bit of the SDA data and the status of the SPOL, as follows.

Table 6

SPOL=L		SPOL=H	
RS	Data distinction	RS	Data distinction
L	Display data	L	Instruction data
H	Instruction data	H	Display data

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Since the serial interface operation is sensitive to external noises, the SCL must be set to "0" after data transmissions or during non-access. To release a mal-function caused by the external noises, the chip-selected status should be released (CSb="1") after each of 9-bit data transmissions. The following figure illustrates the interface timing of the 3-line serial interface operation.

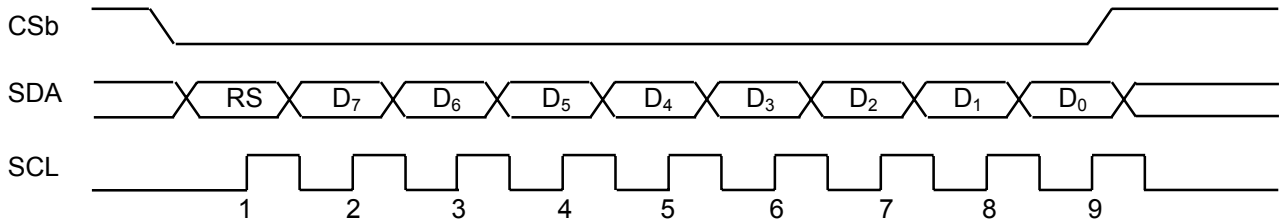


Fig 2 3-line serial interface timing

(2) Access to the DDRAM

When the CS_b signal is "0", transferred data from MPU is written into the DDRAM or the instruction register in accordance with the condition of the RS signal.

When the RS signal is "1", the transferred data is distinguished as display data. After the "column address" and "row address" instructions are executed, display data can be written into the DDRAM by the "Display data write" instruction. The display data is written at the rising edge of the WR_b signal in the 80 series MPU mode, or at the falling edge of the E signal in the 68 series MPU mode.

Table 6

RS	Data distinction
L	Display RAM Data
H	Internal Command Register

In the sequence of the "Display data read" operation, transferred data from MPU is temporarily held in the internal bus-holder, then transferred to the internal data-bus. When the "Display data read" operation is executed just after the "column address" and "row address" instructions or "Display data write" instruction, unexpected data on the bus-holder is read out at the 1st execution, then the data of designated DDRAM address is read out from the 2nd execution. For this reason, a dummy read cycle must be executed to avoid the unexpected 1st data read.

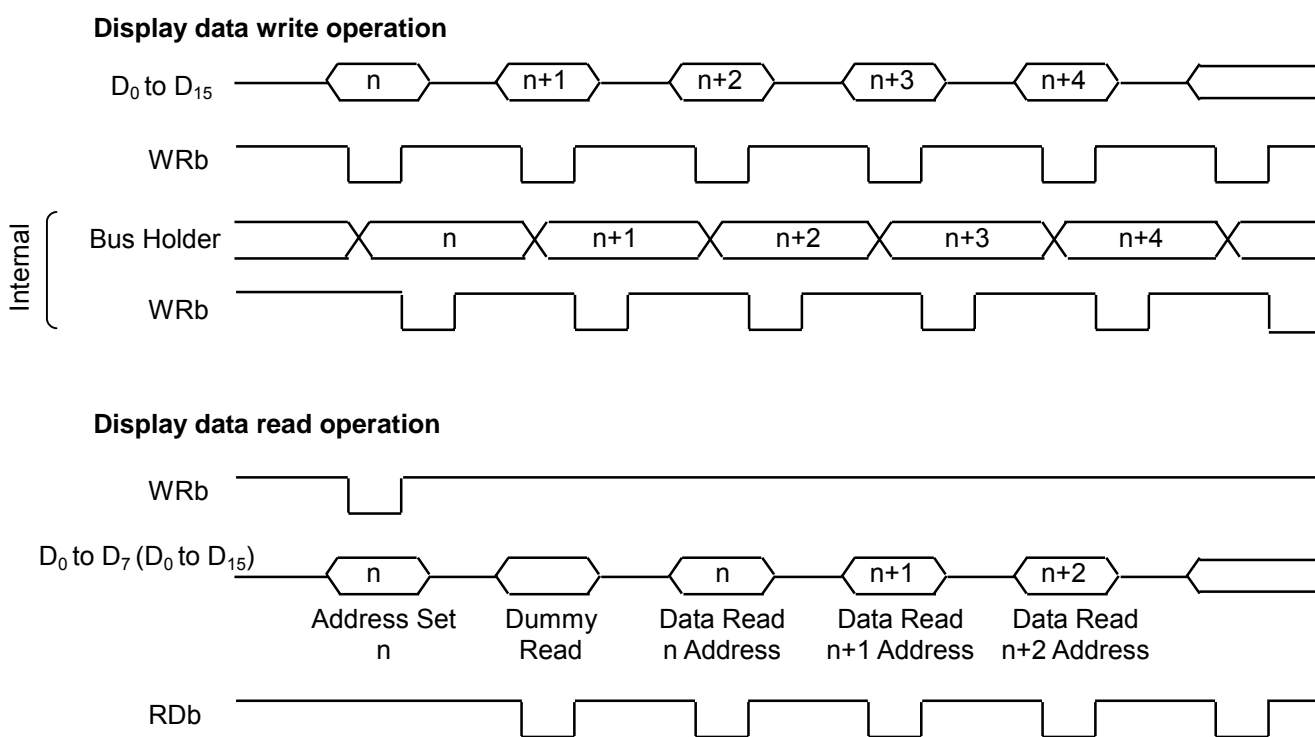


Fig 3

Note) In the 16-bit data bus mode, instruction data must be 16-bit as well as the display data.

(3) Access to the instruction register

Each instruction registers is assigned to each address between 0_H and F_H , and the content of the instruction register can be read out by the combination of the "Instruction register address" and "Instruction register read".

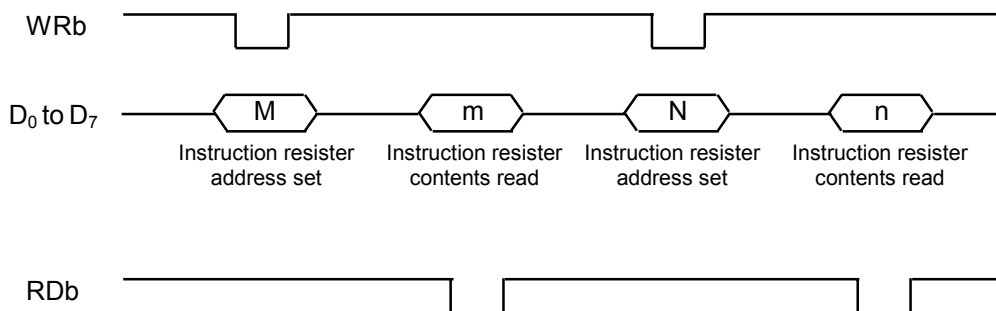


Fig 4

(4) 8-/16-bit data bus length for display data (In the parallel interface mode)

The 8- or 16-bit data bus length for display data is determined by the "WLS" of the "Data bus length" instruction.

In the 16-bit data bus mode, instruction data must be 16-bit (D_{15} to D_0) as well as display data. However, for the access to the instruction register, the only lower 8-bit data (D_7 to D_0) of 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D_{15} to D_0) is valid.

Table 8

WLS	Data bus length mode
L	8-bit
H	16-bit

(5) Initial display line register

The initial display line register specifies the line address, corresponding to the initial COM line, by the "Initial display line" instruction. The initial COM line signifies the common driver, starting scanning the display data in the DDRAM, and specified by the "Initial COM line" instruction.

The line address, established in the initial display line register, is preset into the line counter whenever the FLM signal becomes "1". At the rising edge of the CL signal, the line counter is counted-up and addressed 312-bit display data, corresponding to the counted-up line address, is latched into the data latch circuit. At the falling edge of the CL signal, the latched data outputs to the segment drivers.

(6) DDRAM Mapping

The DDRAM is capable of 1,248-bit (12-bit x 104-segment) for the column address and 80-bit for the row address.

In the gradation mode, each pixel for RGB corresponds to successive 3-segment drivers, and each segment driver has 16-gradation. Therefore, the LSI can drive up to 104x80 pixels in 4096-color display (16-gradation x 16-gradation x 16-gradation).

In the B&W mode, only MSB data from each 4-bit display data group in the DDRAM is used. Therefore, 312x80 pixels in the B&W and 104x80 pixels in the 8-gradation are available.

The range of the column address varies depending on data bus length. The range between 00_H and CF_H is used in the 8-bit data bus length, and the range between 00_H and 67_H is in the 16-bit data bus length.

- In the 8-bit data bus length mode

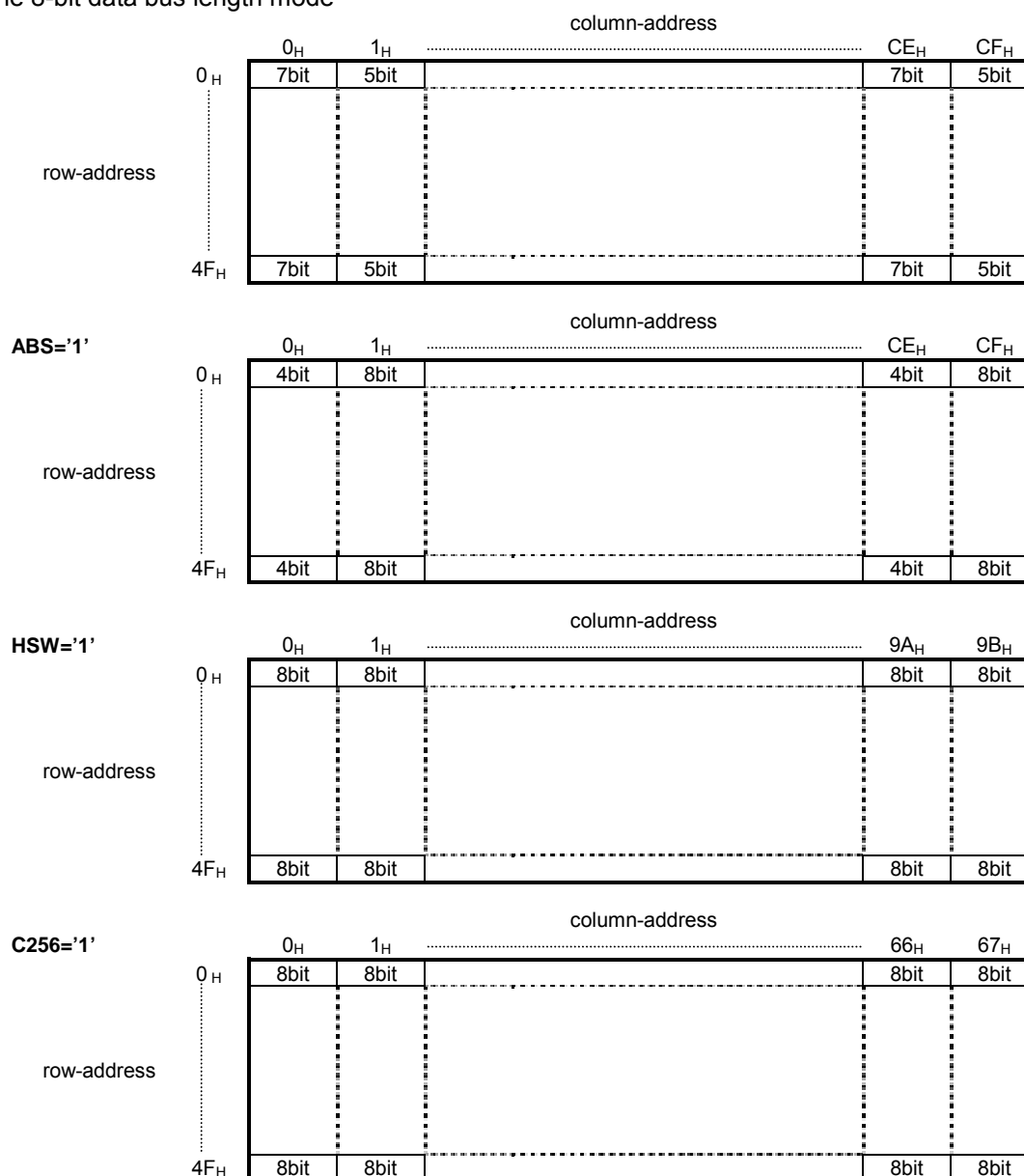


Fig 5

- In the 16-bit data bus length mode

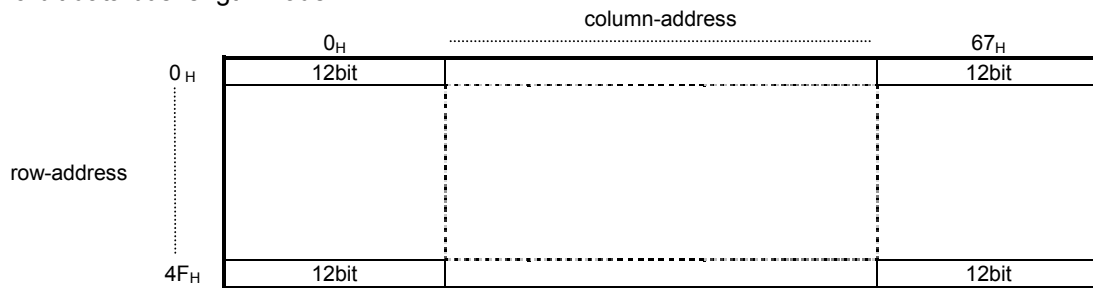


Fig 6

The increments for the column address and row address are set to the auto-increment mode by programming the “AXI” and “AYI” registers of the “Increment control” instruction. In this mode, the contents of the column address and row address counters automatically increment whenever the DDRAM is accessed.

The column address and row address counters, independent of the line counter. They are used to designate the column and row addresses for the display data transferred from MPU. On the other hand, the line counter is used to generate the line address, and output display data to the segment drivers, being synchronized with the display control timing of the FLM and CL signals.

(7) Window addressing mode

In addition to the above usual DDRAM addressing, it is possible to access some part of DDRAM in using the window addressing mode, in which the start and end points are designated. The start point is determined by the "column address" and "row address" instructions, and the end point is determined by the "Window end column address" and "Window end row address" instructions. The setting example of the window addressing is listed, as follows.

1. Set WIN=1, AXI=1, and AYI=1 by the "Increment control" instruction
2. Set the start point by the "column address" and "row address" instructions
3. Set the end point by the "Window end column address" and "Window end row address" instructions
4. Enable to access to the DDRAM in the window addressing mode

In the window addressing mode (WIN=1, AXI=1, AYI=1), the read-modify-write operation is available by setting "0" to the "AIM" register of the "Increment control" instruction.

And in the window addressing mode, the following relation for the start and end points must be maintained to avoid a malfunction.

AX (column address of start point) < EX (column address of the end point) < Maximum of column address

AY (row address of start point) < EY (row address of the end point) < Maximum of row address

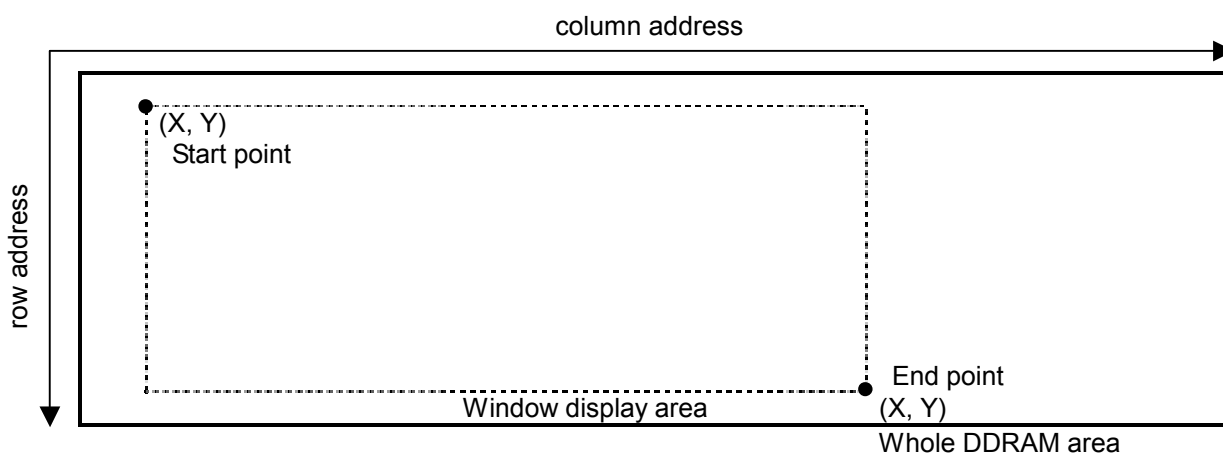


Fig 7

(8) Reverse display ON/OFF

The "Reverse display ON/OFF" function is used to reverse the display data without changing the contents of the DDRAM.

Table 9

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(9) Segment direction

The "Segment direction" function is used to reverse the assignments for the segment drivers and the column addresses, and it is possible to reduce restrictions for the placement of the LSI on LCD modules.

(10) The relation among the DDRAM column address, display data, and segment drivers

In the color mode and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	0	0	0	X=00 _H												↔	X=67 _H											
*	0	1	1	X=67 _H												↔	X=00 _H											
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	0	0	1	X=00 _H												↔	X=67 _H											
*	0	1	0	X=67 _H												↔	X=00 _H											
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	1	0	0	X=00 _H												↔	X=67 _H											
*	1	1	1	X=67 _H												↔	X=00 _H											
				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
*	1	0	1	X=00 _H												↔	X=67 _H											
*	1	1	0	X=67 _H												↔	X=00 _H											
				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

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In the color mode and 8-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																														
0	0	0	0	X=00 _H					X=01 _H					↔					X=CE _H					X=CF _H										
0	0	1	1	X=CE _H					X=CF _H					↔					X=00 _H					X=01 _H										
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
				palette A					palette B					palette C					↔	palette A					palette B					palette C				
				SEGA ₀					SEGB ₀					SEGC ₀					↔	SEGA ₁₀₃					SEGB ₁₀₃					SEGC ₁₀₃				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																														
0	0	0	1	X=00 _H					X=01 _H					↔					X=CE _H					X=CF _H										
0	0	1	0	X=CE _H					X=CF _H					↔					X=00 _H					X=01 _H										
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
				palette A					palette B					palette C					↔	palette A					palette B					palette C				
				SEGC ₀					SEGB ₀					SEGA ₀					↔	SEGC ₁₀₃					SEGB ₁₀₃					SEGA ₁₀₃				

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
0	1	0	0	X=00 _H				X=01 _H								↔				X=CE _H				X=CF _H				
0	1	1	1	X=CE _H				X=CF _H								↔				X=00 _H				X=01 _H				
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																								
0	1	0	1	X=00 _H				X=01 _H								↔				X=CE _H				X=CF _H				
0	1	1	0	X=CE _H				X=CF _H								↔				X=00 _H				X=01 _H				
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				palette A				palette B				palette C				↔	palette A				palette B				palette C			
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAF	Column-address / bit / segment assign		
1	*	1	1	X=9AH	X=9BH	X=99H
SEGA	0	Palette A	D3	D2	D1	D0
SEGB	0	Palette B	D7	D6	D5	D4
SEGC	0	Palette C	D3	D2	D1	D0
SEGA	1	Palette A	D7	D6	D5	D4
SEGB	1	Palette B	D3	D2	D1	D0
SEGC	1	Palette C	D7	D6	D5	D4
SEGA	102	Palette A	D3	D2	D1	D0
SEGB	102	Palette B	D7	D6	D5	D4
SEGC	102	Palette C	D3	D2	D1	D0
SEGA	103	Palette A	D7	D6	D5	D4
SEGB	103	Palette B	D3	D2	D1	D0
SEGC	103	Palette C	D7	D6	D5	D4

HSW	ABS	REF	SWAF	Column-address / bit / segment assign		
1	*	1	0	X=9AH	X=9BH	X=99H
SEGC	0	Palette A	D3	D2	D1	D0
SEGB	0	Palette B	D7	D6	D5	D4
SEGA	0	Palette C	D3	D2	D1	D0
SEGC	1	Palette A	D7	D6	D5	D4
SEGB	1	Palette B	D3	D2	D1	D0
SEGA	1	Palette C	D7	D6	D5	D4
SEGC	102	Palette A	D3	D2	D1	D0
SEGB	102	Palette B	D7	D6	D5	D4
SEGA	102	Palette C	D3	D2	D1	D0
SEGC	103	Palette A	D7	D6	D5	D4
SEGB	103	Palette B	D3	D2	D1	D0
SEGA	103	Palette C	D7	D6	D5	D4

HSW	ABS	REF	SWAF	Column-address / bit / segment assign		
1	*	0	1	X=00H	X=01H	X=02H
SEGC	0	Palette A	D7	D6	D5	D4
SEGB	0	Palette B	D3	D2	D1	D0
SEGA	0	Palette C	D7	D6	D5	D4
SEGC	1	Palette A	D3	D2	D1	D0
SEGB	1	Palette B	D7	D6	D5	D4
SEGA	1	Palette C	D3	D2	D1	D0
SEGC	102	Palette A	D7	D6	D5	D4
SEGB	102	Palette B	D3	D2	D1	D0
SEGA	102	Palette C	D7	D6	D5	D4
SEGC	103	Palette A	D3	D2	D1	D0
SEGB	103	Palette B	D7	D6	D5	D4
SEGA	103	Palette C	D3	D2	D1	D0

HSW	ABS	REF	SWAF	Column-address / bit / segment assign		
1	*	0	0	X=00H	X=01H	X=02H
SEGA	0	Palette A	D7	D6	D5	D4
SEGB	0	Palette B	D3	D2	D1	D0
SEGC	0	Palette C	D7	D6	D5	D4
SEGA	1	Palette A	D3	D2	D1	D0
SEGB	1	Palette B	D7	D6	D5	D4
SEGC	1	Palette C	D3	D2	D1	D0
SEGA	102	Palette A	D7	D6	D5	D4
SEGB	102	Palette B	D3	D2	D1	D0
SEGC	102	Palette C	D7	D6	D5	D4
SEGA	103	Palette A	D3	D2	D1	D0
SEGB	103	Palette B	D7	D6	D5	D4
SEGC	103	Palette C	D3	D2	D1	D0

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In the color mode, 8-bit data bus mode, and C256 mode (C256=1)

HSW	ABS	REF	SWAP	Column address / bit / segment assign																		
*	*	0	0	X=00 _H							↔	X=67 _H										
*	*	1	1	X=67 _H							↔	X=00 _H										
				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				palette A			palette B			palette C			↔	palette A			palette B			palette C		
				SEGA ₀			SEGB ₀			SEGC ₀			↔	SEGA ₁₀₃			SEGB ₁₀₃			SEGC ₁₀₃		

HSW	ABS	REF	SWAP	Column address / bit / segment assign																		
*	*	0	1	X=00 _H							↔	X=67 _H										
*	*	1	0	X=67 _H							↔	X=00 _H										
				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				palette A			palette B			palette C			↔	palette A			palette B			palette C		
				SEGC ₀			SEGB ₀			SEGA ₀			↔	SEGC ₁₀₃			SEGB ₁₀₃			SEGA ₁₀₃		

In the B&W mode and 16-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	0	0	0	X=00 _H								↔	X=67 _H																							
*	0	1	1	X=67 _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃											

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	0	0	1	X=00 _H								↔	X=67 _H																							
*	0	1	0	X=67 _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃											

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	1	0	0	X=00 _H								↔	X=67 _H																							
*	1	1	1	X=67 _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃											

HSW	ABS	REF	SWAP	Column address / bit / segment assign																																
*	1	0	1	X=00 _H								↔	X=67 _H																							
*	1	1	0	X=67 _H								↔	X=00 _H																							
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃											

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In the B&W mode and 8-bit data bus mode

HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	0	0	0	X=00 _H				X=01 _H				↔	X=CE _H				X=CF _H												
0	0	1	1	X=CE _H				X=CF _H				↔	X=00 _H				X=01 _H												
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	
				SEGA ₀				SEGB ₀					SEGC ₀					SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	0	0	1	X=00 _H				X=01 _H				↔	X=CE _H				X=CF _H												
0	0	1	0	X=CE _H				X=CF _H				↔	X=00 _H				X=01 _H												
				D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	
				SEGC ₀				SEGB ₀					SEGA ₀					SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	1	0	0	X=00 _H				X=01 _H				↔	X=CE _H				X=CF _H												
0	1	1	1	X=CE _H				X=CF _H				↔	X=00 _H				X=01 _H												
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				SEGA ₀				SEGB ₀					SEGC ₀					SEGA ₁₀₃				SEGB ₁₀₃				SEGC ₁₀₃			

HSW	ABS	REF	SWAP	Column address / bit / segment assign																									
0	1	0	1	X=00 _H				X=01 _H				↔	X=CE _H				X=CF _H												
0	1	1	0	X=CE _H				X=CF _H				↔	X=00 _H				X=01 _H												
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
				SEGC ₀				SEGB ₀					SEGA ₀					SEGC ₁₀₃				SEGB ₁₀₃				SEGA ₁₀₃			

HSW	ABS	REF	SWAF	SWAF
1	*	0	0	0

Column-address / bit / segment assign	
SEGA 0	D7
	D6
	D5
	D4
SEGB 0	D3
	D2
	D1
	D0
SEGC 0	D7
	D6
	D5
	D4
SEGA 1	D3
	D2
	D1
	D0
SEGB 1	D7
	D6
	D5
	D4
SEGC 1	D3
	D2
	D1
	D0
SEGA 102	D7
	D6
	D5
	D4
SEGB 102	D3
	D2
	D1
	D0
SEGC 102	D7
	D6
	D5
	D4
SEGA 103	D3
	D2
	D1
	D0
SEGB 103	D7
	D6
	D5
	D4
SEGC 103	D3
	D2
	D1
	D0

HSW	ABS	REF	SWAF	SWAF
1	*	0	1	1

Column-address / bit / segment assign	
SEGC 0	D7
	D6
	D5
	D4
SEGB 0	D3
	D2
	D1
	D0
SEGA 0	D7
	D6
	D5
	D4
SEGC 1	D3
	D2
	D1
	D0
SEGB 1	D7
	D6
	D5
	D4
SEGA 1	D3
	D2
	D1
	D0
SEGC 102	D7
	D6
	D5
	D4
SEGB 102	D3
	D2
	D1
	D0
SEGA 102	D7
	D6
	D5
	D4
SEGC 103	D3
	D2
	D1
	D0
SEGB 103	D7
	D6
	D5
	D4
SEGA 103	D3
	D2
	D1
	D0

HSW	ABS	REF	SWAF	SWAF
1	*	1	0	0

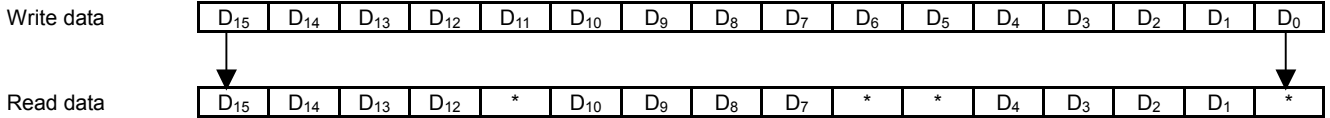
Column-address / bit / segment assign	
SEGC 0	D3
	D2
	D1
	D0
SEGB 0	D7
	D6
	D5
	D4
SEGA 0	D3
	D2
	D1
	D0
SEGC 1	D7
	D6
	D5
	D4
SEGB 1	D3
	D2
	D1
	D0
SEGA 1	D7
	D6
	D5
	D4
SEGC 102	D3
	D2
	D1
	D0
SEGB 102	D7
	D6
	D5
	D4
SEGA 102	D3
	D2
	D1
	D0
SEGC 103	D7
	D6
	D5
	D4
SEGB 103	D3
	D2
	D1
	D0
SEGA 103	D7
	D6
	D5
	D4

HSW	ABS	REF	SWAF	SWAF
1	*	1	1	1

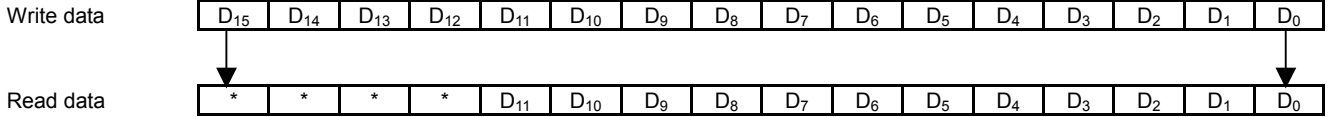
Column-address / bit / segment assign	
SEGA 0	D3
	D2
	D1
	D0
SEGB 0	D7
	D6
	D5
	D4
SEGC 0	D3
	D2
	D1
	D0
SEGA 1	D7
	D6
	D5
	D4
SEGB 1	D3
	D2
	D1
	D0
SEGC 1	D7
	D6
	D5
	D4
SEGA 102	D3
	D2
	D1
	D0
SEGB 102	D7
	D6
	D5
	D4
SEGC 102	D3
	D2
	D1
	D0
SEGA 103	D7
	D6
	D5
	D4
SEGB 103	D3
	D2
	D1
	D0
SEGC 103	D7
	D6
	D5
	D4

Bit assignments between write and read data (In the 16-bit data bus mode)

ABS=0

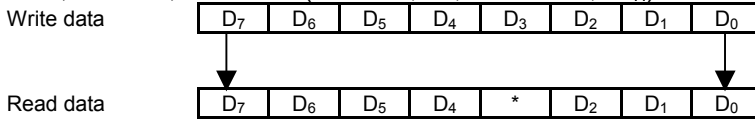


ABS=1

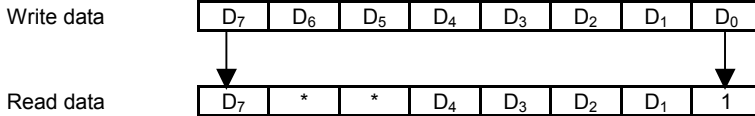


Examples of write and read data (In the 8 bit bus mode)

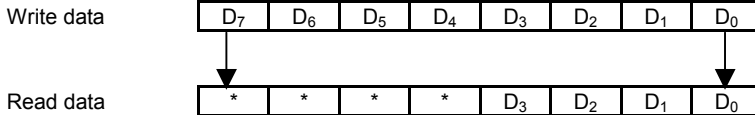
ABS=0, HSW=0, C256=0 (Address; 00, 02.....CC, CE_H)



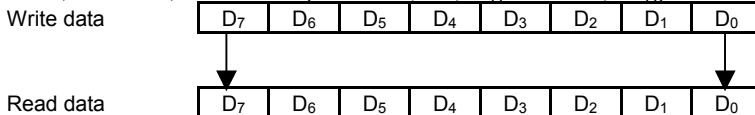
ABS=0, HSW=0, C256=0 (Address; 01, 03_H.....CD, CF_H)



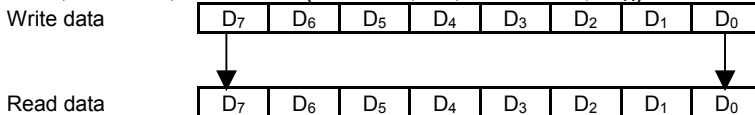
ABS=1, HSW=0, C256=0 (Address; 00, 02.....CC, CE_H)



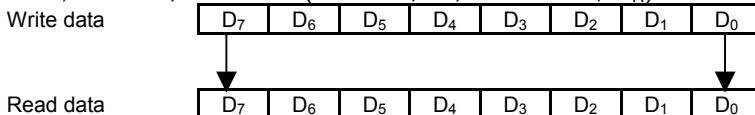
ABS=1, HSW=0, C256=0 (Address; 01, 03_H..... CD, CF_H)



ABS=0, HSW=1, C256=0 (Address; 00, 01.....9A, 9B_H)



ABS=0, HSW=0, C256=1 (Address; 00, 01..... 66, 67_H)



*: Invalid Data

(11) Gradation palette

In the gradation mode, either variable or fixed gradation mode is selected by programming the “PWM” register of the “Gradation control” instruction.

PWM=0:	Variable gradation mode (Select 16-gradation level out of 32-gradation level of the gradation palette)
PWM=1:	Fixed gradation mode (Fixed 8-gradation level)

In these modes, each of the gradation palettes of the Aj, Bj and Cj can select 16-gradation level out of 32-gradation level by setting 5-bit data to the “PA” registers in the “Gradation palette j” instructions (j=0 to Fh). For instance, the gradation palettes Aj correspond to the SEGAI, the Bj to the SEGBj, and the Cj to the SEGCi (j=0 to 15, i=0 to 103).

Correspondence between display data and gradation palettes

Table 10 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

(MSB) Display data (LSB)				Gradation palette	Default palette value
0	0	0	0	Palette 0	0 0 0 0
0	0	0	1	Palette 1	0 0 0 1
0	0	1	0	Palette 2	0 0 1 0
0	0	1	1	Palette 3	0 0 1 1
0	1	0	0	Palette 4	0 1 0 0
0	1	0	1	Palette 5	0 1 0 1
0	1	1	0	Palette 6	0 1 1 0
0	1	1	1	Palette 7	0 1 1 1
1	0	0	0	Palette 8	1 0 0 0
1	0	0	1	Palette 9	1 0 0 1
1	0	1	0	Palette 10	1 0 1 0
1	0	1	1	Palette 11	1 0 1 1
1	1	0	0	Palette 12	1 1 0 0
1	1	0	1	Palette 13	1 1 0 1
1	1	1	0	Palette 14	1 1 1 0
1	1	1	1	Palette 15	1 1 1 1

Gradation palette table (Variable gradation mode, PWM="0", MON="0")

Table 11 (Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0	0	Palette 0(default)	1 0 0 0	16/31	
0 0 0 1	1/31		1 0 0 1	17/31	Palette 8(default)
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

Gradation palette table (Fixed gradation mode, PWM="1", MON="0")

Table 12 8-gradation segment drivers

(MSB) Display data (LSB)				Gradation level
0	0	0	*	0/7
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

(MSB) Display data (LSB)				Gradation level
0	0	*	*	0/7
0	0	*	*	
0	1	*	*	3/7
0	1	*	*	
1	0	*	*	5/7
1	0	*	*	
1	1	*	*	7/7
1	1	*	*	

Correspondence between display data and gradation level (B&W mode, MON="1")

Table 13

(MSB) Display data (LSB)				Gradation level
0	*	*	*	0
1	*	*	*	1

*:Don't care

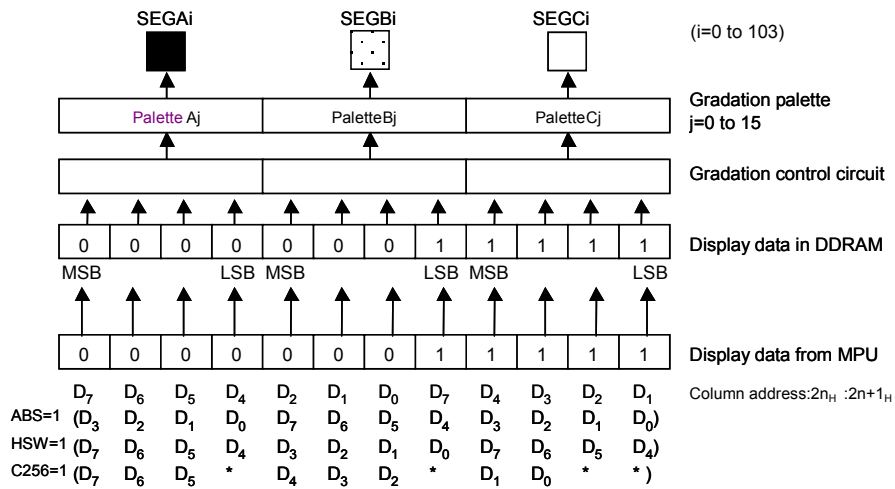
(12) Gradation control and display data

(12-1) Gradation mode

In the gradation mode, each pixel for RGB corresponds to successive 3 segment-drivers, and each segment driver provides 16-gradation PWM output by controlling 4-bit display data of the DDRAM. Accordingly, the LSI can drive up to 104x80 pixels in 4096-color (16-gradation x 16-gradation x 16-gradation = 4-bit x 4-bit x 4-bit).

In addition, the LSI can transfer the display data for the RGB by 16-bit at once or 8-bit two times. The data assignment between gradation palettes and segment drivers varies in accordance with setting for the "SWAP" and "REF" registers of the "Display control (2)" instruction.

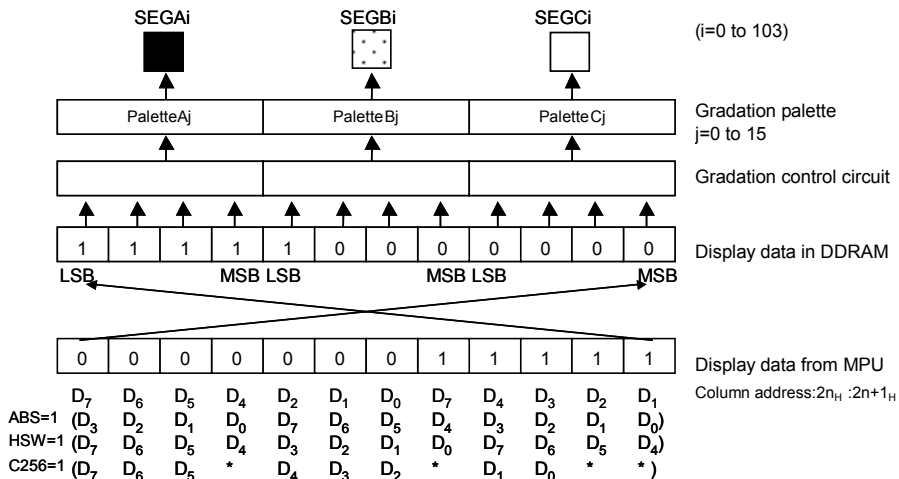
(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : $2n_H, 2n_H+1_H$ (REF="0")
 : $CE_H-2n_H, CF_H-(2n_H+1_H)$ (REF="1")

HSW=1; 00_H to 9B_H
 C256=1; 00_H to 67_H

(REF, SWAP)=(0, 1) or (1, 0)

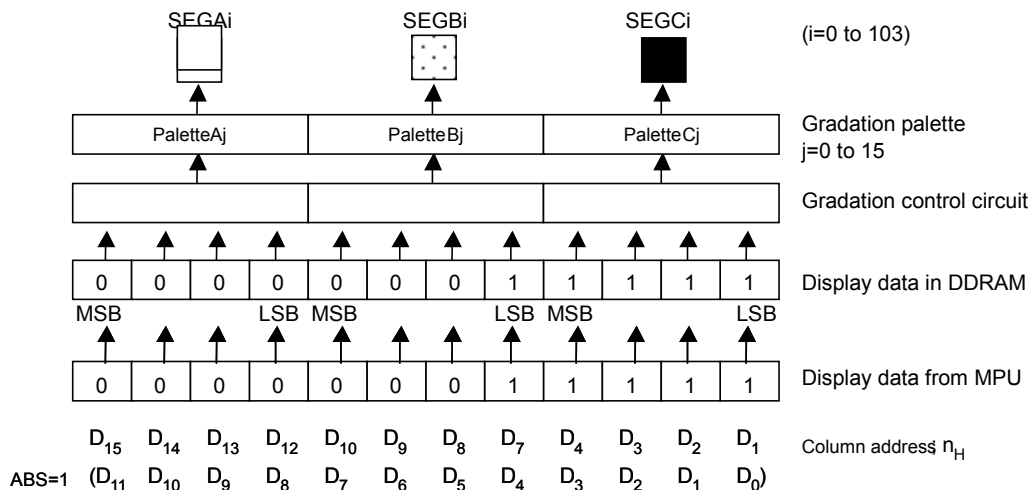


Note) DDRAM column address : $2n_H, 2n_H+1_H$ (REF="0")
 : $CE_H-2n_H, CF_H-(2n_H+1_H)$ (REF="1")

HSW=1; 00_H to 9B_H
 C256=1; 00_H to 67_H

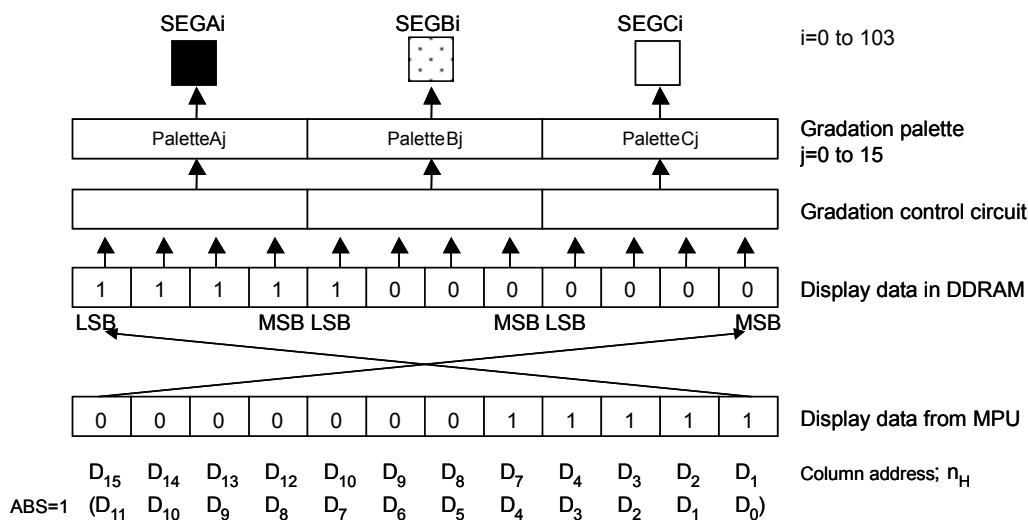
In the 16-bit data bus mode, the data assignments between the gradation palettes and the segment drivers vary in accordance with setting for the "SWAP" and "REF" bits of the "Display control (2)" instruction as well as the assignment in the 8-bit data bus mode.

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address :n_H (REF="0")
 :67_H - n_H (REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



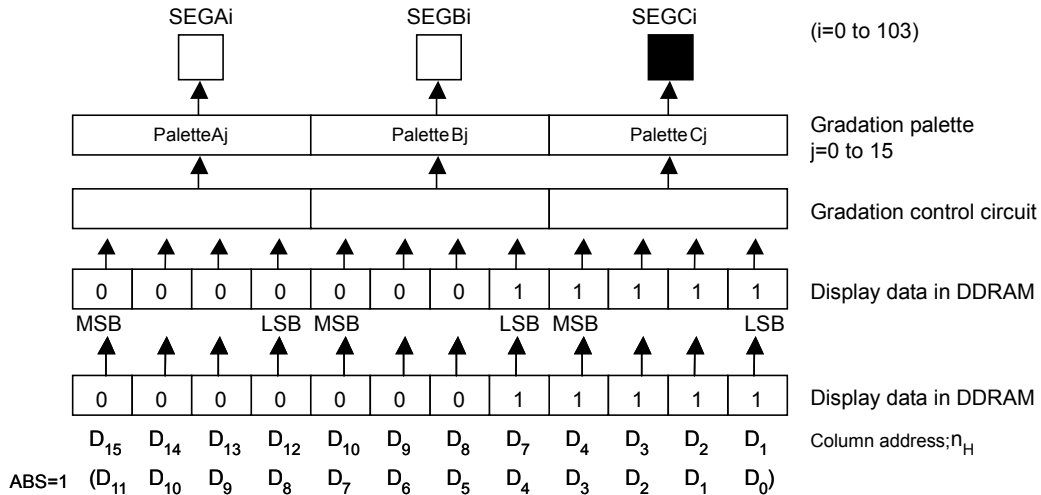
Note) DDRAM column address :n_H (REF="0")
 :67_H - n_H (REF="1")

(12-2) B&W mode (MON="1")

In the B&W mode, 3 bits of the MSB data are used in both of the 16-bit and 8-bit data bus modes.

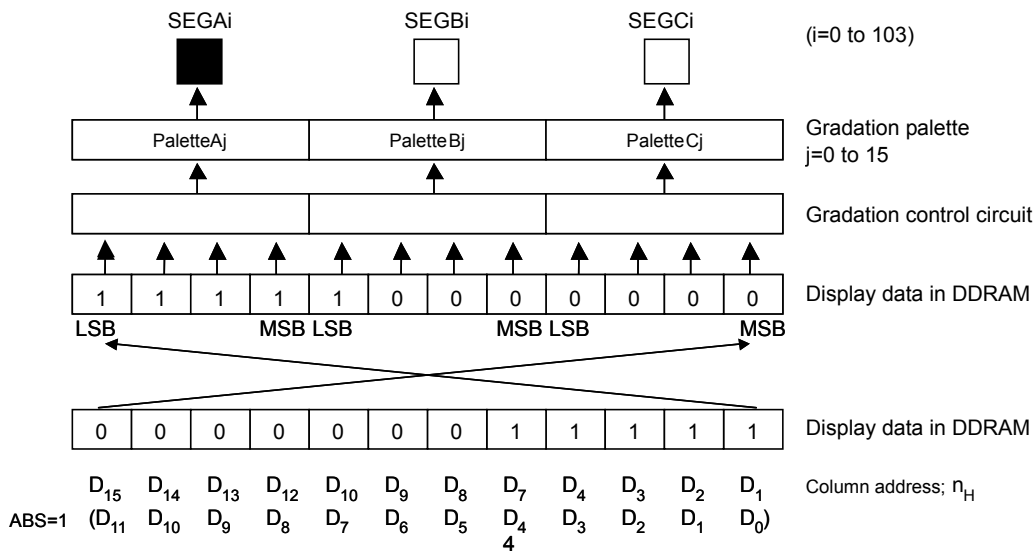
In the 16-bit data bus mode (Similarly 8-bit data bus access)

(REF, SWAP)=(0, 0) or (1, 1)



Note) DDRAM column address : n_H (REF="0")
 : 67_H-n_H (REF="1")

(REF, SWAP)=(0, 1) or (1, 0)



Note) DDRAM column address: n_H (REF="0")
 : 67_H-n_H (REF="1")

(13) Display timing generator

The display-timing generator creates the timing pulses such as the CL, the FLM, the FR and the CLK by dividing the oscillation frequency oscillate an external or internal resistor mode. The each of timing pulses is outputted through the each output terminals by "SON"=1.

(14) LCD line clock (CL)

The LCD line clock (CL) is used as a count-up signal for the line counter and a latch signal for the data latch circuit. At the rising edge of the CL signal, the line counter is counted-up and 312-bit display data, corresponding to this line address, is latched into the data latch circuit. And at the falling edge of the CL signal, this latched data output on the segment drivers. Read out timing of the display data, from DDRAM to the latch circuits, is completely independent of the access timing to MPU. For this reason, the MPU can access to the LSI regardless of an internal operation.

(15) LCD alternate signal (FR) and LCD synchronous signal (FLM)

The FR and FLM signals are created from the CL signal. The FR signal is used to alternate the crystal polarization on a LCD panel. It is programmed that the FR signal is toggle on every frame in the default setting or once every N lines in the N-line inversion mode. The FLM signal is used to indicate a start line of a new display frame. It presets an initial display line address of the line counter when the FLM signal becomes "1".

(16) Data latch circuit

The data latch circuit is used to temporarily store the display data that will output on the segment drivers. The display data in this circuit is updated in synchronization of the CL signal.

The "All pixels ON/OFF", "Display ON/OFF" and "Reverse display ON/OFF" instructions change the display data in this circuit but do not change the display data of the DDRAM.

(17) Common and segment drivers

The LSI includes 312-segment drivers and 80-common drivers. The common drivers generate LCD driving waveforms composed of the V_{LCD} , V_1 , V_4 and V_{SS} in accordance with the FR signal and scanning data. The segment drivers generate waveforms composed of the V_{LCD} , V_2 , V_3 and V_{SS} in accordance with the FR signal and display data.

(18) Chip Identification (ID)

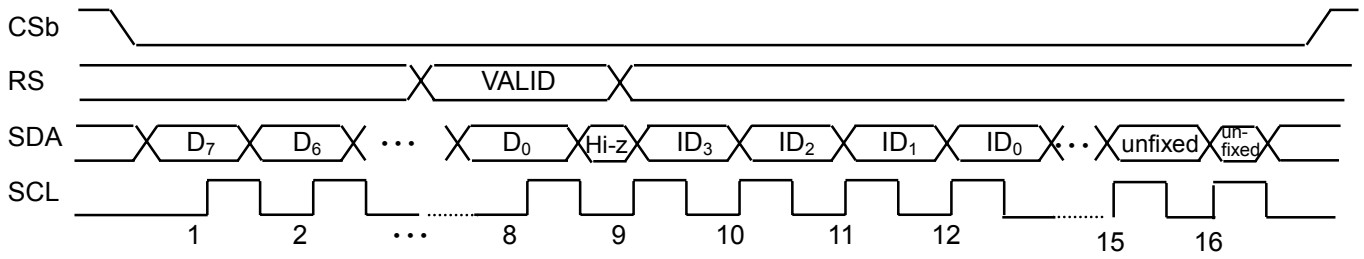
The NJU6818 can read ID data, which is determined by fixing ID3, ID2, ID1 and ID0 pins to "1" (V_{DD}) or "0" (V_{SS}). When the parallel interface is used, the ID data can be read out through the D₇, D₆, D₅ and D₄ pins as upper 4-bit data of the internal register. When the serial interface is used, the ID data can be read out as follows.

In the 4-line serial interface mode, "ID read-out instruction" must be set by IDR=1 during the SDA and SCL pins are enabled by CS=1. First, the serial data on the SDA must be input at the rising edge of the SCL clock, next the SDA must be in high-impedance (Hi-Z) at the falling edge of the 8th SCL clock. From the rising edge of the 9th SCL clock, the ID data such as ID3, ID2, ID1 and ID0 is read out. The serial data after the ID0 is undefined, and this reading mode is returned to the writing mode at the rising edge of the 16th SCL clock. The serial data on the SDA at the 8th and 16th SCL clocks applies specified serial interface timing.

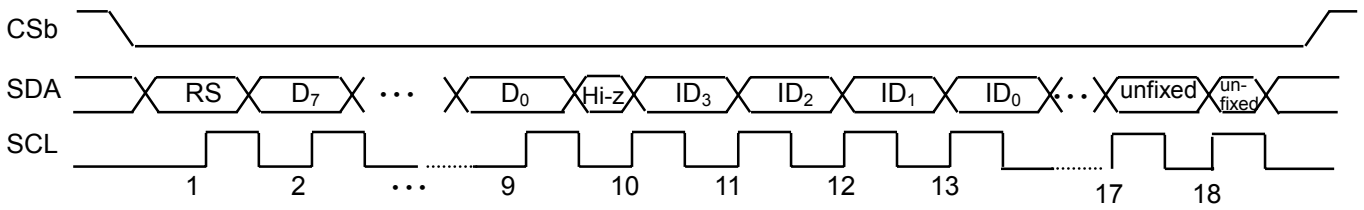
In the 3-line serial interface mode, the SDA must be in high-impedance (Hi-Z) at the falling edge of the 9th SCL clock. From the rising edge of the 10th SCL clock, the ID data is read out as well as operation in the 4-line serial interface mode. The serial data after ID0 is undefined, and this reading mode is returned to the writing mode at the rising edge of the 18th SCL clock. The serial data on the SDA at the 9th and 18th SCL clocks applies specified serial interface timing.

Note) Refer to the "Serial Interface Timing" for the detail

ID Read in the 4-Line serial interface mode



ID Read in the 4-Line serial interface mode



● LCD Driving waveforms (In the B&W mode, Reverse display OFF, 1/81 duty)

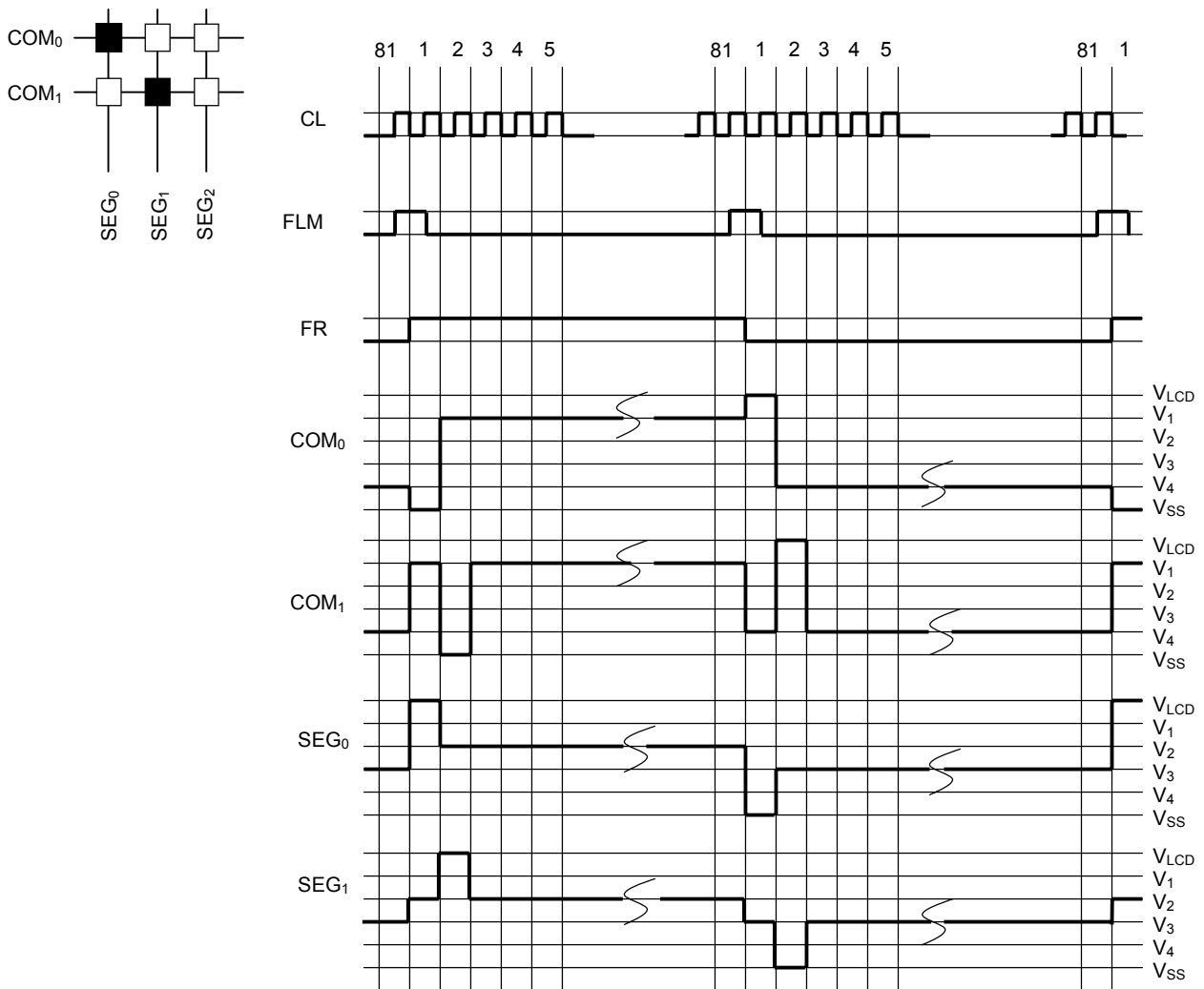


Fig 8

(19) Oscillator

The oscillator generates internal clocks for the display timing and the voltage booster. Since the LSI has internal capacitor (C) and resistor (R) for the oscillation, external capacitor and resistor are not usually required. However, in case that an external resistor is used, the resistor is connected between the OSC₁ and OSC₂ terminals. The external resistor becomes enabled by setting "1" to the "CKS" register of "Data bus length" instruction. When the internal oscillator is not used, the external clocks with 50% duty cycle ratio must be input to the OSC₁ terminal.

In addition, the feed back resistor for the oscillation is varied by programming the "Rf" register of the "Frequency control" instruction, so that it is possible to optimize the frame frequency for a LCD panel. Setting examples of the MON (B&W /Gradation) and the PWM (Variable gradation /Fixed gradation) are described, as follows.

(19-1) Internal oscillation mode (CKS=0)

Symbol	MON	PWM	Display mode
FR1	0	0	Variable gradation mode
FR2	0	1	Fixed gradation mode
FR3	1	*	B&W mode

*: Don't care

(19-2) External resistor oscillation mode (CKS=1)

The internal clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(19-3) External clock input mode (CKS=1)

The external clocks must be adjusted to the same frequency as the one in using the internal oscillation mode, and the "MON" and "PWM" registers must be set as well.

(20) Power supply circuits

The internal power supply circuits are composed of the voltage booster, the electrical variable resistor (EVR), the voltage regulator, reference voltage generator and the voltage followers.

The condition of the power supply circuits is arranged by programming the "DCON" and "AMPON" registers on the "Power control" instruction. For this arrangement, some parts of the internal power supply circuits are activated in using an external power supply, as shown in the following table.

Table 15

DCON	AMPON	Voltage booster	Voltage followers Voltage regulator EVR	External voltage	Note
0	0	Disable	Disable	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3
0	1	Disable	Enable	V _{OUT}	2, 3
1	1	Enable	Enable	-	-

Note1) The internal power circuits are not used. The external V_{OUT} is required and the C₁⁺, C₁⁻, C₂⁺, C₂⁻, C₃⁺, C₃⁻, C₄⁺, C₄⁻, C₅⁺, C₅⁻, V_{REF}, V_{REG} and V_{EE} terminals must be open.

Note2) The internal power circuits except the voltage booster are used. The external V_{OUT} is required and the C₁⁺, C₁⁻, C₂⁺, C₂⁻, C₃⁺, C₃⁻, C₄⁺, C₄⁻, C₅⁺, C₅⁻ and V_{EE} terminals must be open. The reference voltage is required to V_{REF} terminal.

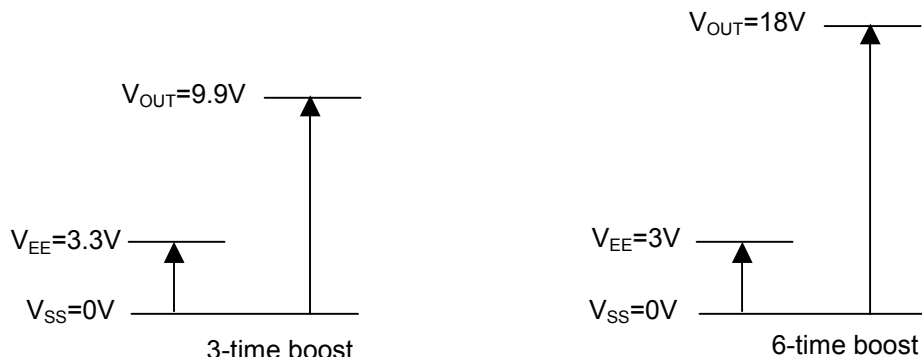
Note3) The relation among the voltages should be maintained as follows.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SS}$$

(21) Voltage booster

The voltage booster generates maximum 6x voltage of the V_{EE} level. It is programmed so that the boost level is selected out of 1x, 2x, 3x, 4x, 5x and 6x by the "Boost level select" instruction. The boosted voltage V_{OUT} must not exceed beyond the value of 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

Boosted voltages



Capacitor connections for the voltage Booster

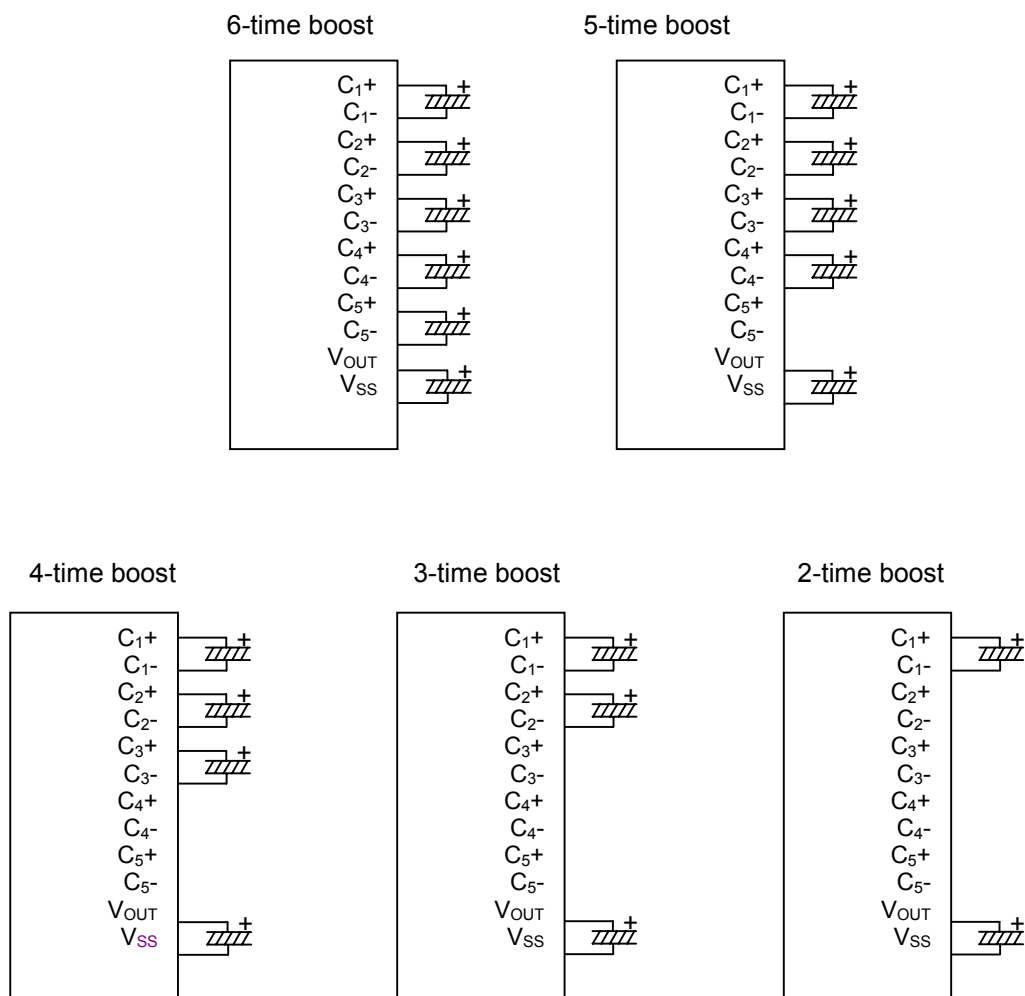


Fig 9

(22) Reference voltage generator

The reference voltage generator is used to produce the reference voltage (V_{BA}), which is output from the V_{BA} terminal and should be input to the V_{REF} terminal.

$$V_{BA} = V_{EE} \times 0.9$$

(23) Voltage regulator

The voltage regulator, composed of a gain control circuit and an operational amplifier, and is used to gain the reference voltage (V_{REF}) and to create the regulated voltage (V_{REG}). The V_{REG} is used as an input voltage to the EVR circuits which is programmed by the "VU" register of the "Boost level" instruction.

$$V_{REG} = V_{REF} \times N \quad (\text{N: register value for the boost level})$$

(24) Electrical variable resistor (EVR)

The EVR is variable within 128-step, and is used to fine-tune the LCD driving voltage (V_{LCD}) by programming the "DV" register of the "EVR control" instruction, so that it is possible to optimize the contrast level of LCD panels.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (\text{M: register value for the EVR})$$

(25) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates the V_{LCD} , V_1 , V_2 , V_3 and V_4 with internal E.V.R and the bleeder resistors. The bias ratio of the LCD driving voltage is selected out of 1/4, 1/5, 1/6, 1/7, 1/8, 1/9 and 1/10.

In using the internal power supply, the capacitors CA_2 must be connected to the V_{LCD} , V_1 , V_2 , V_3 and V_4 terminals, and the CA_2 value must be determined by the evaluation with actual LCD modules.

In using the external power supply, the external LCD driving voltages such as the V_{LCD} , V_1 , V_2 , V_3 and V_4 are supplied and the internal power supply circuits must be set to "OFF" by $DCON = AMPON = "0"$. In this mode, voltage booster terminals such as C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , V_{EE} , V_{REF} and V_{REG} must be opened.

In case that the voltage booster is not used but only some parts of internal power supply circuits (Voltage followers, Voltage regulator and EVR) are used, the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} and C_{5-} terminals must be opened. And, the external power supply is input to the V_{OUT} terminal, and the reference voltage to the V_{REF} terminal. The capacitor CA_3 must connect to the V_{REG} terminal for voltage stabilization.

Using internal power supply circuits without the reference voltage generator (1)
(6-time boost)

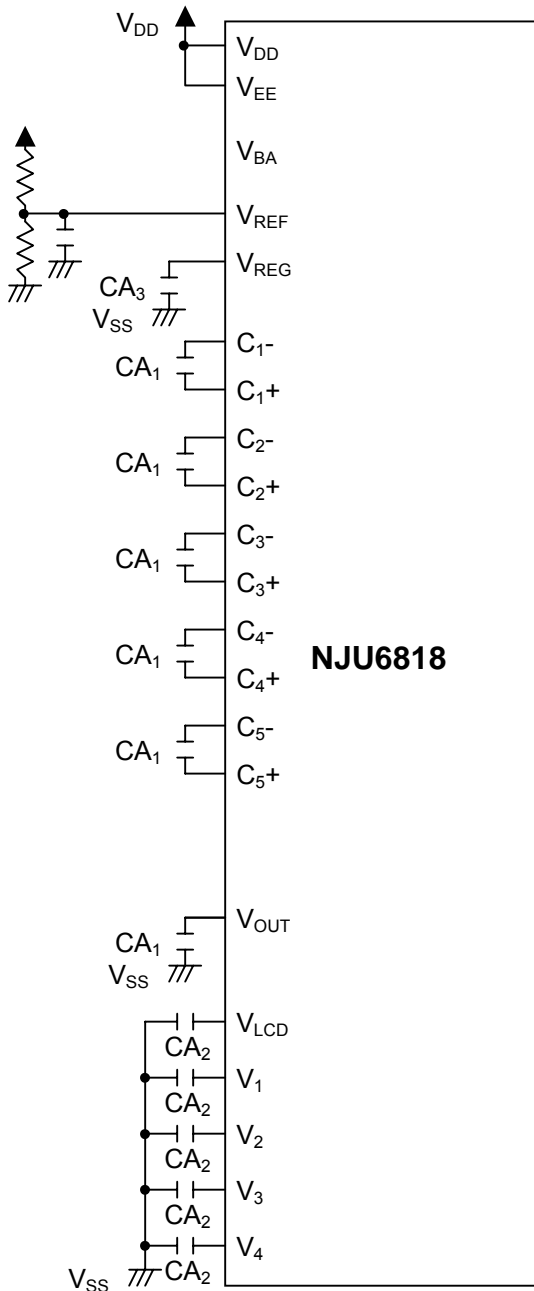


Fig 12

Using internal power supply circuits without the reference voltage generator (2)
(6-time boost)

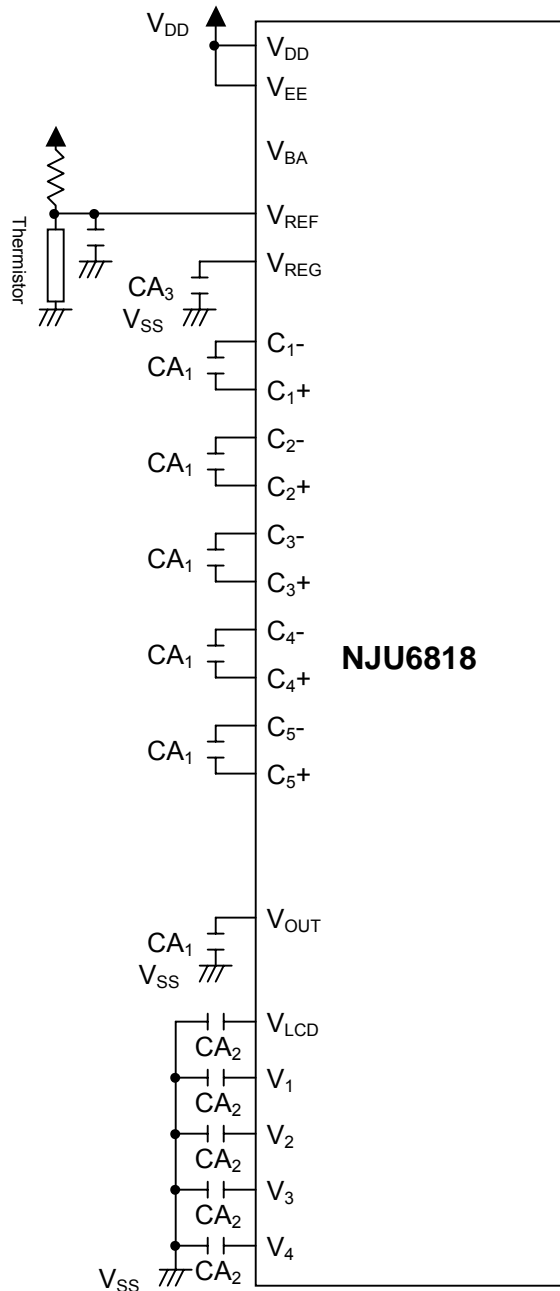


Fig 13

Reference value

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

Note) B grade capacitors are required.

Using internal power supply circuits
without the voltage booster

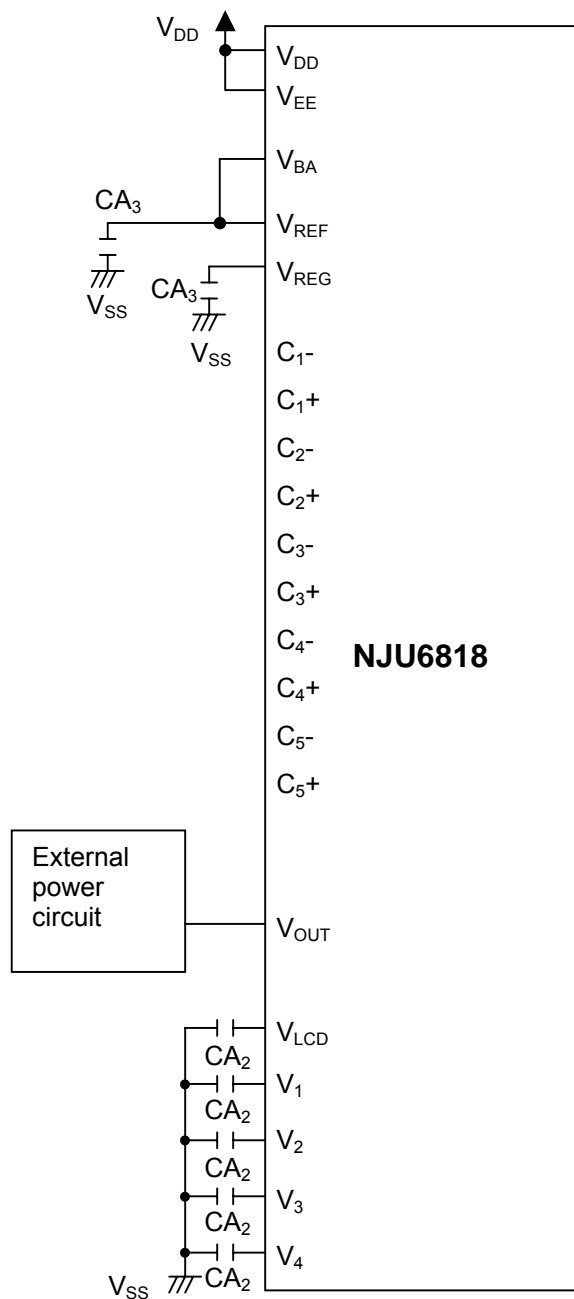


Fig 14

Reference value

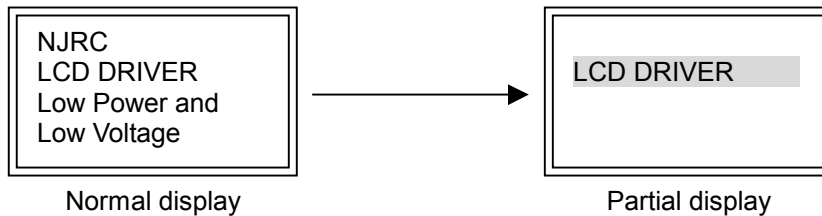
CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

Note) B grade capacitors are required.

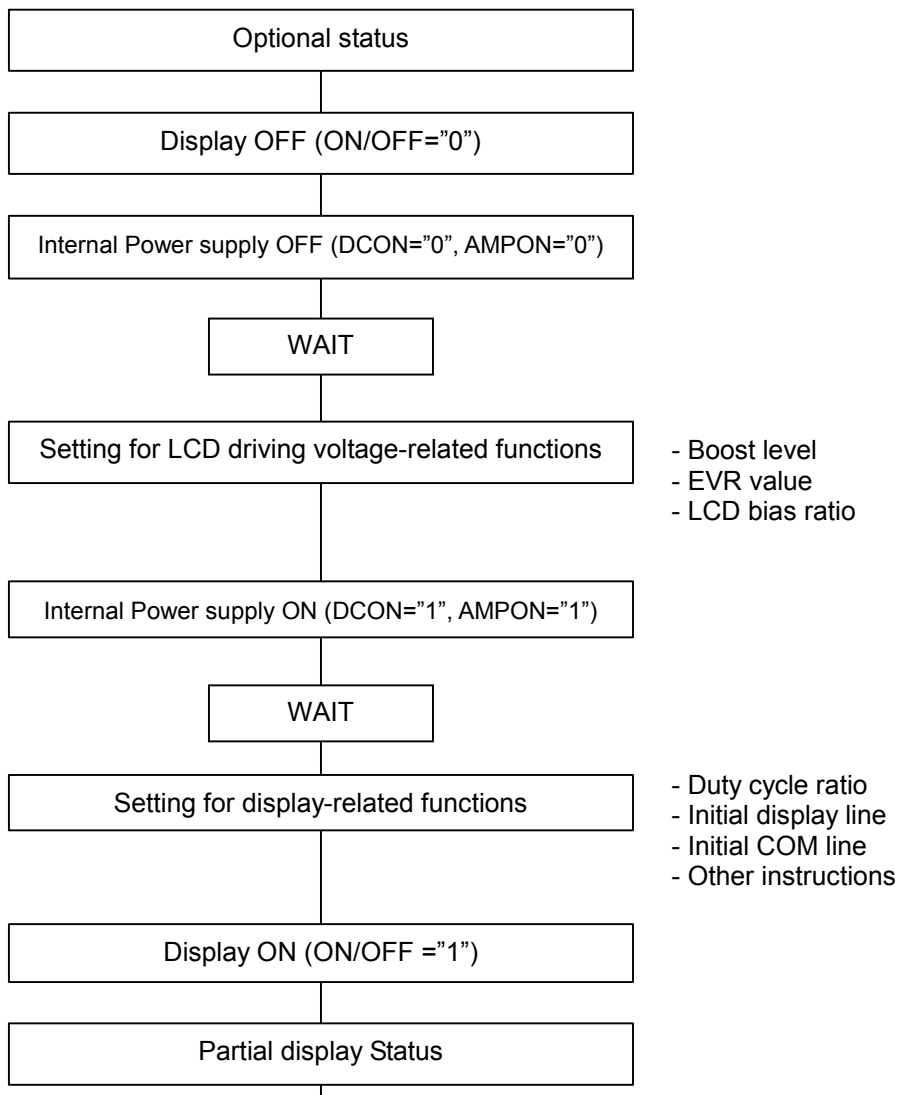
(26) Partial display function

The partial display function is used to partially specify some parts of display area on LCD panels. By using this function, LCD modules can work in lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. It is usually used to display a time and calendar, and is also used to optimize the LSI condition in accordance with the display size. It can be programmed to select the duty cycle ratio (1/13, 1/17, 1/27, 1/33, 1/39, 1/47, 1/57, 1/69, 1/77, 1/81 in "DSE" is "0"), the LCD bias ratio, the boost level and the EVR value by the instructions.

Partial display image



Partial display sequence



(27) Discharge circuit

Discharge circuit is used to discharge the electric charge of the capacitors on the V₁ to V₄ and the VLCD terminals. This circuit is activated by setting "0" to the "DIS" register of the "Discharge" instruction or by setting the "RESb" terminal to "0" level. The "Discharge ON/OFF" instruction is usually required just after the internal power supply is turned off by setting "0" into the "DCON" and "AMPON" registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

(28) Reset circuit

The reset circuit initializes the LSI into the following default status. It is activated by setting the RESb terminal to "0". The RESb terminal is usually required to connect to MPU reset terminal in order that the LSI can be initialized at the same timing of the MPU.

● Default status

1. DDRAM display data	:Undefined
2. Column address	:(00) _H
3. Row address	:(00) _H
4. Initial display line	:(0) _H (1st line)
5. Display ON/OFF	:OFF
6. Reverse display ON/OFF	:OFF (normal)
7. Duty cycle ratio	:1/81 duty(DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM scan direction	:COM ₀ → COM ₇₉
10. Increment mode	:OFF
11. Reverse SEG direction	:OFF (normal)
12. SWAP mode	:OFF (normal)
13. EVR value	:(0, 0, 0, 0, 0, 0, 0, 0)
14. Internal power supply	:OFF
15. Display mode	:Gradation display mode
16. LCD bias ratio	:1/9 bias
17. Gradation Palette 0	:(0, 0, 0, 0, 0)
18. Gradation Palette 1	:(0, 0, 0, 1, 1)
19. Gradation Palette 2	:(0, 0, 1, 0, 1)
20. Gradation Palette 3	:(0, 0, 1, 1, 1)
21. Gradation Palette 4	:(0, 1, 0, 0, 1)
22. Gradation Palette 5	:(0, 1, 0, 1, 1)
23. Gradation Palette 6	:(0, 1, 1, 0, 1)
24. Gradation Palette 7	:(0, 1, 1, 1, 1)
25. Gradation Palette 8	:(1, 0, 0, 0, 1)
26. Gradation Palette 9	:(1, 0, 0, 1, 1)
27. Gradation Palette 10	:(1, 0, 1, 0, 1)
28. Gradation Palette 11	:(1, 0, 1, 1, 1)
29. Gradation Palette 12	:(1, 1, 0, 0, 1)
30. Gradation Palette 13	:(1, 1, 0, 1, 1)
31. Gradation Palette 14	:(1, 1, 1, 0, 1)
32. Gradation Palette 15	:(1, 1, 1, 1, 1)
33. Gradation mode control	:Variable gradation mode
34. Data bus length	:8-bit data bus length
35. Discharge circuit	:(DIS/DIS2) : "0"

(29) Power supply ON/OFF sequences

The following paragraphs describe power supply ON/OFF sequences, which are to protect the LSI from over current.

(29-1) Using an external power supply

Power supply ON sequence

Logic voltage (V_{DD}) must be always input first, and next the LCD driving voltages (V_1 to V_4 and V_{LCD}) are turned on. In using the external V_{OUT} , the V_{DD} must be input first, next the reset operation must be performed, and finally the V_{OUT} can be input

Power supply OFF sequence

Either the reset operation, cutting off the V_1 to V_4 and V_{LCD} from the LSI, by the RESb terminal or the "Power control" instruction must be performed first, and next the V_{DD} is turned off. It is recommended that a series-resistor between 50Ω and 100Ω is added on the V_{LCD} line (or V_{OUT} line in using only the external V_{OUT} voltage) in order to protect the LSI from the over current.

(29-2) Using the internal power supply circuits

Power supply ON sequence

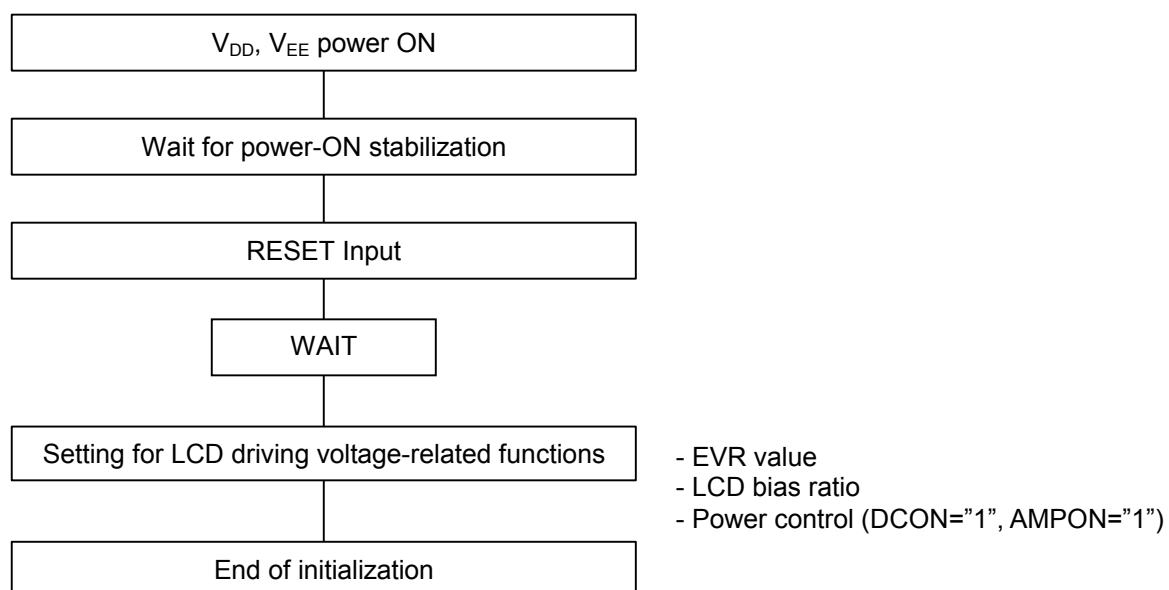
The V_{DD} must be input first, next the reset operation must be performed, and finally the V_1 to V_4 and the V_{LCD} can be turned on by setting "1" to the "DCON" and "AMPON" registers of the "Power control" instruction.

Power supply OFF sequence

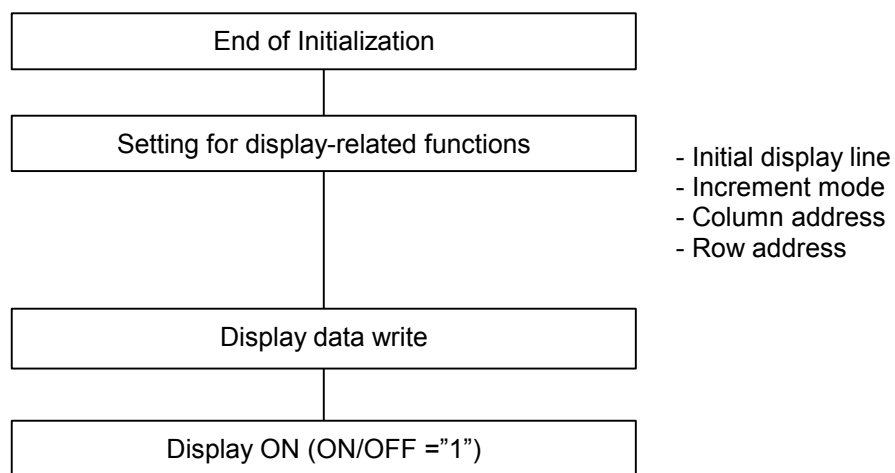
Either the reset operation by the RESb terminal or the "Power control" instruction must be performed first, and next the input voltage for the voltage booster (V_{EE}) and the V_{DD} can be turned off. If the V_{EE} is supplied from different power sources for the V_{DD} , the V_{EE} is turned off first and next the V_{DD} is turned off

(30) Referential instruction sequences

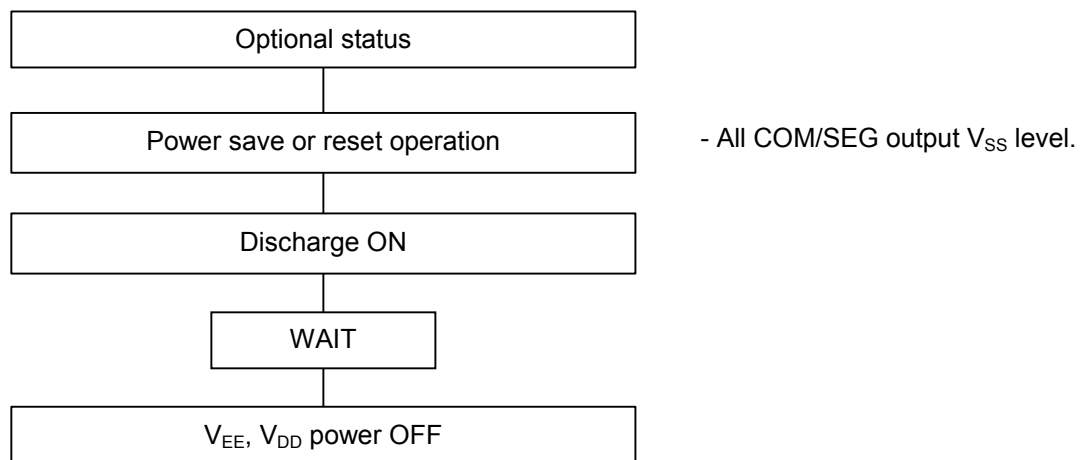
(30-1) Initialization in using the internal power supply circuits



(30-2) Display data writing



(30-3) Power OFF



(31) Instruction table

Instruction Table (1)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Display data write	0	0	1	0	0/1	0/1	0/1	Write Data								Write display data to DDRAM
Display data read	0	0	0	1	0/1	0/1	0/1	Read Data								Read display data from DDRAM
Column address (Lower) [0 _H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	DDRAM column address
Column address (Upper) [1 _H]	0	1	1	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	DDRAM column address	
Row address (Lower) [2 _H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	DDRAM row address
Row address (Upper) [3 _H]	0	1	1	0	0	0	0	0	0	1	1	*	AY6	AY5	AY4	DDRAM row address
Initial display line (Lower) [4 _H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Row address for an initial COM line (Scan start line)
Initial display line (Upper) [5 _H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Row address for an initial COM line (Scan start line)
N-line inversion (Lower) [6 _H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	The number of N-line inversion
N-line inversion (Upper) [7 _H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	The number of N-line inversion
Display control (1) [8 _H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF	SHIFT: Common direction MON: Gradation or B/W display mode ALLON: All pixels ON/OFF ON/OFF: Display ON/OFF
Display control (2) [9 _H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Reverse display ON/OFF NLIN: N-line inversion ON/OFF, SWAP: SWAP mode ON/OFF REF: Segment direction
Increment control [A _H]	0	1	1	0	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Window addressing mode ON/OFF AIM: Read-modify-write ON/OFF AYI: Row auto-increment mode ON/OFF AXI: Column auto-increment mode ON/OFF
Power control [B _H]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON: Voltage followers ON/OFF HALT: Power save ON/OFF DCON: Voltage booster ON/OFF ACL: Reset
Duty cycle ratio [C _H]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Set LCD duty cycle ratio
Boost level / ID read [D _H]	0	1	1	0	0	0	0	1	1	0	1	IDR	VU2	VU1	VU0	Set boost level Sets ID reading in the serial interface
LCD bias ratio [E _H]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Sets LCD bias ratio
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (2)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A0/A8 (Lower) [0 _H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper) [1 _H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Sets palette values to gradation palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower) [2 _H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper) [3 _H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Sets palette values to gradation palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower) [4 _H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper) [5 _H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Sets palette values to gradation palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower) [6 _H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper) [7 _H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Sets palette values to gradation palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower) [8 _H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper) [9 _H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Sets palette values to gradation palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower) [A _H]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper) [B _H]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Sets palette values to gradation palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower) [C _H]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper) [D _H]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Sets palette values to gradation palette A6(PS=0)/A14(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (3)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette A7/A15 (Lower) [0 _H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper) [1 _H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Sets palette values to gradation palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower) [2 _H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper) [3 _H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Sets palette values to gradation palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower) [4 _H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper) [5 _H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Sets palette values to gradation palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower) [6 _H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper) [7 _H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Sets palette values to gradation palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower) [8 _H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper) [9 _H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Sets palette values to gradation palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower) [A _H]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper) [B _H]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Sets palette values to gradation palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower) [C _H]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper) [D _H]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Sets palette values to gradation palette B5(PS=0)/B13(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (4)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette B6/B14 (Lower) [0 _H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper) [1 _H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Sets palette values to gradation palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower) [2 _H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper) [3 _H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Sets palette values to gradation palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower) [4 _H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper) [5 _H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Sets palette values to gradation palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower) [6 _H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper) [7 _H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Sets palette values to gradation palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower) [8 _H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper) [9 _H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Sets palette values to gradation palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower) [A _H]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper) [B _H]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Sets palette values to gradation palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower) [C _H]	0	1	1	0	0	1	1	1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper) [D _H]	0	1	1	0	0	1	1	1	1	0	1	*	*	*	PC44/ PC124	Sets palette values to gradation palette C4(PS=0)/C12(PS=1)
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag set

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Instruction Table (5)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Gradation palette C5/C13 (Lower) [0 _H]	0	1	1	0	1	0	0	0	0	0	0	PC53/PC133	PC52/PC132	PC51/PC131	PC50/PC130	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper) [1 _H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/PC134	Sets palette values to gradation palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower) [2 _H]	0	1	1	0	1	0	0	0	0	1	0	PC63/PC143	PC62/PC142	PC61/PC141	PC60/PC140	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper) [3 _H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/PC144	Sets palette values to gradation palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower) [4 _H]	0	1	1	0	1	0	0	0	1	0	0	PC73/PC153	PC72/PC152	PC71/PC151	PC70/PC150	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper) [5 _H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/PC154	Sets palette values to gradation palette C7(PS=0)/C15(PS=1)
Initial COM line [6 _H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Scan-starting common driver
Display clock / Duty-1 [7 _H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display clock ON/OFF DSE : Duty-1 ON/OFF
Gradation mode control [8 _H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	*	*	PWM : Variable/Fixed gradation mode C256 : 256-color mode ON/OFF
Data bus length [9 _H]	0	1	1	0	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : High speed access ON/OFF ABS : ABS mode ON/OFF CKS : Internal/external oscillation WLS : Display data Length
EVR control (Lower) [A _H]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Sets EVR level (Lower bit)
EVR control (Upper) [B _H]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Sets EVR level (Upper bit)
Frequency control [D _H]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Oscillation frequency
Discharge ON/OFF [E _H]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge the electric charge in Capacitors on V ₁ to V ₄ , V _{LCD}
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag
Instruction register address [C _H]	0	1	1	0	1	0	0	1	1	0	0	Register address				Sets instruction register address
Instruction register read / ID read	0	1	0	1	0/1	0/1	0/1	ID3	ID2	ID1	ID0	Read Data				Read out instruction register data

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

Note 4) CKS=0: Internal oscillation mode (default)
CKS=1: External oscillation mode

Instruction Table (6)

Instructions	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE ₂	RE ₁	RE ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Window end column address (Lower) [0 _H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Sets column address for end point
Window end column address (Upper) [1 _H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Sets column address for end point
Window end row address (Lower) [2 _H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Sets row address for end point
Window end row address (Upper) [3 _H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Sets row address for end point
Initial reverse line (Lower) [4 _H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Sets address for reverse line
Initial reverse line (Upper) [5 _H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Sets address for reverse line
Last reverse line (Lower) [6 _H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Sets address for reverse line
Last reverse line (Upper) [7 _H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Sets address for reverse line
Reverse line display ON/OFF [8 _H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink type setting LREV : Reverse line display ON/OFF
Gradation palette setting [9 _H]	0	1	1	0	1	0	1	1	0	0	1	*	*	*	PS	PS : Gradation setting
PWM control [A _H]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Sets PWM mode
RE register [F _H]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST ₀	RE ₂	RE ₁	RE ₀	RE flag

Note 1) * : Don't care.

Note 2) [N_H] : Address of instruction register

Note 3) The dual instructions including upper and lower bytes is enabled after either upper or lower bytes are set into the register. The only "EVR control" instruction is enabled after both of the upper and lower bytes are set.

(32) Instruction descriptions

This chapter provides detail descriptions and instructions and instruction registers. Nonexistent instruction codes must not be set into the LSI.

(32-1) Display data write

The "Display data write" instruction is used to write 8-bit display data into the DDRAM.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
Display data							

(32-2) Display data read

The "Display data read" instruction is used to read out 8-bit display data from the DDRAM, where the column address and row address must be specified beforehand by the "column address" and "row address" instructions. The dummy read is required just after the "column address" and "row address" instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
Display data							

(32-3) Column address

The "column address" instruction is used to specify the column address for display data's reading and writing operations. It requires dual bytes for lower 4-bit and upper 4-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 4-bit.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AX7	AX6	AX5	AX4

(32-4) Row address

The "row address" instruction is used to specify the row address for display data read and write operations. It requires dual bytes for lower 4-bit and upper 3-bit data. The instruction for the lower 4-bit data must be executed first, next the instruction for the upper 3-bit. The row address is specified in between 00_H and 4F_H. The setting for nonexistent row address between 50_H and FF_H is prohibited.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AY2	AY1	AY0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	AY6	AY5	AY4

(32-5) Initial display line

The "Initial display line" instruction is used to specify the line address corresponding to the initial COM line. The initial COM line is specified by the "Initial COM line" instruction and indicates the common driver that starts scanning display data.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	LA6	LA5	LA4

LA6	LA5	LA4	LA3	LA2	LA1	LA0	Line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
⋮							⋮
1	0	0	1	1	1	1	79

(32-6) N-line inversion

The "N-line inversion" instruction is used to control the alternate rates of liquid crystal direction. It is programmed to select the N value between 2 and 80, and the FR signal toggles once every N lines by setting "1" into the "NLIN" register of the "Display control (2)" instruction. When the N-line inversion is disabled by setting "0" into the "NLIN" register, the FR signal toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

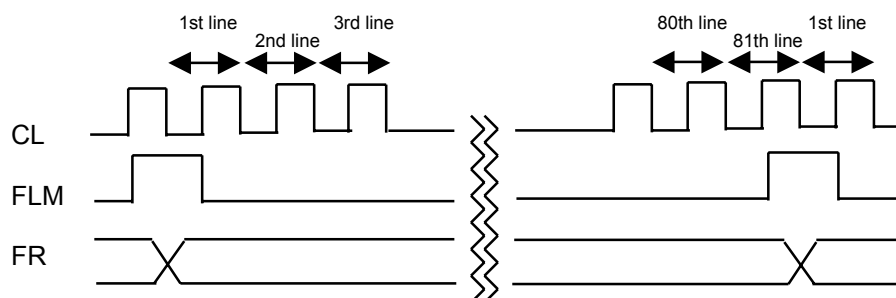
CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	N6	N5	N4

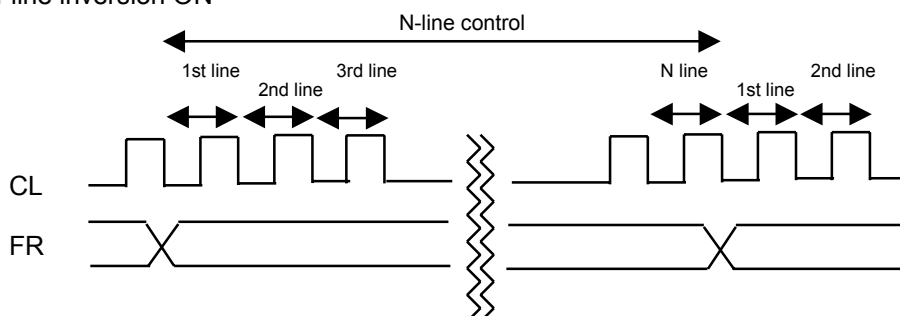
N6	N5	N4	N3	N2	N1	N0	N value
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
⋮							⋮
1	0	0	1	1	1	1	80

N-line Inversion Timing (1/81 duty cycle ratio)

N-line inversion OFF



N-line inversion ON



(32-7) Display control (1)

The "Display control (1)" instruction is used to control display conditions by setting the "Display ON/OFF", "All pixels ON/OFF", "Display mode" and "Common direction" registers.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	SHIFT	MON	ALL ON	ON/OFF

ON/OFF register

ON/OFF=0 : Display OFF (All COM/SEG output the Vss level.)
 ON/OFF=1 : Display ON

All ON register

The "All pixels ON/OFF" register is used to turn on all pixels without changing display data of the DDRAM. The setting for the "All pixels ON/OFF" register has a priority over the "Reverse display ON/OFF" register.

ALLON=0 : Normal
 ALLON=1 : All pixels turn on.

MON register

MON=0 : Gradation mode
 MON=1 : B&W mode

SHIFT register

SHIFT=0 : COM₀ → COM₇₉
 SHIFT=1 : COM₇₉ → COM₀

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(32-8) Display control (2)

The "Display control (2)" instruction is used to control display conditions by setting the "Segment direction", "SWAP mode ON/OFF", "N-line inversion ON/OFF" and "Reverse display ON/OFF" registers.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	REV	NLIN	SWAP	REF

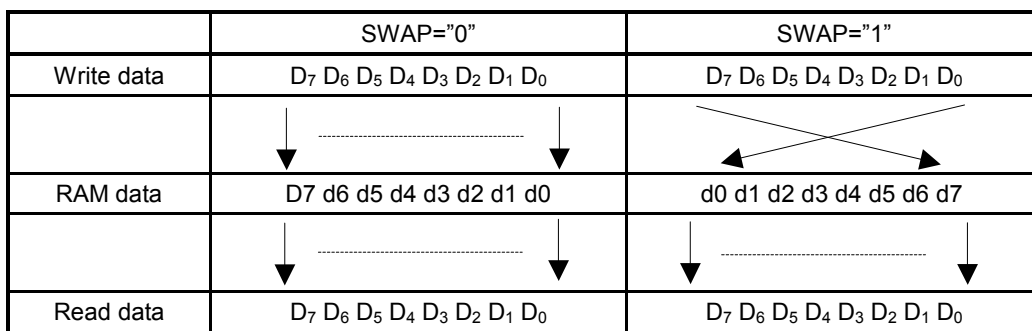
REF register

The "REF" register is used to reverse the assignment between segment drivers and column address, and it is possible to reduce restrictions for placement of the LSI on the LCD module. For more information, see (10) "The relation among the DDRAM column address, display data and segment drivers".

SWAP register

The "SWAP" register is used to reverse the arrangement of display data in the DDRAM.

SWAP=0 : SWAP mode OFF (Normal)
 SWAP=1 : SWAP mode ON



NLIN register

The "NLIN" is used to enable or disable the N-line inversion.

NLIN=0 : N-line inversion OFF (The FR signal toggles by the frame.)
 NLIN=1 : N-line inversion ON (The FR signal toggles once every N lines.)

REV register

The "REV" register is used to enable or disable the reverse display mode that reverses the polarity of display data without changing display data of the DDRAM.

REV=0 : Reverse display mode OFF
 REV=1 : Reverse display mode ON

REV	Display	DDRAM data → Display data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(32-9) Increment control

The "Increment control" instruction is used for the increment mode. In using the auto-increment mode, DDRAM address automatically increments (+1) whenever the DDRAM is accessed by the "Display data write" or "Display data read" instruction. Therefore, once "Display data write" or "Display data read" instruction is established, it is possible to continuously access to the DDRAM without the "column address" and "row address" instructions. The settings for the "AIM", "AXI" and "AYI" registers are listed in the following tables.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	WIN	AIM	AYI	AXI

AIM, AYI and AXI registers

AIM	Increment mode	Note
0	Auto-increment for the both of display data read and write operations	1
1	Auto-increment for the display write operation (Read-modify-write)	2

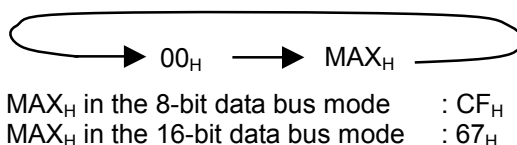
Note 1) It is effective for usual operations accessing successive addresses.

Note 2) It is effective for the read-modify-write operation.

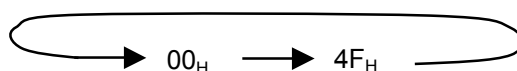
AYI	AXI	Increment mode	Note
0	0	No auto-increment	1
0	1	Auto-increment for the column address	2
1	0	Auto-increment for the row address	3
1	1	Auto-increment for the column address and row address	4

Note 1) Auto-increment is disabled regardless of the "AIM" register.

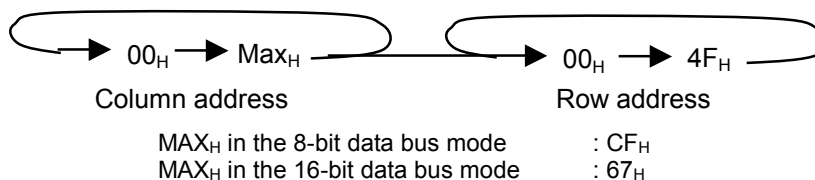
Note 2) Auto-increment of the column address is enabled in accordance with the "AIM" register.



Note 3) Auto-increment of the row address is enabled in accordance with the "AIM" register.



Note 4) Auto-increments of the column address and the row address are enabled. The row address increments whenever the column address reaches to the MAX_H .

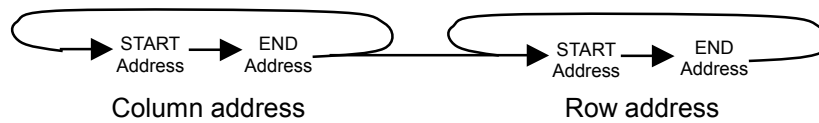


WIN register

The "WIN" register is used to access to the DDRAM for the window display area, where the start point is determined by the "column address" and "row address" instructions, and the end point by the "Window end column address" and "Window end row address" instructions. The setting sequence for the window display area is listed as follows. For more detail, see (6) "Window addressing mode".

WIN=0 : Window addressing mode OFF
WIN=1 : Window addressing mode ON

1. Set WIN=1, AXI=1, and AYI=1 by the "Increment control" instruction
2. Set the start point by the "column address" and "row address" instructions
3. Set the end point by the "Window end column address" and "Window end row address" instructions
4. Enable to access to the DDRAM in the window addressing mode



(32-10) Power control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	AMPON	HALT	DCON	ACL

ACL register

The “ACL” register is used to initialize the internal power supply circuits.

ACL=0 : Initialization OFF (Normal)

ACL=1 : Initialization ON

When the data of the “ACL register” is read out by the “Instruction register read” instruction, the read-out data is “1” during the initialization, and “0” after the initialization. This initialization is performed by using the signal produced by 2 clocks on the OSC₁. For this reason, the wait time for 2 clocks of the OSC₁ is necessary until next instruction.

DCON register

The “DCON” register is used to enable or disable the voltage booster.

DCON=0 : Voltage booster OFF

DCON=1 : Voltage booster ON

HALT register

The “HALT” register is used to enable or disable the power save mode. It is possible to reduce operating current down to stand-by level. The internal status in the power save mode is listed below.

HALT=0 : Power save OFF (Normal)

HALT=1 : Power save ON

Internal status in the power save mode

- The oscillation circuits and internal power supply circuits are halted.
- All segment and common drivers output the V_{SS} level.
- The clock input into the OSC₁ is inhibited.
- The display data in the DDRAM is maintained.
- The operational modes before the power save mode are maintained.
- The V₁ to V₄ and the V_{LCD} are in high impedance.

As a power save ON sequence, the “Display OFF” must be executed first, next the “Power save ON” instruction, and then all common and segment drivers output the V_{SS} level. And as power save OFF sequence, the “Power save OFF” instruction is executed first, next the “Display ON” instruction. If the “Power save OFF” instruction is executed in the display ON status, unexpected pixels may instantly turn on.

AMPON register

The “AMPON” register is used to enable or disable the voltage followers, voltage regulator and EVR.

AMPON=0 : The voltage followers, the voltage regulator and the EVR OFF

AMPON=1 : The voltage followers, the voltage regulator and the EVR ON

(32-11) Duty cycle ratio

The "Duty cycle ratio" instruction is used to select LCD duty cycle ratio for the partial display function. The partial display function specifies some parts of display area on a LCD panel in the condition of lower duty cycle ratio, lower LCD bias ratio, lower boost level and lower LCD driving voltage. Therefore, it is possible to optimize the LSI's conditions with extremely low power consumption.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	DS3	DS2	DS1	DS0

DS3	DS2	DS1	DS0	Duty cycle ratio		Row way displays
				DSE=0	DES=1	
0	0	0	0	1/81	1/80	80 commons
0	0	0	1	1/77	1/76	76 commons
0	0	1	0	1/69	1/68	68 commons
0	0	1	1	1/57	1/56	56 commons
0	1	0	0	1/47	1/46	46 commons
0	1	0	1	1/39	1/38	38 commons
0	1	1	0	1/33	1/32	32 commons
0	1	1	1	1/27	1/26	26 commons
1	0	0	0	1/17	1/16	16 commons
1	0	0	1	1/13	1/12	12 commons
1	0	1	0	Inhibited		
1	0	1	1	Inhibited		
1	1	0	0	Inhibited		
1	1	0	1	Inhibited		
1	1	1	0	Inhibited		
1	1	1	1	Inhibited		

The duty cycle ratio is controlled by the "DS3 to DS0" registers of the "Duty cycle ratio" instruction and the "DSE" register of the "Display clock / Duty-1" instruction.

- DSE=0 : The number of commons +1 (Duty cycle ratio in the default setting)
- DSE=1 : The number of commons (Duty-1)

When the "DSE" is "0", all common drivers output non-selective levels in period of lost common. And the segment drivers output the same data for the last line as the data for previous line: For instance they output the same data for the 80th and 81st lines when the duty cycle ratio is set to 1/81. For the setting of the "DSE" register, see (32-17) "Display clock / Duty-1".

(32-12) Boost level

The "Boost level" is used to select multiple of the voltage booster for the partial display function.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	IDR	VU2	VU1	VU0

a) ID read in serial interface

ID data can be read out by setting IDR=1.

b) Boost level set

VU2	VU1	VU0	Boost level
0	0	0	1-time (No boost)
0	0	1	2-time
0	1	0	3-time
0	1	1	4-time
1	0	0	5-time
1	0	1	6-time
1	1	0	Inhibited
1	1	1	Inhibited

(32-13) LCD bias ratio

The "LCD bias ratio" is used to select the LCD bias ratio for the partial display function.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	B2	B1	B0

B2	B1	B0	LCD bias ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/4
1	1	0	1/10
1	1	1	Inhibited

(32-14) RE flag

The "RE flag" registers are used to determine the contents for the RE registers (RE₂, RE₁ and RE₀), and it is possible to access to the instruction registers.

The data of the "TST₀" register must be "0", and it is used for maker tests only.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	TST0	RE2	RE1	RE0

(32-15) Gradation palette A, B and C

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	PA04/ PA84

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	*	PA14/ PA94

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	PA24/ PA104

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	*	PA34/ PA114

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PA44/ PA124

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	*	PA54/ PA134

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	*	*	PA64/ PA144

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	PA74/ PA154

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	*	PB04/ PB84

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	PB14/ PB94

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	*	PB24/ PB104

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PB34/ PB114

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	*	PB44/ PB124

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	*	*	PB54/ PB134

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	PB64/ PB144

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	*	PB74/ PB154

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	PC04/ PC84

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	*	PC14/ PC94

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PC24/ PC104

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	*	*	PC34/ PC114

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	*	*	PC44/ PC124

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	PC54/ PC134

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	*	*	PC64/ PC144

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	*	*	PC74/ PC154

Gradation palette table (Variable gradation mode, PWM="0" and MON="0")

(Palette Aj, Palette Bj, Palette Cj (j=0 to 15))

Palette value	Gradation level	Gradation palette	Palette value	Gradation level	Gradation palette
0 0 0 0 0	0	Palette 0(default)	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette 8(default)
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette 1(default)	1 0 0 1 1	19/31	Palette 9(default)
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette 2(default)	1 0 1 0 1	21/31	Palette 10(default)
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette 3(default)	1 0 1 1 1	23/31	Palette 11(default)
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette 4(default)	1 1 0 0 1	25/31	Palette 12(default)
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette 5(default)	1 1 0 1 1	27/31	Palette 13(default)
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette 6(default)	1 1 1 0 1	29/31	Palette 14(default)
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette 7(default)	1 1 1 1 1	31/31	Palette 15(default)

(32-16) Initial COM line

The "Initial COM line" instruction is used to specify the common driver that starts scanning display data. The line address, corresponding to the initial COM line, is specified by the "Initial display line" instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	SC3	SC2	SC1	SC0

SC3	SC2	SC1	SC0	Initial COM line (SHIFT=0)	Initial COM line (SHIFT=1)
0	0	0	0	COM0	COM79
0	0	0	1	COM4	COM75
0	0	1	0	COM8	COM71
0	0	1	1	COM16	COM63
0	1	0	0	COM24	COM55
0	1	0	1	COM32	COM47
0	1	1	0	COM40	COM39
0	1	1	1	COM48	COM31
1	0	0	0	COM56	COM23
1	0	0	1	COM64	COM15
1	0	1	0	COM72	COM7
1	0	1	1	Inhibited	Inhibited
1	1	0	0	Inhibited	Inhibited
1	1	0	1	Inhibited	Inhibited
1	1	1	0	Inhibited	Inhibited
1	1	1	1	Inhibited	Inhibited

SHIFT=0: Positive scan direction

(COM₀ → COM₇₉)

SHIFT=1: Negative scan direction

(COM₇₉ → COM₀)

(32-17) Display clock / Duty-1

The "Display clock / Duty-1" instruction is used to enable or disable the display clocks (CL, FLM, FR, and CLK), and to control ON/OFF of the "Duty-1". For more detail about the "Duty-1", see (32-11) "Duty cycle ratio".

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	DSE	SON

SON=0: CL, FLM, FR, and CLK are level "0"

SON=1: CL, FLM, FR, and CLK outputs are active.

DSE=0: Duty-1 OFF

DSE=1: Duty-1 ON

(32-18) Gradation mode control

The "Gradation mode control" is used to select display mode as follows.

CSb	RS	RDb	WRb	RE2	RE1	RE0		D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	0		1	0	0	0	PWM	C256	*	*

PWM register

- PWM=0: Variable gradation mode
(Variable 16-gradation levels out of 32-gradation level of the gradation palette)
- PWM=1: Fixed gradation mode
(Fixed 8-gradation levels)

C256 register

- C256=0 256-color mode OFF (4,096-color in the default setting)
- C256=1 256-color mode ON

(32-19) Data bus length

The "Data bus length" instruction is used to select 8- or 16- bit data bus length and determine the internal or external oscillation. In the 16-bit data bus mode, instruction data must be 16-bit (D₁₅ to D₀) as well as display data. However, for the access to the instruction registers, the lower 8-bit data (D₇ to D₀) of the 16-bit data is valid. For the access to the DDRAM, all of the 16-bit data (D₁₅ to D₀) is valid.

CSb	RS	RDb	WRb	RE2	RE1	RE0		D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	0		1	0	0	1	HSW	ABS	CKS	WLS

HSW register

- HSW =0 :High speed access mode OFF
- HSW=1 :High speed access mode ON (only in the 8-bit data bus length)

ABS register

- ABS=0 :ABS mode OFF (normal)
- ABS=1 :ABS mode ON

WLS register

- WLS=0 :8-bit data bus length
- WLS =1 :16-bit data bus length

CKS register

- CKS =0 :Internal oscillation
(The OSC₁ terminal must be fixed "1" or "0".)
- CKS =1 :External oscillation
(By the external clock into the OSC₁ or external resistor between the OSC₁ and OSC₂.
OSC₂ should be open when clock is inputted from OSC₁.)

(32-20) EVR control

The “EVR control” instruction is used to fine-tune the LCD driving voltage (V_{LCD}), so that it is possible to optimize contrast level for a LCD panel.

This instruction must be programmed by upper 3-bit data first, next lower 4-bit data. And it becomes enabled when the lower 4-bit data is programmed, so that it can prevent unexpected high voltage for the V_{LCD} from being generated.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DV3	DV2	DV1	DV0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	*	DV6	DV5	DV4

DV6	DV5	DV4	DV3	DV2	DV1	DV0	VLCD
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

The formula of the V_{LCD} is shown below.

$$V_{LCD} [V] = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127$$

$$V_{BA} = V_{EE} \times 0.9$$

$$V_{REG} = V_{REF} \times N$$

- V_{BA} : Output voltage of the reference voltage generator
- V_{REF} : Input voltage of the voltage regulator
- V_{REG} : Output voltage of the voltage regulator
- N : Register value for the voltage booster
- M : Register value for the EVR

(32-21) Frequency control

The "Frequency control" instruction is used to control the frame frequency for a LCD panel.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	Rf2	Rf1	Rf0

Rfx register (x=0, 1, 2)

The "Rfx" register is used to determine the feed back resistor value for the internal oscillator, and it is possible to adjust the frame frequency for the LCD modules.

Rf 2	Rf 1	Rf 0	Feedback resistor value
0	0	0	Reference value
0	0	1	0.8 x reference value
0	1	0	0.9 x reference value
0	1	1	1.1 x reference value
1	0	0	1.2 x reference value
1	0	1	0.7 x reference value
1	1	0	1.3 x reference value
1	1	1	Inhibited

(32-22) Discharge ON/OFF

Discharge circuit is used to discharge the electric charge of the capacitors on the V_1 to V_4 and the V_{LCD} terminals. The "Discharge ON/OFF" instruction is usually required just after the internal power supply is turned off by setting "0" into the "DCON" and "AMPON" registers, or just after the external power supply is turned off. During the discharge operation, the internal or external power supply must not be turned on.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	*	DIS2	DIS

DIS=0: Discharge OFF (Capacitors on the V_{LCD} , V_1 , V_2 , V_3 and V_4)

DIS=1: Discharge ON (Capacitors on the V_{LCD} , V_1 , V_2 , V_3 and V_4)

DIS2=0: Discharge OFF (Resistance between V_{OUT} and V_{EE})

DIS2=1: Discharge ON (Resistance between V_{OUT} and V_{EE})

Note) V_{OUT} and V_{EE} are internally connected with the resistor (100k Ω typical) in the power-ON.

(32-23) Instruction register address

The "Instruction register address" is used to specify the instruction register address, so that it is possible to read out the contents of the instruction registers in combination with the "Instruction register read" instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	RA3	RA2	RA1	RA0

(32-24) Instruction register read / ID read

The "Instruction register read" instruction is used to read out the contents of the instruction register in combination with the "Instruction register address" instruction. Upper 4-bit of the read-out data is assigned to the ID data.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D7	D6	D5	D4	D3	D2	D1	D0
ID3	ID2	ID1	ID0	Internal register data read			

(32-25) Window end column address

The "Window end column address" is used to specify the column address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	EX3	EX2	EX1	EX0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	EX7	EX6	EX5	EX4

(32-26) Window end row address set

The "Window end row address" is used to specify the row address for the window end point. The lower 4-bit data is required to be programmed first and then the upper 3-bit data can be programmed.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	EY3	EY2	EY1	EY0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	EY6	EY5	EY4

(32-27) Initial reverse line

The "Initial reverse line" instruction is used to specify the initial reverse line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 3-bit data. It is programmed in between 00_H and 4F_H and the line address beyond 4F_H is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LS3	LS2	LS1	LS0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	LS6	LS5	LS4

(32-28) Last reverse line

The "Last reverse line" instruction is used to specify the last reverse line address for the reverse line display. Lower 4-bit data must be programmed first, next upper 3-bit. It is programmed in between 00_H and 4F_H and the line address beyond the 4F_H is inhibited. The address relation: LSi < LEi (i=7 to 0) must be maintained in the reverse line display.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	LE3	LE2	LE1	LE0

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	LE6	LE5	LE4

(32-29) Reverse line display ON/OFF

The "Reverse line display ON/OFF" is used to enable or disable the reverse line display for the blink operation and determine the reverse line display mode.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	*	BT	LREV

LREV register

The "LREV" register is used to enable or disable the reverse line display.

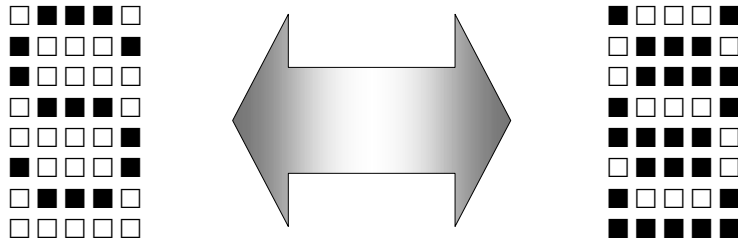
- LREV =0: Reverse line display OFF (Normal)
- LREV =1: Reverse line display ON

BT register

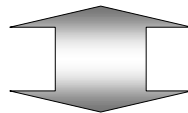
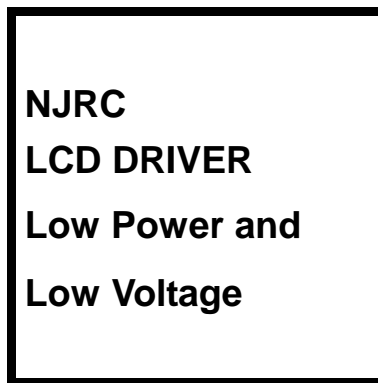
The "BT" register is used to determine the reverse line display mode in the reverse line display ON (LREV=1) status.

- BT =0: Normal reverse line display
- BT =1: Blink once every 32 frames

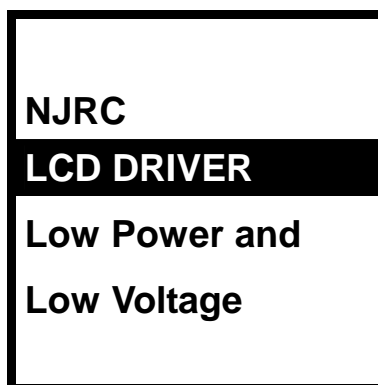
Display examples in the LREV="1" and BT="1"



Blink once every 32 frames



Blink once every 32 frames



←Initial reverse line address

←Last reverse line address

(32-30) Gradation Palette setting control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	*	*	*	PS

PS register

PS=0: Lower 8 Gradation setting
 PS=1: Upper 8 Gradation setting

(32-31) PWM control

The "PWM control" is used to determine the PWM type for segment waveforms, where the type can be specified for each of the SEG*A*_i, SEG*B*_i and SEG*C*_i (i=0-103) drivers.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	PWMS	PWMA	PWMB	PWMC

PWMS register

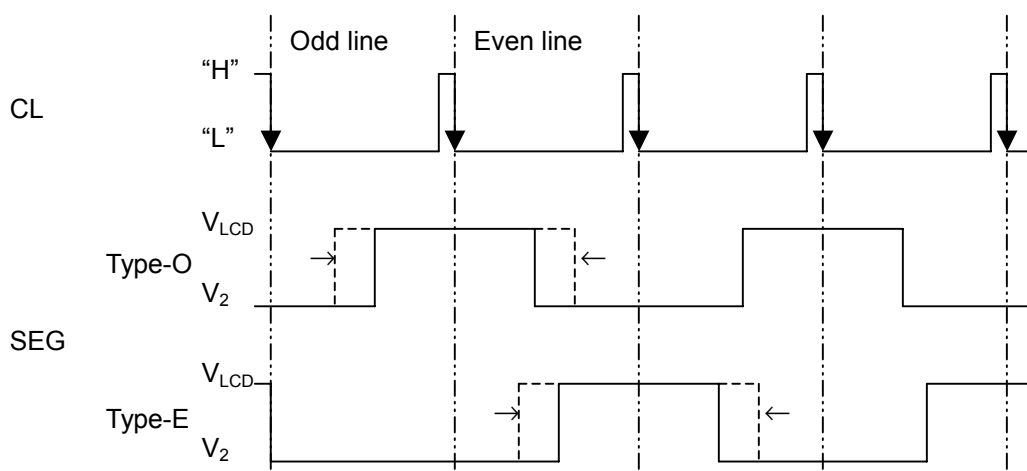
PWMS=0: Type 1
 PWMS=1: Type 2

PWMA, B and C registers

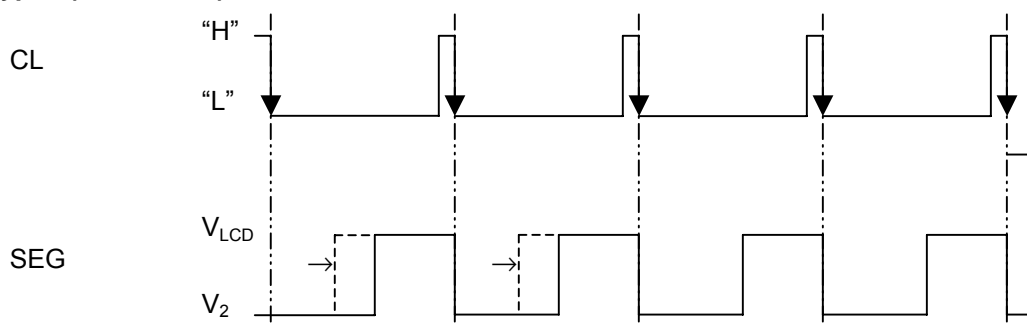
The "PWMA, PWMB and PWMC" registers are used to select the type 1-O or type 1-E.

PWMZ=0 (Z=A, B and C): Type 1-O
 PWMZ=1 (Z=A, B and C): Type 1-E

PWM type1 (PWMS="0")



PWM type2 (PWMS="1")



(33) The relation between Common drivers and Row addresses

Row address assignment of common drivers is programmed by the "SHIFT" register of the "Display control (1)", "Duty cycle ratio", "Initial display line" and "Initial COM line" instructions.

When initial display line is "0"

If the "SHIFT" is "0", the scan direction is normal. When the "LA₀ to LA₆" registers of the "Initial display line" instruction is "0", the "MY" corresponding to the initial COM line is "0" and is increasing during display.

When initial display line is not "0"

If the "SHIFT" is "1", the scan direction is inversed. When the "LA₀ to LA₆" registers of the "Initial display line" instruction is not "0", the "MY" corresponding to the initial COM line is this setting value and is increasing during display.

The followings are examples of setting the start-line 0 or 5 at 1/81, or 1/13 duty.

(33-4) Initial display line "5", 1/81 duty cycle (Common forward scan)

SHIFT="0"(Common forward scan), DS _{3,2,1} ="0000", LA ₈ ...LA ₀ ="00000101"(Initial display line 5)														
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM ₀				5	1	77	69	61	53	45	37	29	21	13
COM ₁						78								
COM ₂						79								
COM ₃					5	0								
COM ₄														
COM ₅														
COM ₆														
COM ₇														
COM ₈						5								
COM ₉														
COM ₁₀							79							
COM ₁₁							0							
COM ₁₂														
COM ₁₃														
COM ₁₄														
COM ₁₅														
COM ₁₆							5							
COM ₁₇														
COM ₁₈								79						
COM ₁₉								0						
COM ₂₀														
COM ₂₁														
COM ₂₂														
COM ₂₃								5						
COM ₂₄														
COM ₂₅														
COM ₂₆									79					
COM ₂₇									0					
COM ₂₈														
COM ₂₉														
COM ₃₀														
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COM ₁₆₀														

(33-5) Initial display line "0", 1/80 duty cycle (Common forward scan, DSE="1")

SHIFT="0"(Common forward scan), DS _{2,1,0} ="0000", LA _{8,7,6,5,4,3,2,1,0} ="00000000"(Initial display line 0) DSE="1"														
SC ₃	SC ₂	SC ₁	SC ₀	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
COM ₀				0	76	72	64	56	48	40	32	24	16	8
COM ₁					79									
COM ₂					0									
COM ₃						79								
COM ₄						0								
COM ₅							79							
COM ₆							0							
COM ₇								79						
COM ₈								0						
COM ₉									79					
COM ₁₀									0					
COM ₁₁										79				
COM ₁₂										0				
COM ₁₃											79			
COM ₁₄											0			
COM ₁₅												79		
COM ₁₆												0		
COM ₁₇													79	
COM ₁₈													0	
COM ₁₉														79
COM ₂₀														0
COM ₂₁														
COM ₂₂														
COM ₂₃														
COM ₂₄														
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COM ₇₈														
COM ₇₉														

DS: Duty cycle ratio, SC: Initial COM line, LA: Initial display line

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +19.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +19.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +19.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

Note 1) D_0 to D_{15} , CSb, RS, RDb, WRb, OSC₁, RESb, TEST₁, TEST₂, terminals.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
		V_{EE}	V_{EE}	2.4		3.3	V
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	$^{\circ}C$	

Note1) Applies to the condition when the reference voltage generator is not used.

Note2) Applies to the condition when the reference voltage generator is used.

Note3) Applies to the condition when the voltage booster is used.

Note4) The following relation among the supply voltages must be maintained.

$$V_{SS} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$$

Note5) The relation: $V_{REF} < V_{EE}$ must be maintained.

DC CHARACTERISTICS 1

$V_{SS} = 0V, V_{DD} = +1.7 \text{ to } +3.3V, T_a = -30 \text{ to } +85^\circ C$

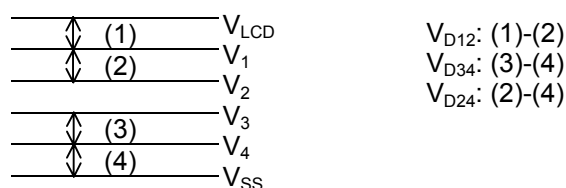
PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	*1
Low level input voltage	V_{IL}		0		$0.2V_{DD}$	V	*1
High level output voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	*2
Low level output voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	*2
High level output voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	*3
Low level output voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	*3
Input leakage current	I_{LI}	$V_i = V_{SS} \text{ or } V_{DD}$	-10		10	μA	*4
Output leakage current	I_{LO}	$V_i = V_{SS} \text{ or } V_{DD}$	-10		10	μA	*5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$	$V_{LCD} = 10V$	1	2	k Ω	*6
			$V_{LCD} = 6V$	2	4		
Stand-by current	I_{STB}	$CSb = V_{DD}, T_a = 25^\circ C$			15	μA	*7
Internal oscillation Frequency	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^\circ C$	309	377	445	kHz	*8
	f_{OSC2}		69	85	101		*9
	f_{OSC3}		10.0	12.2	14.4		*10
External oscillation Frequency	f_{r1}	$R_f = 24k\Omega$		382		kHz	*11
	f_{r2}	$R_f = 120k\Omega$		84			
	f_{r3}	$R_f = 820k\Omega$		12.8			
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 6) $R_L = 500k\Omega (V_{OUT} - V_{SS})$	$(N \times V_{EE}) \times 0.95$			V	*12
Supply current (1)	I_{DD1}	$V_{DD} = 3V$, 6-time booster Whole ON pattern		760	1140	μA	*13
Supply current (2)	I_{DD2}	$V_{DD} = 3V$, 6-time booster Checker pattern		930	1400		
Supply current (3)	I_{DD3}	$V_{DD} = 3V$, 5-time booster Whole ON pattern		520	780		
Supply current (4)	I_{DD4}	$V_{DD} = 3V$, 5-time booster Checker pattern		650	980		
Supply current (5)	I_{DD5}	$V_{DD} = 3V$, 4-time booster Whole ON pattern		360	540		
Supply current (6)	I_{DD6}	$V_{DD} = 3V$, 4-time booster Checker pattern		450	680		
V_{BA} Operating voltage	V_{BA}	$V_{EE} = 2.4 \text{ to } 3.3V$	$(0.9 V_{EE}) \times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE}) \times 1.02$	V	*14
V_{REG} Operating voltage	V_{REG}	$V_{EE} = 2.4 \text{ to } 3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time booster (N=2 to 6)	$(V_{REF} \times N) \times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N) \times 1.03$	V	*15
Output Voltage	V_2		-100	0	+100	mV	*16
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ CLOCK and FRAME FREQUENCY

PARAMETER	SYMBOL	Display mode	Display duty cycle ratio (1/D) <DSE=0>			NOTE
			1/81 to 1/57	1/47 to 1/27	1/17, 1/13	
Internal clock	f_{osc}	16 Gradation mode	$f_{osc} / (62xD)$	$f_{osc} / (62xDx2)$	$f_{osc} / (62xDx4)$	FLM
		Simplified 8 gradation mode	$f_{osc} / (14xD)$	$f_{osc} / (14xDx2)$	$f_{osc} / (14xDx4)$	
		B&W mode	$f_{osc} / (2xD)$	$f_{osc} / (2xDx2)$	$f_{osc} / (2xDx4)$	
External clock	f_{ck}	16 Gradation mode	$f_{ck} / (62xD)$	$f_{ck} / (62xDx2)$	$f_{ck} / (62xDx4)$	
		Simplified 8 gradation mode	$f_{ck} / (14xD)$	$f_{ck} / (14xDx2)$	$f_{ck} / (14xDx4)$	
		B&W mode	$f_{ck} / (2xD)$	$f_{ck} / (2xDx2)$	$f_{ck} / (2xDx4)$	

APPLIED TERMINALS and CONDITIONS

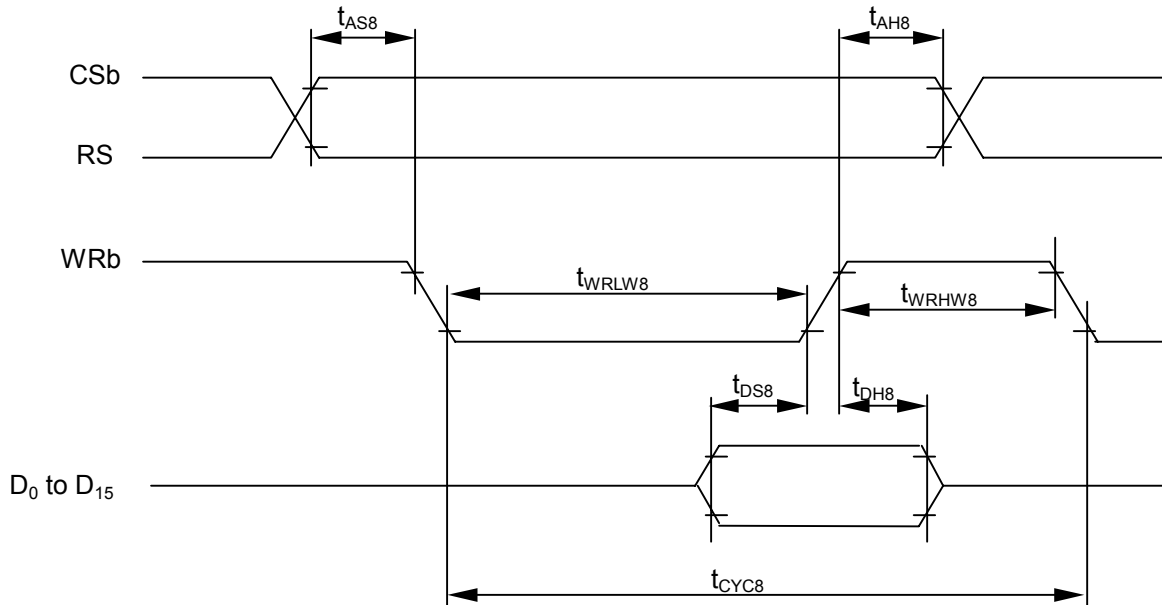
- Note 1) D₀-D₁₅, CSb, RS, RDb, WRb, P/S, SEL68, RESb
- Note 2) D₀-D₁₅
- Note 3) CL, FLM, FR, CLK
- Note 4) CSb, RS, SEL68, RDb, WRb, P/S, RESb, OSC₁
- Note 5) D₀-D₁₅ in high impedance
- Note 6) SEGA₀-SEGA₁₀₃, SEGB₀-SEGB₁₀₃, SEGC₀-SEGC₁₀₃, COM₀-COM₇₉
 - Defines the resistance between the COM/SEG terminals and the power supply terminals (V_{LCD}, V₁, V₂, V₃ and V₄) at the condition of 0.5V deference and 1/9 LCD bias ratio
- Note 7) V_{DD}
 - The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers
- Note 8) OSC
 - Defines the internal oscillation frequency at (Rf2, Rf1, Rf0)=(0,0,0) in the variable gradation mode
- Note 9) OSC
 - Defines the internal oscillation frequency at (Rf2, Rf1, Rf0)=(0,0,0) in the fixed gradation mode
- Note 10) OSC
 - Defines the internal oscillation frequency at (Rf2, Rf1, Rf0)=(0,0,0) in the Black & White mode
- Note 11) V_{DD}=3V, Ta=25°C
- Note 12) V_{OUT}
 - Applies to the condition when the internal voltage booster, the internal oscillator and the internal power circuits are used
 - V_{EE}=2.4V to 3.3V, EVR= (1,1,1,1,1,1,1), 1/4 to 1/10 LCD bias, 1/81 duty cycle, No-load on the COM/SEG drivers
 - RL=500kΩ between the V_{OUT} and the V_{SS}, CA1=CA2=1.0uF, CA3=0.1uF, DCON="1", AMPON="1"
- Note 13) V_{DD}
 - Applies to the condition using the internal oscillator and the internal power circuits, no access between the LSI and MPU
 - EVR= (1,1,1,1,1,1,1), All pixels turned-on or checkerboard display in the gradation mode, No-load on the COM/SEG drivers
 - V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA1=CA2=1.0uF, CA3=0.1uF, DCON="1", AMPON="1", NLIN="0", 1/81 Duty cycle, Ta=25°C
- Note 14) V_{BA}
 - Applies to the condition that V_{BA}=V_{REF} and the voltage booster N= 1, DCON="0", V_{OUT}=13.5V input.
- Note 15) V_{REG}
 - V_{EE}=2.4V to 3.3V, V_{REF}=0.9V_{EE}, V_{OUT}=18V, 1/4 to 1/10 LCD bias ratio, 1/81 duty cycle, EVR=(1,1,1,1,1,1,1),
 - Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 6, CA1=CA2=1.0uF, CA3=0.1uF, DCON="0", AMPON="1", NLIN="0"
- Note 16) V_{LCD}, V₁, V₂, V₃, V₄
 - V_{EE}=3.0V, V_{REF}=0.9V_{EE}, V_{OUT}=15V, 1/4 to 1/10 LCD Bias, EVR= (1,1,1,1,1,1,1), Display OFF, No-load on the COM/SEG drivers, voltage booster N=5, CA1=CA2=1.0uF, CA3=0.1uF, DCON="0", AMPON="1"



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AC CHARACTERISTICS

- Write operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		90		ns	
Enable "L" level pulse width	t_{WRLW8}		35		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

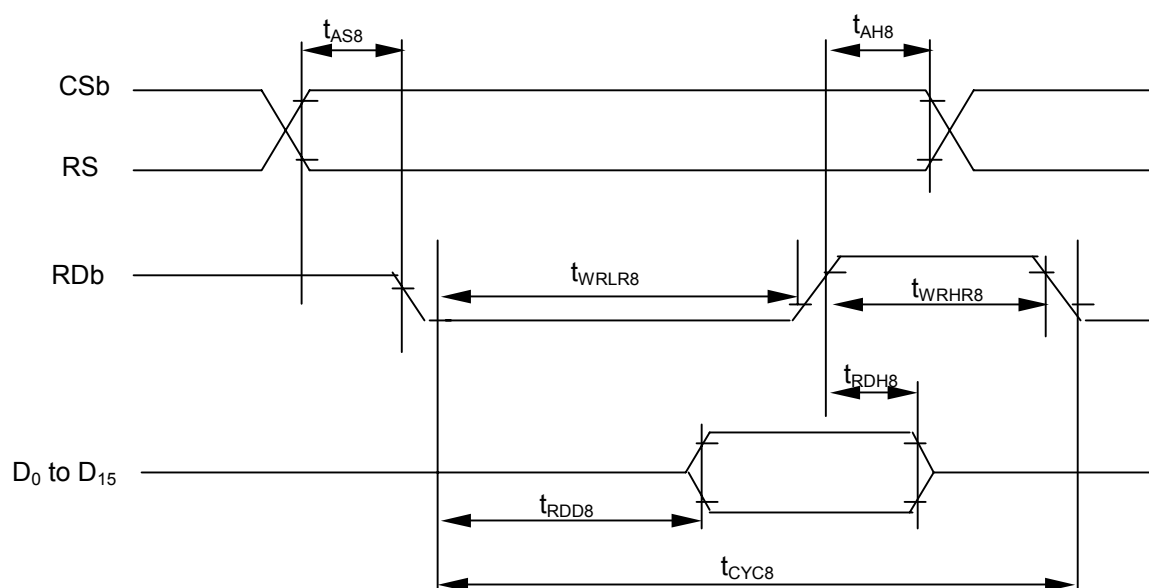
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		160		ns	
Enable "L" level pulse width	t_{WRLW8}		70		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLW8}		80		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Read operation (80-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		0		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		80		ns	
Enable "H" level pulse width	t_{WRHR8}		80		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		0		ns	

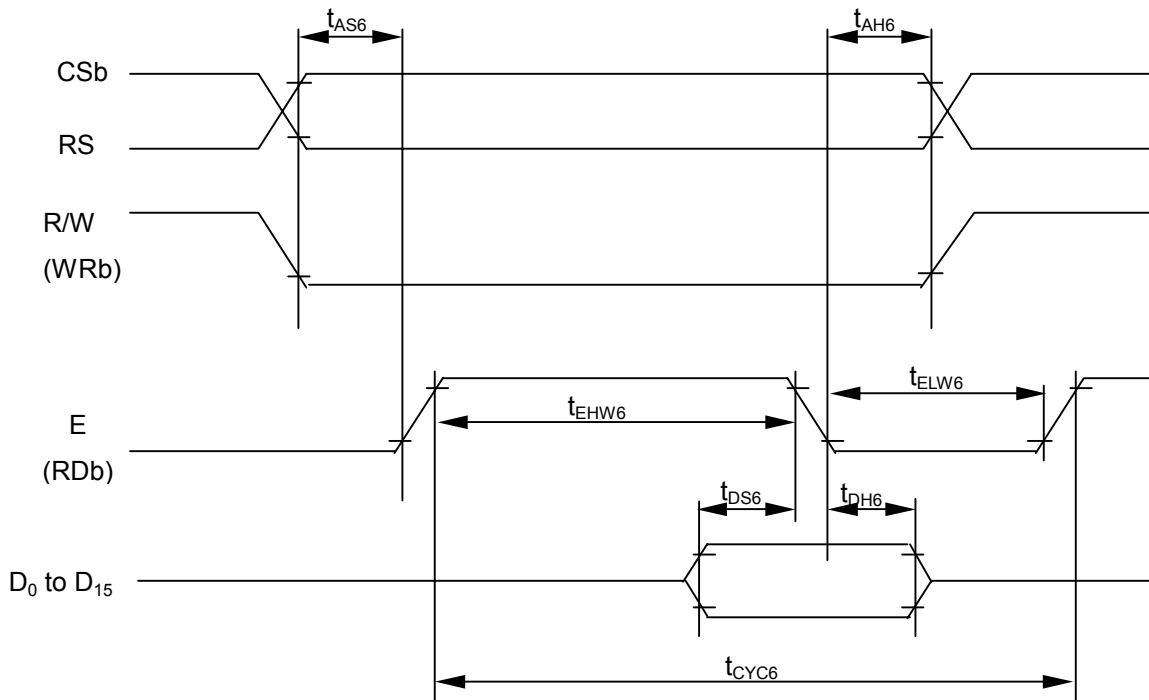
($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		300		ns	RDb
Enable "L" level pulse width	t_{WRLR8}		140		ns	
Enable "H" level pulse width	t_{WRHR8}		140		ns	
Read Data delay time	t_{RDD8}	CL=15pF	0	130	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH8}		0		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

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● Write operation (68-type MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

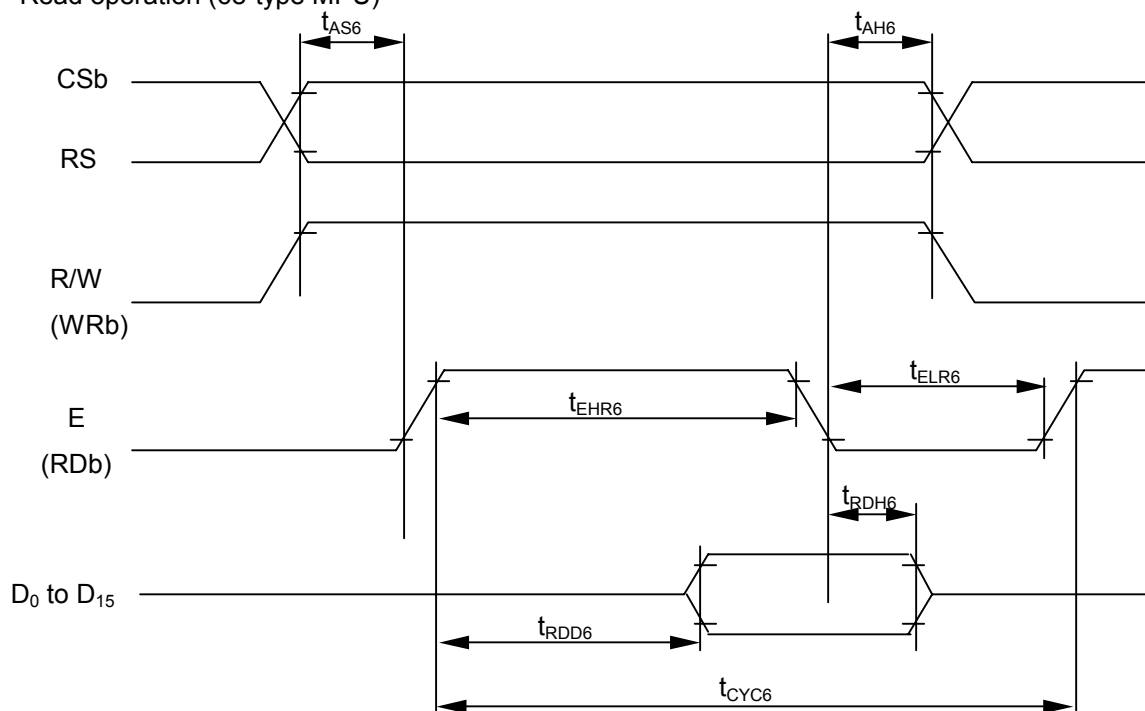
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Read operation (68-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH6}		0		ns	CSb
Address setup time	t _{AS6}		0		ns	RS
System cycle time	t _{CYC6}		180		ns	E
Enable "L" level pulse width	t _{ELR6}		80		ns	
Enable "H" level pulse width	t _{EHR6}		80		ns	
Read Data delay time	t _{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH6}				ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH6}		0		ns	CSb
Address setup time	t _{AS6}		0		ns	RS
System cycle time	t _{CYC6}		180		ns	E
Enable "L" level pulse width	t _{ELR6}		80		ns	
Enable "H" level pulse width	t _{EHR6}		80		ns	
Read Data delay time	t _{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH6}				ns	

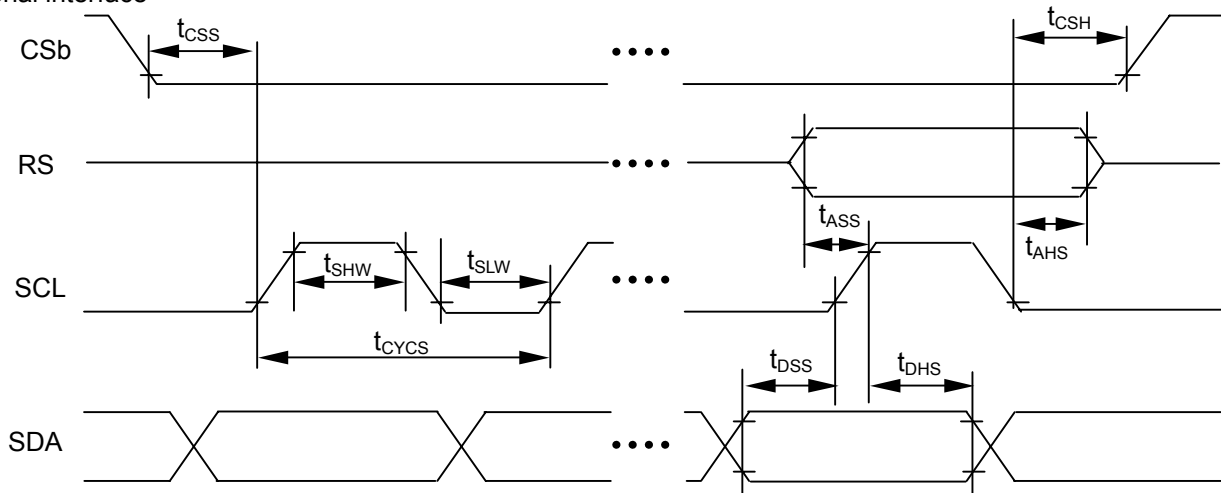
(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH6}		0		ns	CSb
Address setup time	t _{AS6}		0		ns	RS
System cycle time	t _{CYC6}		300		ns	E
Enable "L" level pulse width	t _{ELR6}		140		ns	
Enable "H" level pulse width	t _{EHR6}		140		ns	
Read Data delay time	t _{RDD6}	CL=15pF	0	130	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH6}				ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

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● Serial interface



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCSB}		50		ns	
SCL "H" level pulse width	t_{SHW}	Note 2)	20		ns	SCL
SCL "H" level pulse width 2	t_{SHW2}		300		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		50		ns	
SCL "H" level pulse width	t_{SHW}	Note 2)	20		ns	SCL
SCL "H" level pulse width 2	t_{SHW2}		400		ns	
SCL "L" level pulse width	t_{SLW}		20		ns	
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	

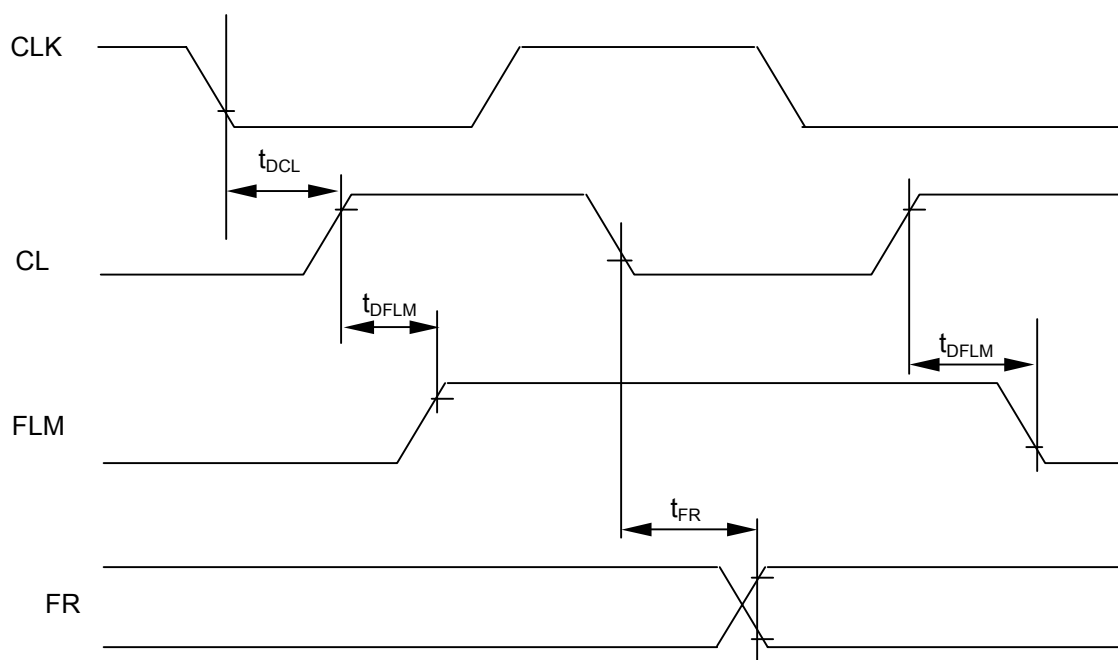
($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		80		ns	
SCL "H" level pulse width	t_{SHW}	Note 2)	35		ns	SCL
SCL "H" level pulse width 2	t_{SHW2}		500		ns	
SCL "L" level pulse width	t_{SLW}		35		ns	
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD} .

Note 2) t_{SHW2} applies to the condition when the ID read-out. Refer to the (18) "Chip Identification" for the detail.

● Display control timing



Output timing

($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing

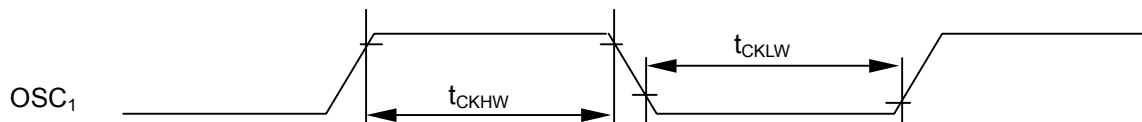
($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD} .

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- Input clock timing

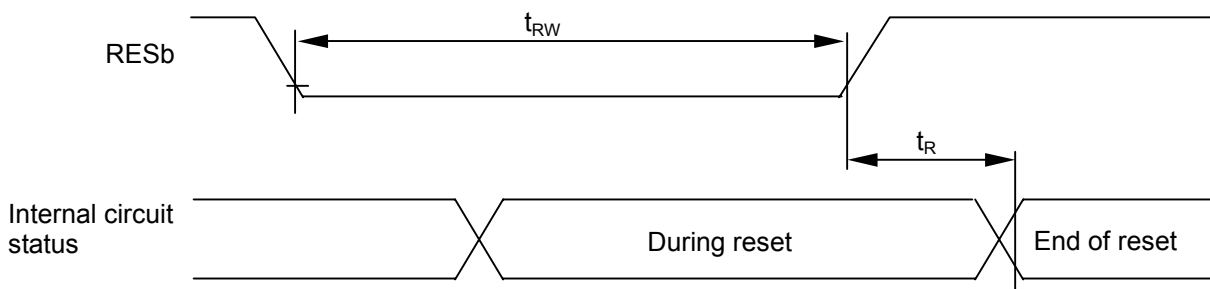


($V_{DD}=1.7$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC ₁ "H" level pulse width (1)	t_{CKHW1}		1.12	1.62	μs	OSC ₁
OSC ₁ "L" level pulse width (1)	t_{CKLW1}		1.12	1.62	μs	*1
OSC ₁ "H" level pulse width (2)	t_{CKHW2}		4.95	7.25	μs	OSC ₁
OSC ₁ "L" level pulse width (2)	t_{CKLW2}		4.95	7.25	μs	*2
OSC ₁ "H" level pulse width (3)	t_{CKHW3}		34.7	50.0	μs	OSC ₁
OSC ₁ "L" level pulse width (3)	t_{CKLW3}		34.7	50.0	μs	*3

- Note) Each timing is specified based on 20% and 80% of V_{DD} .
 Note 1) Applied to the variable gradation mode /MON="0", PWM="0"
 Note 2) Applied to the fixed gradation mode /MON="0", PWM="1"
 Note 3) Applied to the B&W mode /MON="1"

- Reset input timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

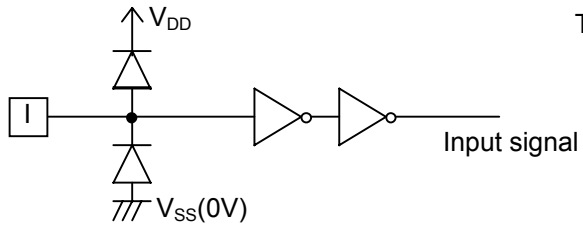
Note) Each timing is specified based on 20% and 80% of V_{DD} .

● Typical characteristic

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	$T_a=+25^{\circ}\text{C}, V_{SS}=0\text{V}, V_{DD}=3.0\text{V}$		10		ns

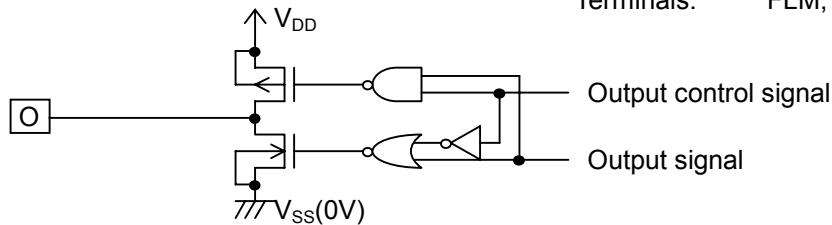
● Input output terminal type

(a) Input circuit



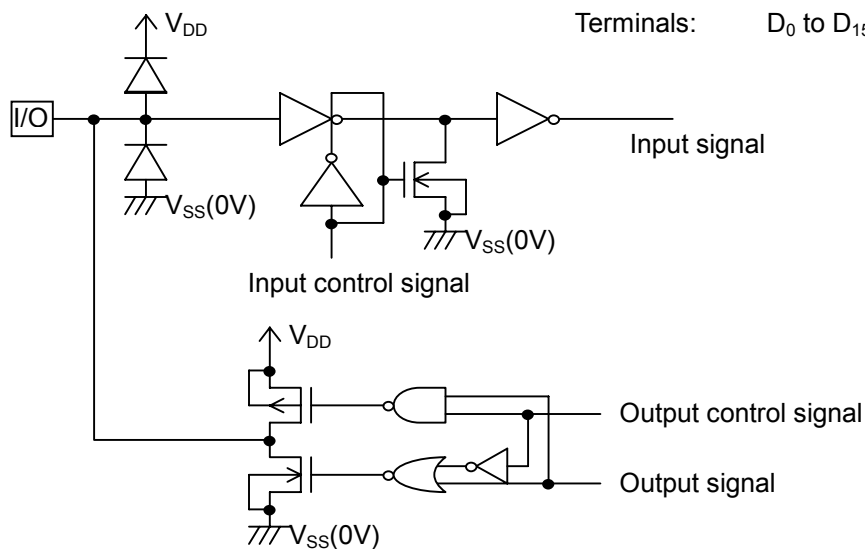
Terminals: CSb, RS, RDb, WRb, SEL68, P/S, RESb

(b) Output circuit



Terminals: FLM, CL, FR, CLK

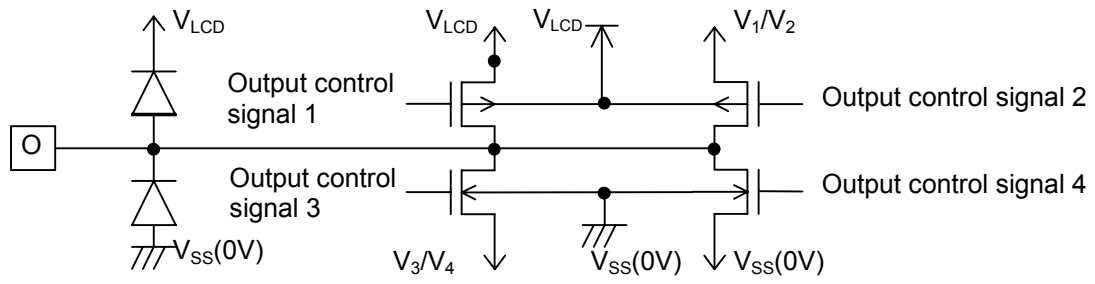
(c) Input/Output circuit



Terminals: D₀ to D₁₅

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(d) Display output circuit

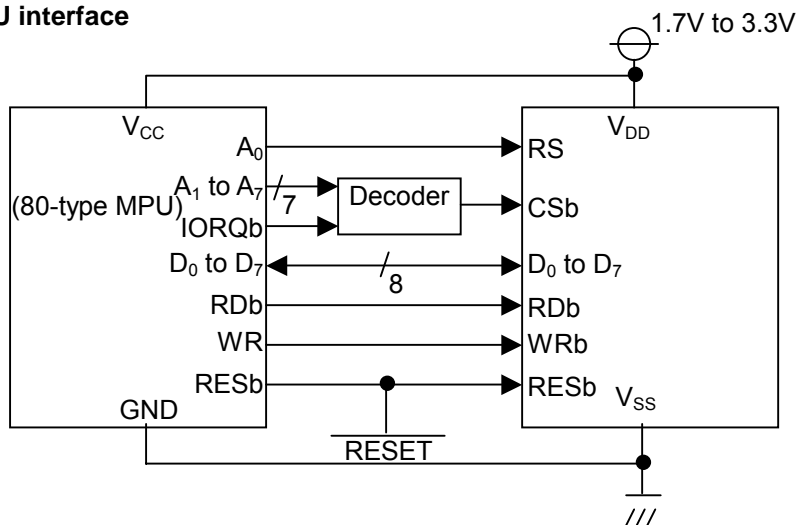


Terminals: SEGA₀ to SEGA₁₀₃
 SEGB₀ to SEGB₁₀₃
 SEGC₀ to SEGC₁₀₃
 COM₀ to COM₇₉

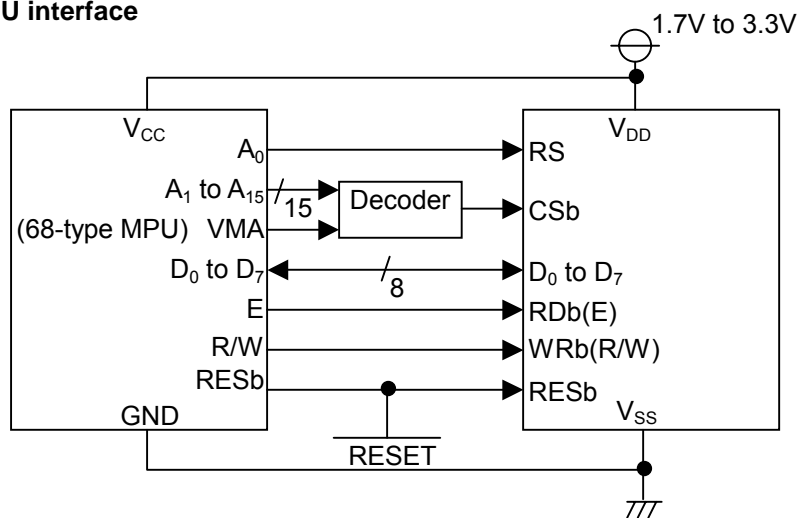
APPLICATION CIRCUIT EXAMPLES

(1) MPU Connections

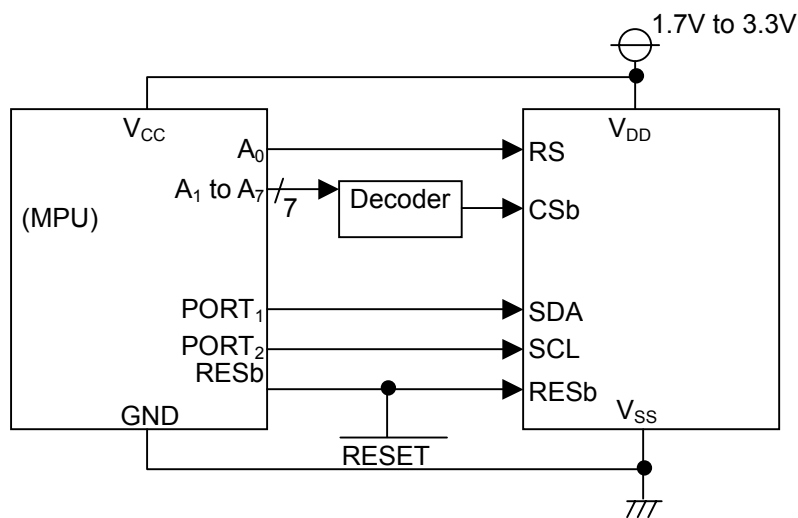
80-type MPU interface



68-type MPU interface



Serial interface



[CAUTION]

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